ADVANCED ANALOG

A Division of intech

T-51-10-90
T-51-10-12

ADC574A/ADC674A

HYBRID 12-BIT A/D CONVERTER WITH μP INTERFACE

DESCRIPTION

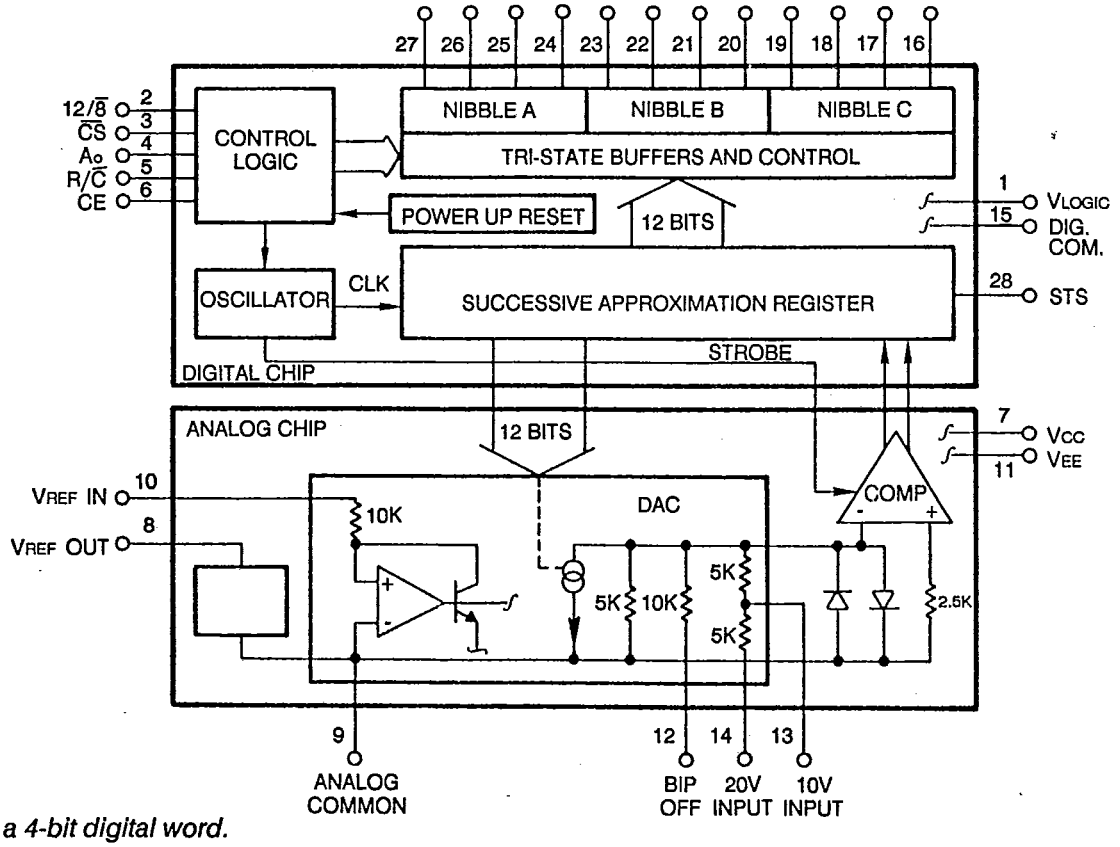
The ADC574A/674A is a 12-bit analog-to-digital converter that contains a +10V reference, clock, tri-state outputs plus a digital interface for μP control. It is a complete, successive approximation device and has four selectable input ranges. The voltage comparator features a high PSRR, plus a high speed current-mode latch. Low noise signal transmission is achieved by utilizing current rather than voltage between the analog and digital ICs. The clock oscillator is current controlled and features 12μs (typ) conversion time for the ADC674A and 20μs (typ) for the ADC574A.

Power requirements are +5V and ±12V to ±15V. Laser trimming assures that linearity, gain and offset accuracy meet or exceed specifications.

FEATURES

- Low cost 12-bit A/D converter
- Small 28-pin hermetic DIP package
- Contains +10V reference, clock, tri-state outputs, μP interface
- Low noise
- Full 8 or 16-bit μP interface
- 12μsec or 20μsec conversion time
- Military version available

BLOCK DIAGRAM



Nibble is a 4-bit digital word.

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SPECIFICATIONS

Typical @+25 °C with V_{CC} = +15V or +12V, V_{logic} = +5V, V_{EE} = -15V or -12V unless otherwise specified.
DC AND TRANSFER ACCURACY SPECIFICATIONS

MODEL	*574AJD *674AJD	*574AKD *674AKD	*574ALD *674ALD	*574ASD *674ASD	*574ATD *674ATD	*574AUD *674AUD	UNITS
Temperature Range	0 to +70			-55 to +125			°C
Resolution (max.)	12	12	12	12	12	12	bits
Linearity Error							
25 °C (max.)	±1	±1/2	±1/2	±1	±1/2	±1/2	LSB
T_{min} to T_{max} (max.)	±1	±1/2	±1/2	±1	±1	±1	LSB
Differential Linearity Error (Maximum resolution for which no missing codes is guaranteed)							
25 °C	11	12	12	11	12	12	bits
T_{min} to T_{max}	11	12	12	11	12	12	bits
Unipolar Offset (max.) (Adjustable to zero)	±2	±2	±2	±2	±2	±2	LSB
Bipolar Offset (max.) (adjustable to zero)	±10	±4	±4	±10	±4	±4	LSB
Full Scale Calibration Error							
25 °C (max.) with fixed 50Ω resistor from REF OUT to REF IN (Adjustable to zero)	0.3	0.3	0.3	0.3	0.3	0.3	% of FS
T_{min} to T_{max}							
(No adjustment at +25 °C)	0.5	0.4	0.35	0.8	0.6	0.4	% of FS
(With adjustment to zero at +25 °C)	0.22	0.12	0.05	0.5	0.25	0.12	% of FS
Temperature Coefficients							
Guaranteed max. change, T_{min} to T_{max} (using internal reference)							
Unipolar Offset	±2	±1	±1	±2	±1	±1	LSB
	(10)	(5)	(5)	(5)	(2.5)	(2.5)	(ppm/°C)
Bipolar Offset	±2	±1	±1	±4	±2	±1	LSB
	(10)	(5)	(5)	(10)	(5)	(2.5)	(ppm/°C)
Full Scale Calibration	±9	±5	±2	±20	±10	±5	LSB
	(45)	(25)	(10)	(50)	(25)	(12.5)	(ppm/°C)
Power Supply Rejection							
Max. change in Full Scale Calibration							
+13.5V<V_{CC}<+16.5V or +11.4V<V_{CC}<+12.6V	±2	±1	±1	±2	±1	±1	LSB
+4.5V<V_{logic}<+5.5V	±1/2	±1/2	±1/2	±1/2	±1/2	±1/2	LSB
-16.5V<V_{EE}<-13.5V or -12.6V <V_{EE}<-11.4V	±2	±1	±1	±2	±1	±1	LSB
Analog Inputs							
Input Ranges							
Bipolar		-5 to +5			-5 to +5		volts
		-10 to +10			-10 to +10		volts
Unipolar		0 to +10			0 to +10		volts
		0 to +20			0 to +20		volts
Input Impedance							
10V span		5k, ±25%			5k, ±25%		ohms
20V span		10k, ±25%			10k, ±25%		ohms
Power Supplies							
Operating Voltage Range							
V_{logic}		+4.5 to +5.5			+4.5 to +5.5		volts
V_{CC}		+11.4 to +16.5			+11.4 to +16.5		volts
V_{EE}		-11.4 to -16.5			-11.4 to -16.5		volts
Operating Current							
I_{logic}		7 typ, 15 max			7 typ, 15 max		mA
I_{CC}		11 typ, 15 max			11 typ, 15 max		mA
I_{EE}		21 typ, 28 max			21 typ, 28 max		mA
Power Dissipation		515 typ, 720 max			515 typ, 720 max		mW
Internal Reference Voltage		+10.00 ±0.1 max			+10.00 ±0.1 max		volts
Output Current,[1] available for external loads (External load should not change during conversion.)		2.0 max			2.0 max		mA

1. *When supplying an external load and operating on ±12V supplies, a buffer must be provided on the reference point.*

* All part numbers have "ADC" preface.

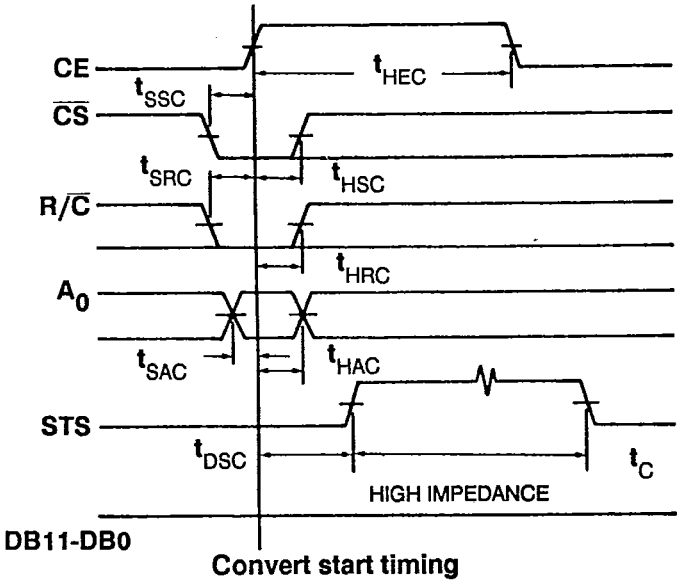
Consult factory for devices with military screening.

CE	$\overline{CS}$	R/$\overline{C}$	12/$\overline{8}$	A0	Operation
0	X	X	X	X	None
X	1	X	X	X	None
↑	0	0	X	0	Initiate 12 bit conversion
↑	0	0	X	1	Initiate 8 bit conversion
1	↓	0	X	0	Initiate 12 bit conversion
1	↓	0	X	1	Initiate 8 bit conversion
1	0	↓	X	0	Initiate 12 bit conversion
1	0	↓	X	1	Initiate 8 bit conversion
1	0	1	1	X	Enable 12 bit output
1	0	1	0	0	Enable 8 MSBs only
1	0	1	0	1	Enable 4 LSBs plus 4 trailing zeros

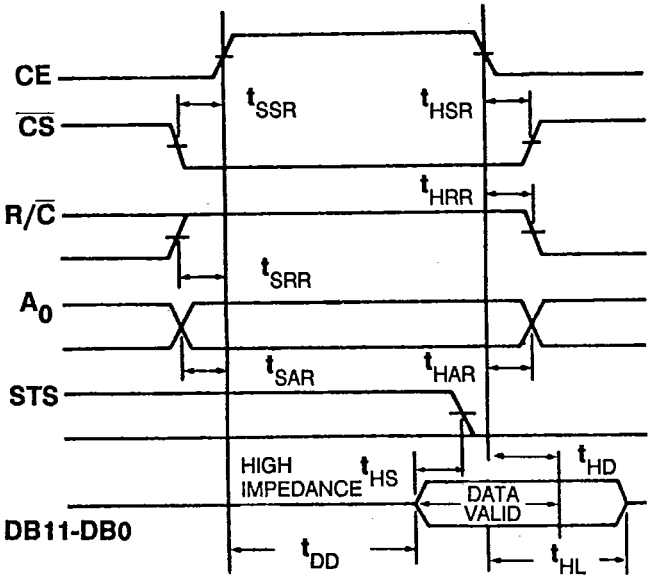
Truth table for control inputs

The output data buffers remain in a high impedance state until four conditions are met: R/$\overline{C}$ high, STS low, CE high and $\overline{CS}$ low. At that time, data lines become active according to the state of inputs 12/$\overline{8}$ and A0. Refer to Timing Diagram.

TIMING DIAGRAM



Convert start timing



Read cycle timing

INDEPENDENT OPERATION

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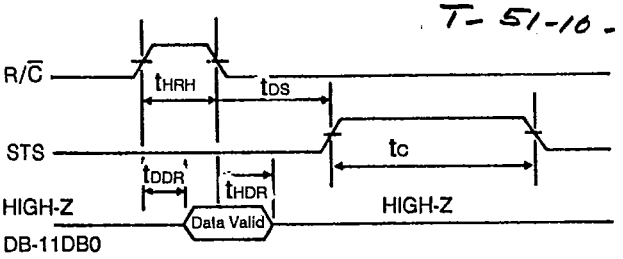
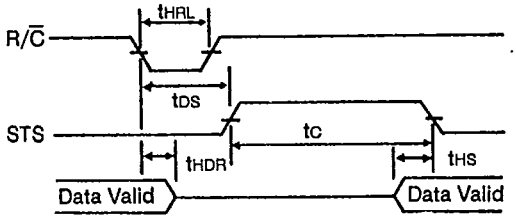
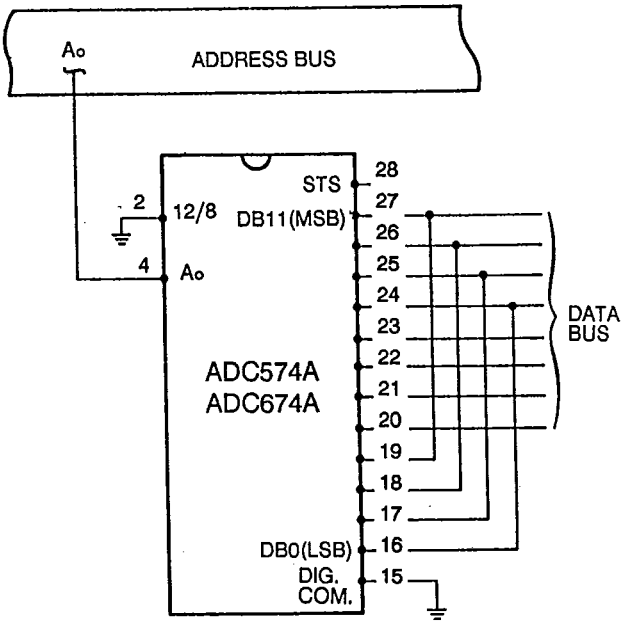


High pulse for R/$\overline{C}$ outputs enabled while R/C high, otherwise HIGH-Z.



Low pulse for R/$\overline{C}$ outputs enabled after conversion.

The independent control interface requires one control line connected to R/$\overline{C}$. CE and 12/$\overline{8}$ are wired high, $\overline{CS}$ and A0 are wired low. Output data will have 12-bit words each. The R/$\overline{C}$ signal may have any duty cycle within and including the parameters shown in the diagram.



8-bit data bus interface

Byte 1

X X X X X X X X

MSB

Byte 2

X X X X 0 0 0 0

LSB

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Symbol	Parameter	Min	Typ	Max	Units
t_{HRL}	Low R/$\overline{C}$ pulse width	50			ns
t_{DS}	STS delay from R/$\overline{C}$			200	ns
t_{HDR}	Data valid after R/$\overline{C}$ low	25			ns
t_{HS}	STS delay after data valid	100	300	600	ns
t_{HRH}	High R/$\overline{C}$ pulse width	150			ns
t_{DDR}	Data access time	150			ns

Timing Specifications (+25 °C)

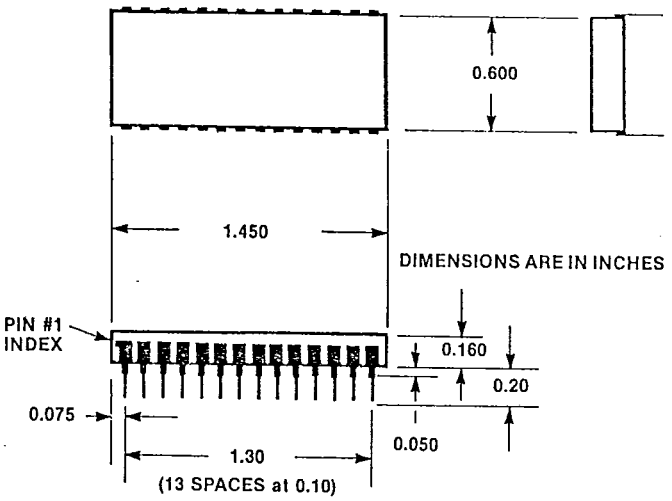
SYMBOL	PARAMETER	Min	Typ	Max	Units
Convert Mode					
t_{DSC}	STS delay from CE		100	200	ns
t_{HEC}	$\overline{CE}$ pulse width	50	30		ns
t_{SSC}	$\overline{CS}$ to CE setup	50	20		ns
t_{HSC}	$\overline{CS}$ low during CE high	50	20		ns
t_{SRC}	R/$\overline{C}$ to CE setup	50	0		ns
t_{HRC}	R/$\overline{C}$ low during CE high	50	20		ns
t_{SAC}	A_0 to CE setup	0	0		ns
t_{HAC}	A_0 valid during CE high	50	20		ns
t_C	ADC574A				
	Conversion time, 12-bit cycle	15	20	25	µs
	8-bit cycle	10	13	17	µs
t_C	ADC674A				
	Conversion time, 12-bit cycle	9	12	15	µs
	8-bit cycle	6	8	10	µs
Read Mode					
t_{DD}	Access time from CE		75	150	ns
t_{HD}	Data valid after CE low	25	35		ns
t_{HL}	Output float delay ADC574A		100	125	ns
t_{HL}	Output float delay ADC674A		100	150	ns
t_{SSR}	$\overline{CS}$ to CE setup	50	0		ns
t_{SRR}	R/$\overline{C}$ to CE setup	0	0		ns
t_{SAR}	A_0 to CE setup	50	25		ns
t_{HSR}	$\overline{CS}$ valid after CE low	0	0		ns
t_{HRR}	R/$\overline{C}$ high after CE low	0	0		ns
t_{HAR}	A_0 valid after CE high	50	25		ns
t_{HS}	STS delay after data valid	100	300	600	ns

Note: Time is measured from 50% level of digital transitions.

PIN DESIGNATION

Pin 1 +5V supply, V_{logic}	Pin 28 Status, STS
Pin 2 Data mode select, 12/$\overline{8}$	Pin 27 DB11 MSB
Pin 3 Chip select, $\overline{CS}$	Pin 26 DB10
Pin 4 Byte address/short cycle, A_0	Pin 25 DB9
Pin 5 Read/convert, R/$\overline{C}$	Pin 24 DB8
Pin 6 Chip enable, CE	Pin 23 DB7
Pin 7 +15V supply, V_{CC}	Pin 22 DB6
Pin 8 +10V reference, REF OUT	Pin 21 DB5
Pin 9 Analog common, AC	Pin 20 DB4
Pin 10 Reference input, REF IN	Pin 19 DB3
Pin 11 -15V supply, V_{EE}	Pin 18 DB2
Pin 12 Bipolar offset, BIP OFF	Pin 17 DB1
Pin 13 10V span input, 10V IN	Pin 16 DB0 LSB
Pin 14 20V span input, 20V IN	Pin 15 Digital Common

MECHANICAL OUTLINE



PART NUMBER

MODEL	TEMP RANGE	LINEARITY ERROR MAX. (Tmin to Tmax)	RESOLUTION (NO MISSING CODES, Tmin to Tmax)	FULL SCALE TC (PPM /°C max)
ADC574/674AJD	0 to 75 °C	±1 LSB	11 bits	45.0
ADC574/674AKD	0 to 75 °C	±1/2 LSB	12 bits	25.0
ADC574/674ALD	0 to 75 °C	±1/2 LSB	12 bits	10.0
ADC574/674ASD	-55 to +125 °C	±1 LSB	11 bits	50.0
ADC574/674ASD/B	-55 to +125 °C	±1 LSB	11 bits	50.0
ADC574/674ATD	-55 to +125 °C	±1 LSB	12 bits	25.0
ADC574/674ATD/B	-55 to +125 °C	±1 LSB	12 bits	25.0
ADC574/674AUD	-55 to +125 °C	±1 LSB	12 bits	12.5
ADC574/674AUD/B	-55 to +125 °C	±1 LSB	12 bits	12.5

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