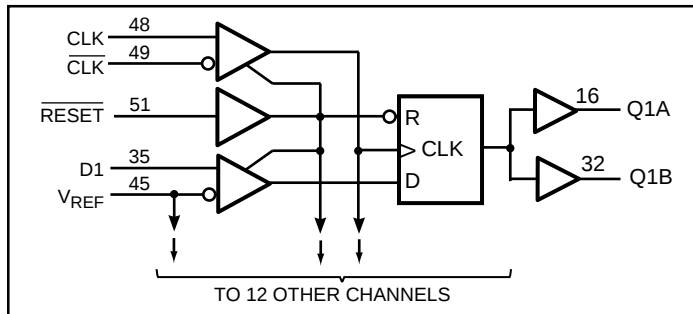


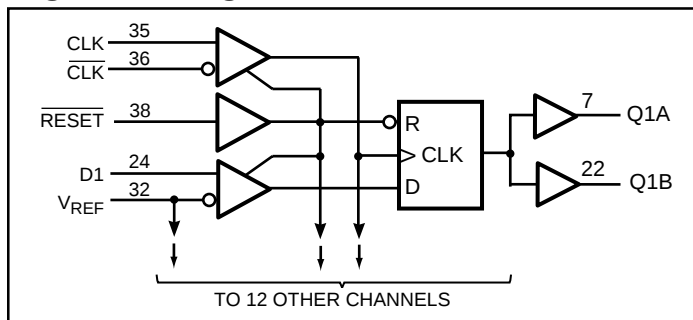
Product Features

- PI74 SSTV16859 is designed for low-voltage operation, $V_{DD} = V_{DDQ} = 2.3V$ to $2.7V$
- Supports SSTL_2 Class II specifications on outputs
- All Inputs are SSTL_2 Compatible, except $\overline{RESET}$ which is LVC MOS.
- Designed for DDR Memory
- Flow-Through Architecture
- Packages:
64-pin, 240-mil wide plastic TSSOP (A)
56-pin, Plastic Very Thin Fine Pitch Quad Flat
No Lead QFN (ZB)

Logic Block Diagram - TSSOP



Logic Block Diagram - QFN



Product Pin Description

Pin Name	Description
$\overline{RESET}$	Reset (Active Low) LVC MOS
CLK	Clock Input, Positive Differential Input
$\overline{CLK}$	Clock Input, Negative Differential Input
D	Data Input, D1-D13
Q	Data Output, Q1-Q13
GND	Ground
V_{DD}	Core Supply Voltage, 2.5V Nominal
V_{DDQ}	Output Supply Voltage, 2.5V Nominal
V_{REF}	Input Reference Voltage, 1.25V Nominal

Product Description

Pericom Semiconductor's PI74SSTV16859 logic circuit is produced using the Company's advanced 0.35 micron CMOS technology, achieving industry leading speed.

All inputs are compatible with the JEDEC standard for SSTL_2, except the LVC MOS reset ($\overline{RESET}$) input. All outputs are SSTL_2, Class II compatible.

The device operates from a differential clock (CLK and $\overline{CLK}$). Data registered at the crossing of CLK going HIGH, and $\overline{CLK}$ going LOW.

The PI74SSTV16859 supports low-power standby operation. When $\overline{RESET}$ is LOW, the differential input receivers are disabled, and undriven (floating) data, clock and reference voltage (V_{REF}) inputs are allowed. In addition, when $\overline{RESET}$ is LOW, all registers are reset, and all outputs are forced LOW. The LVC MOS $\overline{RESET}$ input must always be held at a valid logic HIGH or LOW level.

To ensure defined outputs from the register before a stable clock has been supplied, $\overline{RESET}$ must be held in the LOW state during power up.

In the DDR DIMM application, $\overline{RESET}$ is specified to be completely asynchronous with respect to CLK and $\overline{CLK}$. Therefore, no timing relationship can be guaranteed between the two. When entering $\overline{RESET}$, the register will be cleared and the outputs will be driven LOW quickly, relative to the time to disable the differential input receivers, thus ensuring no glitches on the output. However, when coming out of $\overline{RESET}$, the register will become active quickly, relative to the time to enable the differential input receivers. When the data inputs are LOW, and the clock is stable, during the time from the LOW-to-HIGH transition of $\overline{RESET}$ until the input receivers are fully enabled, the design must ensure that the outputs will remain LOW.

Pericom's PI74SSTV16859 is characterized for operation from $0^{\circ}C$ to $70^{\circ}C$.

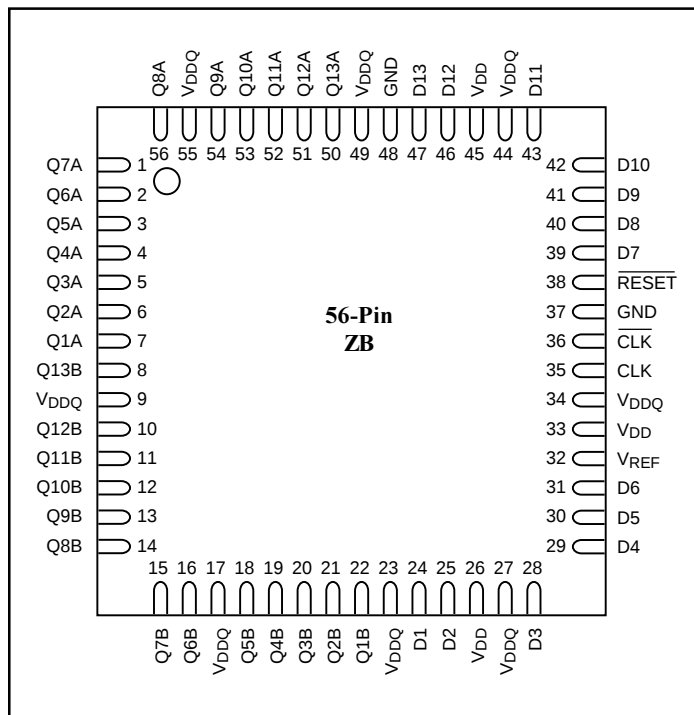
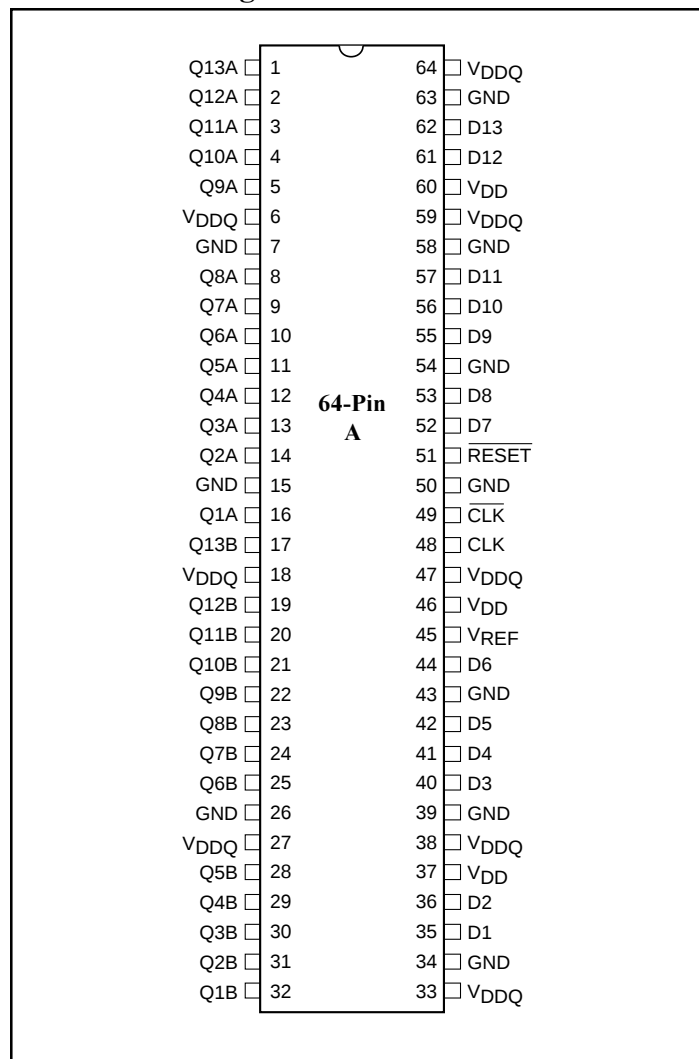
Truth Table⁽¹⁾

Inputs				Outputs
$\overline{RESET}$	CLK	$\overline{CLK}$	D	Q
L	X or Floating	X or Floating	X or Floating	L
H	↑	↓	H	H
H	↑	↓	L	L
H	L or H	L or H	X	$Q_0^{(2)}$

Notes:

- H = High Signal Level
L = Low Signal Level
↑ = Transition LOW-to-HIGH
↓ = Transition HIGH-to-LOW
X = Irrelevant or floating
- Output level before the indicated steady state input conditions were established.

Product Pin Configurations



Maximum Ratings (Above which the useful life may be impaired. For user guidelines, not tested.)

Item	Symbol/ Conditions	Ratings	Units
Storage temperature	T_{stg}	-65 to 150	°C
Supply voltage	V_{DD} or V_{DDQ}	-0.5 to 3.6	V
Input voltage ^(1,2)	V_I	-0.5 to V_{DD} +0.5	
Output voltage ^(1,2)	V_O	-0.5 to V_{DDQ} +0.5	
Input clamp current	$I_{IK}, V_I < 0$ or $V_I > V_{DD}$	±50	mA
Output clamp current	$I_{OK}, V_O < 0$ or $V_O > V_{DDQ}$	±50	
Continuous output current	$I_O, V_O = 0$ to V_{DDQ}	±50	
V_{DD}, V_{DDQ} or GND current/pin	I_{DD}, I_{DDQ} or I_{GND}	±100	
Package Thermal Impedance ⁽³⁾	θ_{JA}	55	°C/W

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

1. The input and output negative voltage ratings may be excluded if the input and output clamp ratings are observed.
2. This value is limited to 3.6V Maximum.
3. The package thermal impedance is calculated in accordance with JESD 51.

Recommended Operating Conditions⁽⁴⁾

Parameters	Description		Min.	Nom.	Max.	Units
V _{DD}	Supply Voltage		2.3	2.5	2.7	V
V _{DDQ}	I/O Supply Voltage		2.3	2.5	2.7	
V _{REF}	Reference Voltage V _{REF} = 0.5X V _{DDQ}		1.15	1.25	1.35	
V _{TT}	Termination Voltage		V _{REF} −0.04	V _{REF}	V _{REF} +0.04	
V _I	Input Voltage	Data Inputs	0		V _{DD}	
V _{IH}	AC High -Level Input Voltage		V _{REF} +310mV			
V _{IL}	AC Low -Level Input Voltage				V _{REF} − 310mV	
V _{IH}	DC High -Level Input Voltage		V _{REF} +150mV			
V _{IL}	DC Low -Level Input Voltage				V _{REF} −150mV	
V _{IH}	High -Level Input Voltage	$\overline{\text{RESET}}$	1.7			
V _{IL}	Low -Level Input Voltage				0.7	
V _{ICR}	Common-mode input range	CLK, $\overline{\text{CLK}}$	0.97		1.53	
V _{ID}	Differential Input Voltage		360			
I _{OH}	High-Level Output Current				−20	mA
I _{OL}	Low-Level Output Current				20	
T _A	Operating Free-Air Temperature		0		70	°C

Note:

4. The $\overline{\text{RESET}}$ input of the device must be held at V_{DD} or GND to ensure proper device operation. The differential inputs must not be floating, unless RESET is LOW.

DC Electrical Characteristics

(Over the Operating Range, $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$, $V_{DD} = 2.5\text{V} \pm 200\text{mV}$, $V_{DDQ} = 2.5\text{V} \pm 200\text{mV}$)

Parameters		Test Conditions	V_{DD}	Min.	Typ.	Max.	Units
V_{IK}		$I_I = -18\text{mA}$	2.3V			-1.2	V
V_{OH}		$I_{OH} = -100\mu\text{A}$	2.3V-2.7V	$V_{DD}-0.2$			
		$I_{OH} = -16\text{mA}$	2.3V	1.95			
V_{OL}		$I_{OL} = 100\mu\text{A}$	2.3V-2.7V			0.2	
		$I_{OH} = 16\text{mA}$	2.3V			0.35	
I_I	All Inputs	$V_I = V_{DD}$ or GND	2.7V			± 5	μA
I_{DD}	Standby (Static)	$\overline{\text{RESET}} = \text{GND}$	2.7V			10	
	Operating (Static)	$\overline{\text{RESET}} = V_{DD}$, $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$				TBD	mA
I_{DDD}	Dynamic operating - clock only	$\overline{\text{RESET}} = V_{DD}$, $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$, CLK and $\overline{\text{CLK}}$ switching 50% duty cycle.				TBD	$\mu\text{A}/\text{clock MHz}$
	Dynamic Operating - per each data input	$\overline{\text{RESET}} = V_{DD}$, $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$, CLK and $\overline{\text{CLK}}$ switching 50% duty cycle. One data input switching at half clock frequency, 50% duty cycle.				TBD	$\mu\text{A}/\text{clock MHz}/\text{data input}$
r_{OH}	Output High	$I_O = -20\text{mA}$	2.3 to 2.7V	TBD		TBD	Ω
r_{OL}	Output Low	$I_O = 20\text{mA}$					
$r_{O(\Delta)}$	$ r_{OH} - r_{OL} $ each separate bit	$I_O = 20\text{mA}$, $T_A = 25^\circ\text{C}$	2.5V			TBD	
C_i	Data Inputs	$V_I = V_{REF} \pm 350\text{mV}$		2.5		3.5	pF
	CLK and $\overline{\text{CLK}}$	$V_{ICR} = 1.25\text{V}$, $V_{I(PP)} = 360\text{mV}$					
	$\overline{\text{RESET}}$	$V_I = V_{DD}$ or GND		TBD		TBD	

Timing Requirements (over recommended operating free-air temperature range, unless otherwise noted)

		V_{DD} = 2.5V ±0.2V		Units
		Min.	Max.	
f_{clock}	Clock frequency		200	MHz
t_W	Pulse Duration, CLK, $\overline{\text{CLK}}$ high or low	2.5		ns
$t_{\text{act}}^\dagger$	Differential Inputs active time, data inputs must be low after $\overline{\text{RESET}}$ high.	22		
$t_{\text{inact}}^\dagger$	Differential Inputs inactive time, data and clock inputs must be held at valid levels (not floating) after $\overline{\text{RESET}}$ Low.			
t_{su}	Setup time, fast slew rate ^(5,7)	Data before CLK $\uparrow$, $\overline{\text{CLK}}\downarrow$	0.75	
	Setup time, slow slew rate ^(6,7)		0.9	
t_h	Hold time, fast slew rate ^(5,7)	Data after CLK $\uparrow$, $\overline{\text{CLK}}\downarrow$	0.75	
	Hold time, slow slew rate ^(6,7)		0.9	

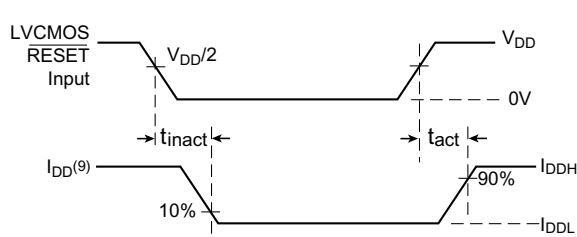
- Notes:**
- 5. For data signal input slew rate $\geq 1\text{V/ns}$.
 - 6. For data signal input slew rate $\geq 0.5\text{V/ns}$ and $< 1\text{V/ns}$.
 - 7. CLK, $\overline{\text{CLK}}$ signals input slew rates are $\geq 1\text{V/ns}$.
 - † This parameter is not necessarily production tested.

Switching characteristics

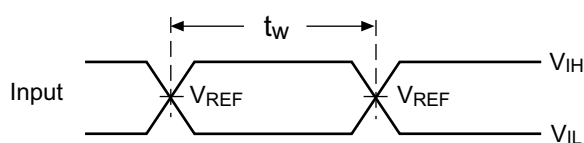
Over recommended operating free-air temperature range, unless otherwise noted. (See test circuits and switching waveforms).

Parameter	From (Input)	To (Output)	V_{DD} = 2.5V ±0.2V			Units
			Min.	Typ.	Max.	
f_{max}			200			MHz
t_{pd}	CLK, $\overline{\text{CLK}}$	Q	1.1		2.8	ns
t_{phl}	$\overline{\text{RESET}}$	Q			5.0	

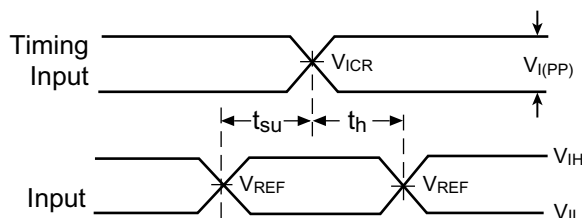
Test Circuit and Switching Waveforms



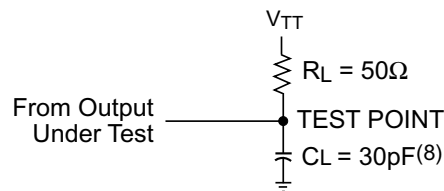
**Voltage and Current Waveforms
Input Active and Inactive Times**



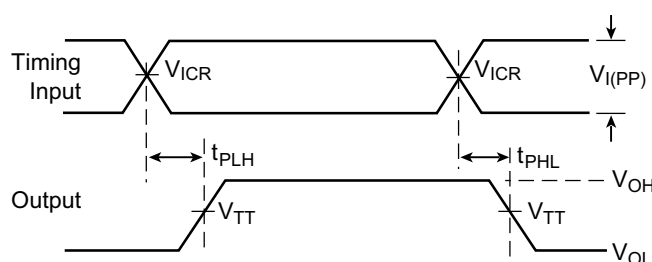
Voltage Waveforms - Pulse Duration



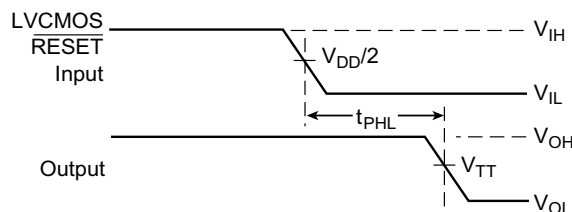
Voltage Waveforms - Setup and Hold Times



Load Circuit



Voltage Waveforms - Propagation Delay Times



Voltage Waveforms - Propagation Delay Times

Parameter Measurement Information ($V_{DD}=2.5V \pm 0.2V$)

Notes:

8. C_L includes probe and jig capacitance.
9. I_{DD} tested with clock and data inputs held at V_{DD} or GND, and $I_O = 0mA$.
10. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 MHz$, $Z_O = 50 ohms$.
Input slew rate = $1V/ns \pm 20\%$ (unless otherwise specified).
11. The outputs are measured one at a time with one transition per measurement.
12. $V_{TT} = V_{REF} = V_{DDQ}/2$
13. $V_{IH} = V_{REF} + 350mV$ (ac voltage levels) for SSTL inputs. $V_{IH} = V_{DD}$ for LVC MOS input.
14. $V_{IL} = V_{REF} + 350mV$ (ac voltage levels) for SSTL inputs. $V_{IL} = GND$ for LVC MOS input.
15. t_{PLH} and t_{PHL} are the same as t_{pd} .



64

1

.665
.673

16.9
17.1

.236
.244

6.0
6.2

1.20
.047 Max.

SEATING PLANE

.004
0.10

.0197
BSC
0.50

.007
.011

0.17
0.27

.002
.006

0.05
0.15

.45
0.75

.018
.030

.319
8.1

BSC

.004
.008

0.09
0.20

X.XX DENOTES DIMENSIONS
X.XX IN MILLIMETERS

The drawing illustrates the JEDEC MO-195 package with the following dimensions and features:

- Top View:**
 - Overall width: 311 (7.90 / 8.10)
 - Overall height: 311 (7.90 / 8.10)
 - Pin 1 indicator: A circle in the top-left corner.
 - Pin pitch: 0.25 (6.35)
- Side View:**
 - Maximum height: 0.33 (0.84) MAX
 - Reference height: 0.08 (2.03) REF
 - Stand-off height: 0 (0.015)
 - Lead thickness: 0.10 (2.54)
 - Lead width: 0.04 (1.01)
- Bottom View:**
 - Pin pitch: 0.12 (3.30) / 0.19 (4.80)
 - Pin width: 0.019 (0.50) BSE
 - Pin spacing: 0.007 (0.18) / 0.012 (0.30)
 - Pin length: 0.10 (2.54) C A B
 - Internal feature: R 0.25 x 3
 - Chamfer: 0.25 Chamfer
 - Overall width: 199 (5.05) / 211 (5.35)
 - Overall length: 171 (4.35) / 183 (4.65)

Legend:
 X.XX
 X.XX DENOTES DIMENSIONS IN MILLIMETERS

Notes:
 1. Controlling dimensions in millimeters
 2. Ref: JEDEC MO-195 (Issue B)

Ordering Code	Package Type	Temperature Range
PI74SSTV16859A	64-Pin TSSOP	0°C to 70°C
PI74SSTV16859ZB	56-Pin QFN	

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