High Accuracy Ultralow I_Q, 500 mA anyCAP® Low Dropout Regulator

ADP3335

FEATURES

High Accuracy Over Line and Load: ±0.9% @ 25°C, ±1.8% Over Temperature
Ultralow Dropout Voltage: 200 mV (Typ) @ 500 mA
Requires Only C_O = 1.0 μF for Stability
anyCAP = Stable with Any Type of Capacitor (Including MLCC)
Current and Thermal Limiting
Low Noise
Low Shutdown Current: < 1.0 μA
2.6 V to 12 V Supply Range
–40°C to +85°C Ambient Temperature Range
Ultrasmall Thermally-Enhanced 8-Lead MSOP Package

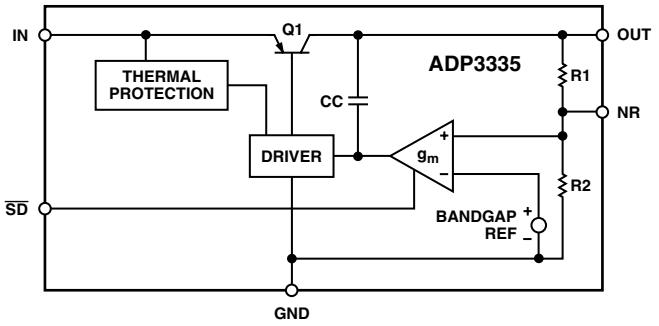
APPLICATIONS

PCMCIA Card
Cellular Phones
Camcorders, Cameras
Networking Systems, DSL/Cable Modems
Cable Set-Top Box
MP3/CD Players
DSP Supply

GENERAL DESCRIPTION

The ADP3335 is a member of the ADP330x family of precision low dropout anyCAP voltage regulators. The ADP3335 operates with an input voltage range of 2.6 V to 12 V and delivers a continuous load current up to 500 mA. The ADP3335 stands out from conventional LDOs with the lowest thermal resistance of any MSOP-8 package and an enhanced process that enables it to offer performance advantages beyond its competition. Its patented design requires only a 1.0 μF output capacitor for stability. This device is insensitive to output capacitor Equivalent Series Resistance (ESR), and is stable with any good quality capacitor, including ceramic (MLCC) types for space-restricted applications. The ADP3335 achieves exceptional accuracy of ±0.9% at room temperature and ±1.8% over temperature, line, and load. The dropout voltage of the ADP3335 is only 200 mV (typical) at 500 mA. This device also includes a safety current limit, thermal overload protection and a shutdown feature. In shutdown mode, the ground current is reduced to less than 1 μA. The ADP3335 has ultralow quiescent current 80 μA (typical) in light load situations.

FUNCTIONAL BLOCK DIAGRAM



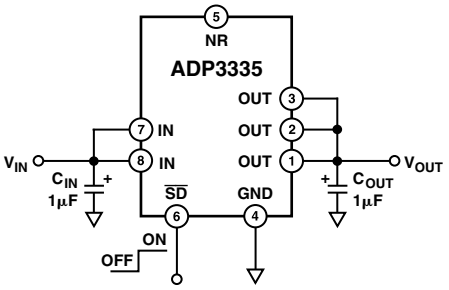


Figure 1. Typical Application Circuit

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ADP3335–SPECIFICATIONS[1, 2, 3] (V_{IN} = 6.0 V, C_{IN} = C_{OUT} = 1.0 µF, T_A = –40°C to +85°C, unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
OUTPUT						
Voltage Accuracy[4]	V_{OUT}	V_{IN} = $V_{OUT(NOM)}$ + 0.4 V to 12 V I_L = 0.1 mA to 500 mA T_A = 25°C	–0.9		+0.9	%
		V_{IN} = $V_{OUT(NOM)}$ + 0.4 V to 12 V I_L = 0.1 mA to 500 mA T_A = 85°C	–1.8		+1.8	%
		V_{IN} = $V_{OUT(NOM)}$ + 0.4 V to 12 V I_L = 0.1 mA to 500 mA T_J = 150°C	–2.3		+2.3	%
Line Regulation[4]		V_{IN} = $V_{OUT(NOM)}$ + 0.4 V to 12 V I_L = 0.1 mA T_A = 25°C		0.04		mV/V
Load Regulation		I_L = 0.1 mA to 500 mA T_A = 25°C		0.04		mV/mA
Dropout Voltage	V_{DROP}	V_{OUT} = 98% of $V_{OUT(NOM)}$				
		I_L = 500 mA		200	370	mV
		I_L = 300 mA		140	230	mV
		I_L = 50 mA		30	110	mV
		I_L = 0.1 mA		10	40	mV
Peak Load Current	I_{LDPK}	V_{IN} = $V_{OUT(NOM)}$ + 1 V		800		mA
Output Noise	V_{NOISE}	f = 10 Hz–100 kHz, C_L = 10 µF I_L = 500 mA, C_{NR} = 10 nF		47		µV rms
		f = 10 Hz–100 kHz, C_L = 10 µF I_L = 500 mA, C_{NR} = 0 nF		95		µV rms
GROUND CURRENT						
In Regulation	I_{GND}	I_L = 500 mA		4.5	10	mA
		I_L = 300 mA		2.6	6	mA
		I_L = 50 mA		0.5	2.5	mA
		I_L = 0.1 mA		80	110	µA
In Dropout	I_{GND}	V_{IN} = $V_{OUT(NOM)}$ – 100 mV I_L = 0.1 mA		120	400	µA
In Shutdown	I_{GNDSD}	$\overline{SD}$ = 0 V, V_{IN} = 12 V		0.01	1	µA
SHUTDOWN						
Threshold Voltage	$V_{\overline{THSD}}$	ON	2.0			V
		OFF			0.4	V
$\overline{SD}$ Input Current	$I_{\overline{SD}}$	0 ≤ $\overline{SD}$ ≤ 5 V		1.2	3	µA
Output Current In Shutdown	$I_{\overline{OSD}}$	T_A = 25°C, V_{IN} = 12 V		1.2	5	µA
		T_A = 85°C, V_{IN} = 12 V		1.2	5	µA

NOTES
[1]All limits at temperature extremes are guaranteed via correlation using standard statistical quality control (SQC) methods.
[2]Ambient temperature of 85°C corresponds to a junction temperature of 125°C under pulsed full load test conditions.
[3]Application stable with no load.
[4]V_{IN} = 2.6 V to 12 V for models with $V_{OUT(NOM)}$ ≤ 2.2 V.

Specifications subject to change without notice.

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ABSOLUTE MAXIMUM RATINGS*

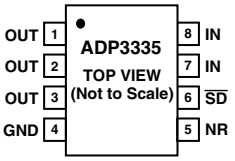
Input Supply Voltage . . . . . –0.3 V to +16 V
Shutdown Input Voltage . . . . . –0.3 V to +16 V
Power Dissipation . . . . . Internally Limited
Operating Ambient Temperature Range . . . . –40°C to +85°C
Operating Junction Temperature Range . . . –40°C to +150°C
θ_{JA} 2-layer . . . . . 153°C/W
θ_{JA} 4-layer . . . . . 110°C/W
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature Range (Soldering 10 sec) . . . . . 300°C
Vapor Phase (60 sec) . . . . . 215°C
Infrared (15 sec) . . . . . 220°C

*This is a stress rating only; operation beyond these limits can cause the device to be permanently damaged.

PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	Function
1, 2, 3	OUT	Output of the Regulator. Bypass to ground with a 1.0 µF or larger capacitor. All pins must be connected together for proper operation.
4	GND	Ground Pin.
5	NR	Noise Reduction Pin. Used for further reduction of output noise (see text for detail). Capacitor required if C_{OUT} > 3.3 µF.
6	$\overline{SD}$	Active Low Shutdown Pin. Connect to ground to disable the regulator output. When shutdown is not used, this pin should be connected to the input pin.
7, 8	IN	Regulator Input. All pins must be connected together for proper operation.

PIN CONFIGURATION



ORDERING GUIDE

Model	Output Voltage*	Package Option	Branding Information
ADP3335ARM-1.8	1.8 V	RM-8 (MSOP-8)	LFA
ADP3335ARM-2.5	2.5 V	RM-8 (MSOP-8)	LFC
ADP3335ARM-2.85	2.85 V	RM-8 (MSOP-8)	LFD
ADP3335ARM-3.3	3.3 V	RM-8 (MSOP-8)	LFE
ADP3335ARM-5	5 V	RM-8 (MSOP-8)	LFF

*Contact the factory for other output voltage options.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADP3335 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

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ADP3335–Typical Performance Characteristics (T_A = 25°C unless otherwise noted.)

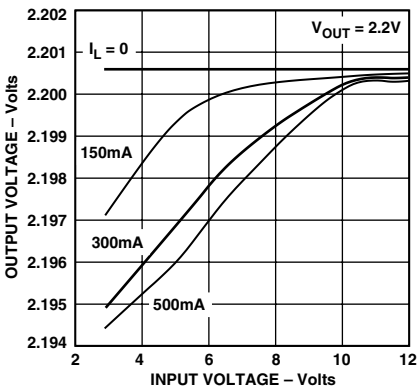

Figure 2. Line Regulation Output Voltage vs. Supply Voltage

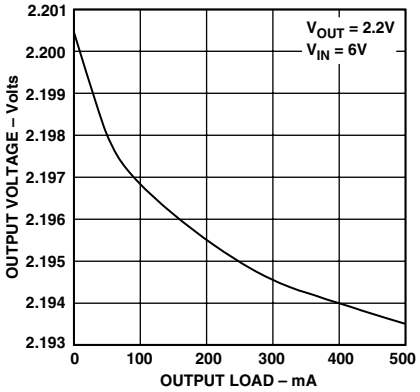

Figure 3. Output Voltage vs. Load Current

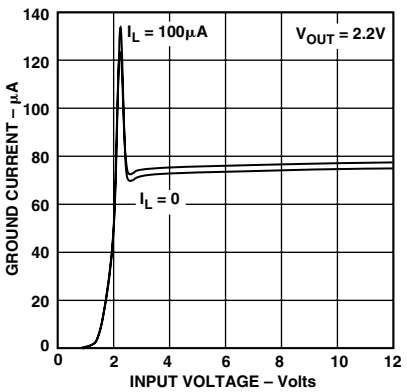

Figure 4. Ground Current vs. Supply Voltage

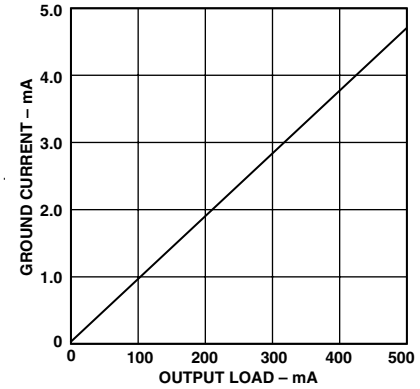

Figure 5. Ground Current vs. Load Current

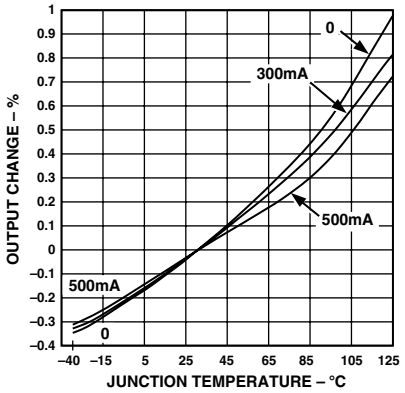

Figure 6. Output Voltage Variation % vs. Junction Temperature

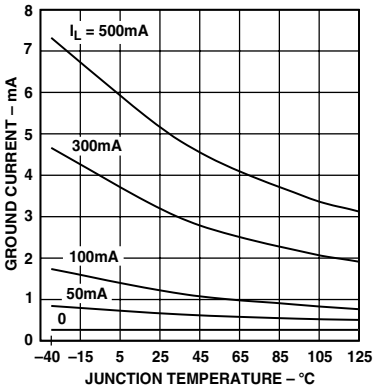

Figure 7. Ground Current vs. Junction Temperature

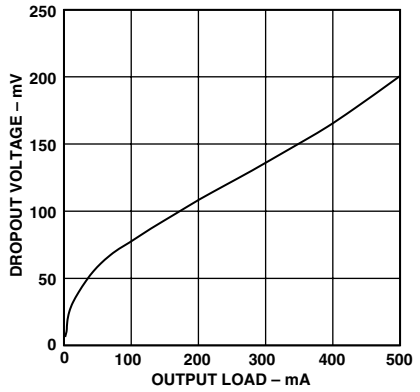

Figure 8. Dropout Voltage vs. Output Current

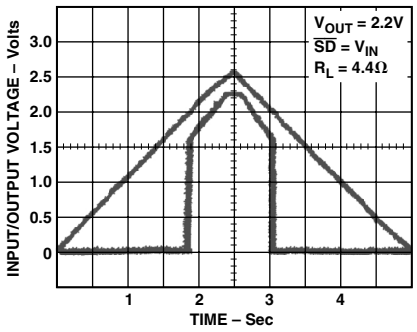

Figure 9. Power-Up/Power-Down

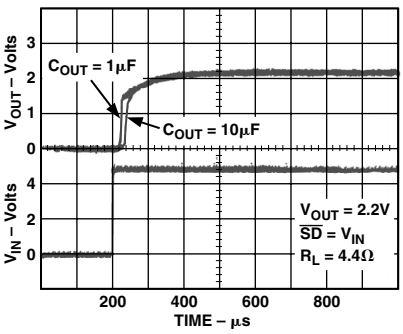

Figure 10. Power–Up Response

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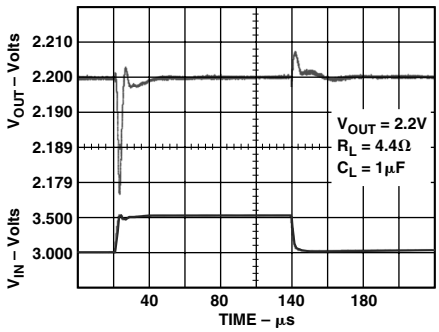

Figure 11. Line Transient Response

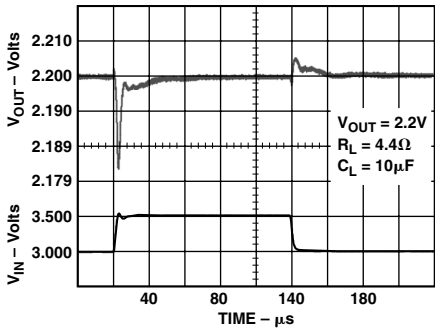

Figure 12. Line Transient Response

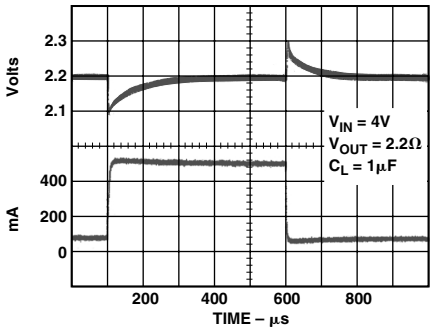

Figure 13. Load Transient Response

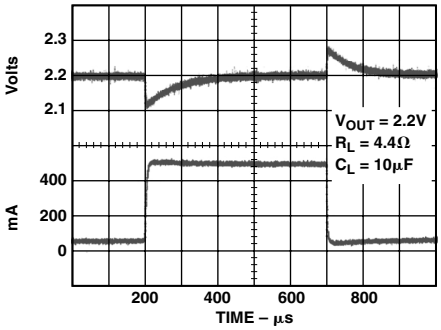

Figure 14. Load Transient Response

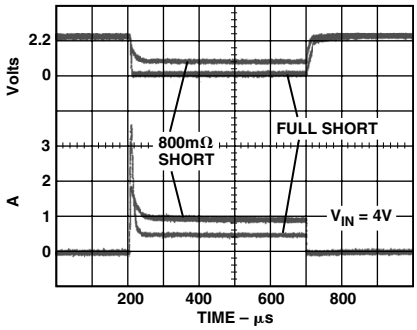

Figure 15. Short Circuit Current

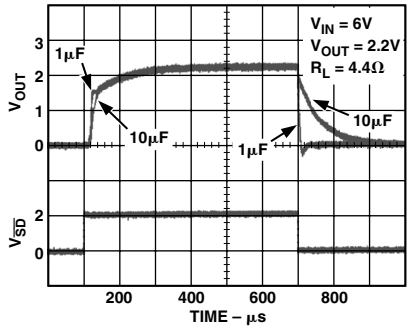

Figure 16. Turn On–Turn Off Response

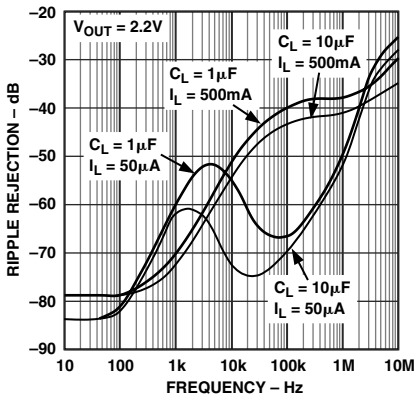

Figure 17. Power Supply Ripple Rejection

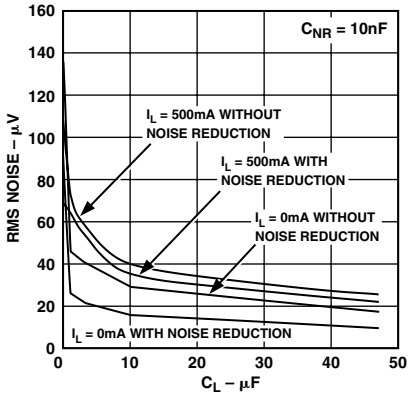

Figure 18. RMS Noise vs. C_L (10 Hz–100 kHz)

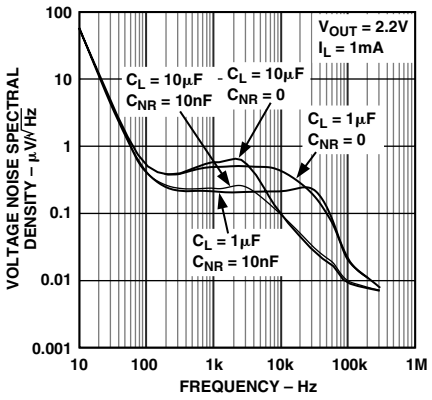

Figure 19. Output Noise Density

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THEORY OF OPERATION

The new anyCAP LDO ADP3335 uses a single control loop for regulation and reference functions. The output voltage is sensed by a resistive voltage divider consisting of R1 and R2 which is varied to provide the available output voltage option. Feedback is taken from this network by way of a series diode (D1) and a second resistor divider (R3 and R4) to the input of an amplifier.

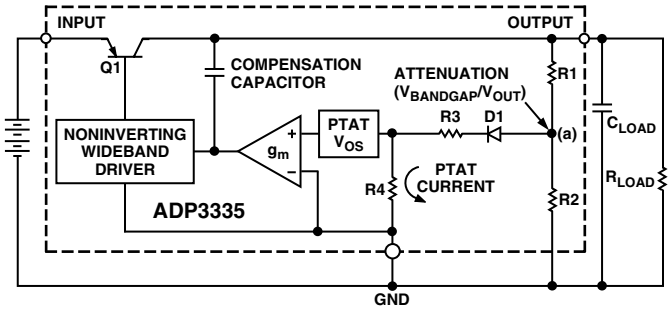

Figure 20. Functional Block Diagram

A very high gain error amplifier is used to control this loop. The amplifier is constructed in such a way that equilibrium produces a large, temperature-proportional input ,"offset voltage" that is repeatable and very well controlled. The temperature-proportional offset voltage is combined with the complementary diode voltage to form a "virtual bandgap" voltage, implicit in the network, although it never appears explicitly in the circuit. Ultimately, this patented design makes it possible to control the loop with only one amplifier. This technique also improves the noise characteristics of the amplifier by providing more flexibility on the trade-off of noise sources that leads to a low noise design.

The R1, R2 divider is chosen in the same ratio as the bandgap voltage to the output voltage. Although the R1, R2 resistor divider is loaded by the diode D1 and a second divider consisting of R3 and R4, the values can be chosen to produce a temperature stable output. This unique arrangement specifically corrects for the loading of the divider thus avoiding the error resulting from base current loading in conventional circuits.

The patented amplifier controls a new and unique noninverting driver that drives the pass transistor, Q1. The use of this special noninverting driver enables the frequency compensation to include the load capacitor in a pole-splitting arrangement to achieve reduced sensitivity to the value, type, and ESR of the load capacitance.

Most LDOs place very strict requirements on the range of ESR values for the output capacitor because they are difficult to stabilize due to the uncertainty of load capacitance and resistance. Moreover, the ESR value, required to keep conventional LDOs stable, changes depending on load and temperature. These ESR limitations make designing with LDOs more difficult because of their unclear specifications and extreme variations over temperature.

With the ADP3335 anyCAP LDO, this is no longer true. It can be used with virtually any good quality capacitor, with no constraint on the minimum ESR. This innovative design allows the circuit to be stable with just a small 1 µF capacitor on the output. Additional advantages of the pole-splitting scheme include superior line noise rejection and very high regulator gain, which leads to excellent line and load regulation. An impressive ±1.8% accuracy is guaranteed over line, load, and temperature.

Additional features of the circuit include current limit and thermal shutdown and noise reduction.

APPLICATION INFORMATION

Capacitor Selection

Output Capacitors: as with any micropower device, output transient response is a function of the output capacitance. The ADP3335 is stable with a wide range of capacitor values, types and ESR (anyCAP). A capacitor as low as 1 µF is all that is needed for stability; larger capacitors can be used if high output current surges are anticipated. The ADP3335 is stable with extremely low ESR capacitors (ESR ≈ 0), such as multilayer ceramic capacitors (MLCC) or OSCON. Note that the effective capacitance of some capacitor types may fall below the minimum at cold temperature. Ensure that the capacitor provides more than 1 µF at minimum temperature.

Input Bypass Capacitor

An input bypass capacitor is not strictly required but is advisable in any application involving long input wires or high source impedance. Connecting a 1 µF capacitor from IN to ground reduces the circuit's sensitivity to PC board layout. If a larger value output capacitor is used, then a larger value input capacitor is also recommended.

Noise Reduction

A noise reduction capacitor (C_{NR}) can be used to further reduce the noise by 6 dB–10 dB (Figure 18) low leakage capacitors in 10 pF–500 pF range provide the best performance. Since the noise reduction pin (NR) is internally connected to a high impedance node, any connection to this node should be carefully done to avoid noise pickup from external sources. The pad connected to this pin should be as small as possible and long PC board traces are not recommended.

When adding a noise reduction capacitor, maintain a minimum load current of 1 mA when not in shutdown.

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It is important to note that as C_{NR} increases, the turn-on time will be delayed. With NR values greater than 1 nF, this delay may be on the order of several milliseconds.

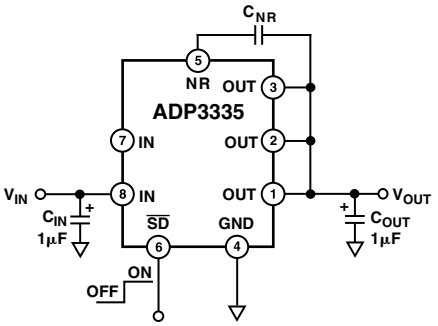

Figure 21. Typical Application Circuit

Paddle-Under-Lead Package

The ADP3335 uses a patented paddle-under-lead package design to ensure the best thermal performance in an MSOP-8 footprint. This new package uses an electrically isolated die attach that allows all pins to contribute to heat conduction. This technique reduces the thermal resistance to 110°C/W on a 4-layer board as compared to >160°C/W for a standard MSOP-8 leadframe. Figure 22 shows the standard physical construction of the MSOP-8 and the paddle-under-lead leadframe.

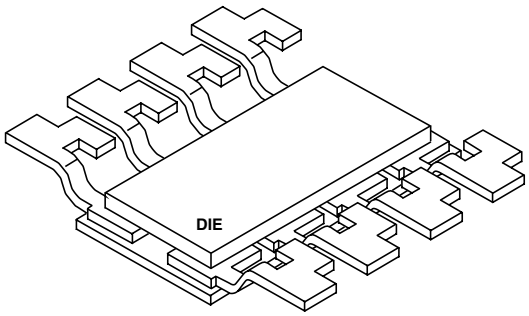

Figure 22. Thermally Enhanced Paddle-Under-Lead Package

Thermal Overload Protection

The ADP3335 is protected against damage from excessive power dissipation by its thermal overload protection circuit which limits the die temperature to a maximum of 165°C. Under extreme conditions (i.e., high ambient temperature and power dissipation) where die temperature starts to rise above 165°C, the output current is reduced until the die temperature has dropped to a safe level. The output current is restored when the die temperature is reduced.

Current and thermal limit protections are intended to protect the device against accidental overload conditions. For normal operation, device power dissipation should be externally limited so that junction temperatures will not exceed 150°C.

Calculating Junction Temperature

Device power dissipation is calculated as follows:

$$P_D = \left(V_{IN} - V_{OUT}\right) I_{LOAD} + \left(V_{IN}\right) I_{GND}$$

Where I_{LOAD} and I_{GND} are load current and ground current, V_{IN} and V_{OUT} are input and output voltages respectively.

Assuming I_{LOAD} = 400 mA, I_{GND} = 4 mA, V_{IN} = 5.0 V and V_{OUT} = 3.3 V, device power dissipation is:

$$P_D = (5 - 3.3)\ 400\ mA + 5.0(4\ mA) = 700\ mW$$

The proprietary package used in the ADP3335 has a thermal resistance of 110°C/W, significantly lower than a standard MSOP-8 package. Assuming a 4-layer board, the junction temperature rise above ambient temperature will be approximately equal to:

$$\Delta T_{JA} = 0.700\,W \times 110°C/W = 77.0°C$$

To limit the maximum junction temperature to 150°C, maximum allowable ambient temperature will be:

$$T_{AMAX} = 150°C - 77.0°C = 73.0°C$$

Printed Circuit Board Layout Consideration

All surface mount packages rely on the traces of the PC board to conduct heat away from the package.

In standard packages the dominant component of the heat resistance path is the plastic between the die attach pad and the individual leads. In typical thermally enhanced packages one or more of the leads are fused to the die attach pad, significantly decreasing this component. To make the improvement meaningful, however, a significant copper area on the PCB must be attached to these fused pins.

The patented paddle-under-lead frame design of the ADP3335 uniformly minimizes the value of the dominant portion of the thermal resistance. It ensures that heat is conducted away by all pins of the package. This yields a very low 110°C/W thermal resistance for an MSOP-8 package, without any special board layout requirements, relying only on the normal traces connected to the leads. This yields a 33% improvement in heat dissipation capability as compared to a standard MSOP-8 package. The thermal resistance can be decreased by, approximately, an additional 10% by attaching a few square cm of copper area to the IN pin of the ADP3335 package.

It is not recommended to use solder mask or silkscreen on the PCB traces adjacent to the ADP3335's pins since it will increase the junction-to-ambient thermal resistance of the package.

Shutdown Mode

Applying a TTL high signal to the shutdown ($\overline{SD}$) pin or tying it to the input pin, will turn the output ON. Pulling $\overline{SD}$ down to 0.4 V or below, or tying it to ground will turn the output OFF. In shutdown mode, quiescent current is reduced to much less than 1 µA.

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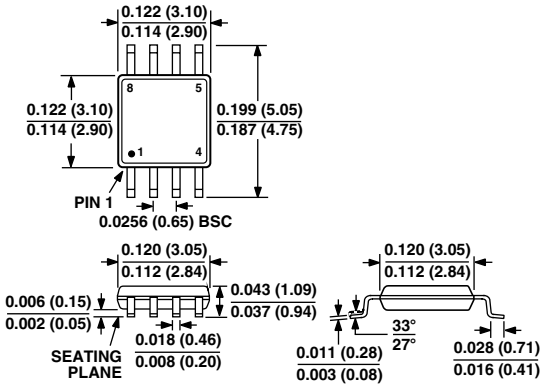
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

8-Lead mini_SO
(RM-8)



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