1.1 Scope.

This specification covers the detail requirements for a monolithic CMOS 16×16-bit digital multiplier integrated circuit.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number[1]
−1	ADSP-1016AS(X)/883B
−2	ADSP-1016AT(X)/883B

NOTE
[1]See paragraph 1.2.3 for package identifier.

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
D	D-64A	64-Pin DIP
E	E-68A	68-Contact LCC
G	G-68A	68-Lead Pin Grid Array

1.3 Absolute Maximum Ratings.

Supply Voltage . . . . . −0.3 V to 7 V
Input Voltage . . . . . −0.3 V to V_{DD}
Output Voltage . . . . . −0.3 V to V_{DD}
Operating Temperature Range (Ambient) . . . . . −55°C to +125°C
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature (Soldering 10 sec) . . . . . +300°C

1.5 Thermal Characteristics.

Thermal Resistance θ_{JC}: see MIL-M-38510, Appendix C.

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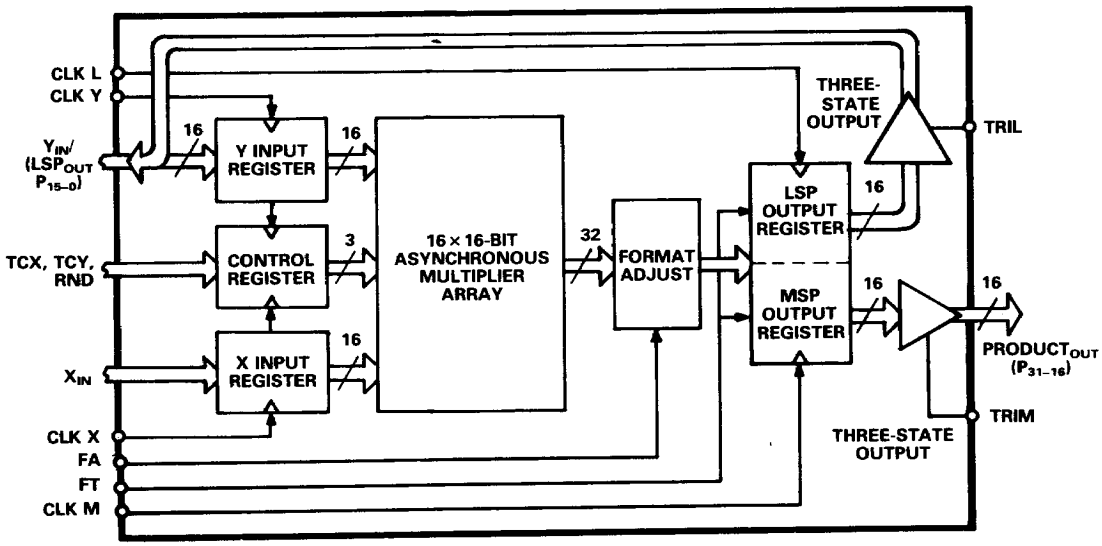
Parameter	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 9	Sub Group 10, 11	Test Condition[1]	Units
Digital Input High Voltage	V_{IH}	−1, 2	2.0	2.0	2.0			V_{DD} = max	V min
Digital Input Low Voltage	V_{IL}	−1, 2	0.8	0.8	0.8			V_{DD} = min	V max
Digital Output High Voltage	V_{OH}	−1, 2	2.4	2.4	2.4			V_{DD} = min I_{OH} = −0.4 mA	V min
Digital Output Low Voltage*	V_{OL}	−1, 2	0.4	0.6	0.6			V_{DD} = min I_{OL} = +4 mA	V max
Digital Input High Current	I_{IH}	−1, 2	10	10	10			V_{DD} = max V_{IN} = +5.0 V	μA max
Digital Input Low Current	I_{IL}	−1, 2	10	10	10			V_{DD} = max V_{IN} = 0.0 V	μA max
Three-State Leakage Current Low	I_{OZL}	−1, 2	50	50	50			V_{DD} = max V_{IL} = 0 V (High Z)	μA max
Three-State Leakage Current High	I_{OZH}	−1, 2	50	50	50			V_{DD} = max V_{IH} = max (High Z)	μA max
Supply Current*	I_{DD1}	−1, 2	45	55	55			V_{DD} = max; TTL Inputs; f = max	mA max
	I_{DD2}	−1, 2	35	40	40			V_{DD} = max All V_{IN} = 2.4 V	mA max
Output Delay*	t_D	−1, 2	20			35	35	Note 2	ns max
Three-State Enable* (High Z to Low)	t_{ENA}	−1, 2	20			35	35	Notes 2 and 3	ns max
Three-State Disable* (Low to High Z)	t_{DIS}	−1, 2	20			35	35	Notes 2 and 3	ns max
Clock Pulse Width	t_{PW}	−1, 2	15			15	15	Note 2	ns min
Input Data Setup Time*	t_{DS}	−1, 2	25			25	25	Note 2	ns min
Input Control Setup Time*	t_{CS}	−1, 2	30			30	30	Notes 2 and 3	ns min
Input Hold Time	t_H	−1, 2	2			2	2	Note 2	ns min
Unclocked Multiply Time*	t_{MUC}	−1	105			120	120	Note 2	ns max
		−2	90			105	105		
Clocked Multiply Time*	t_{MC}	−1	85			95	95	Note 2	ns max
		−2	70			80	80		

NOTES
*Indicates that a limit for this parameter has changed from REV. D.
[1]T_A = +25°C; V_{DD} = +4.5 V min to +5.5 V max (unless otherwise noted).
[2]TTL inputs of 0 V and +3.0 V; V_{DD} = +4.5 V, rise time = 5 ns, and timing transitions, per Figure 1, measured at +1.5 V (unless otherwise noted).
[3]Transitions measured per Figure 2.

Table 1.

REV. E

3.2.1 Functional Block Diagram and Terminal Assignments.



Functional Block Diagram

Pin Assignments

PIN NO.	FUNCTION		
	DIP	LCC	PIN-GRID
1	X4	X4	P0, Y0
2	X3	X3	P1, Y1
3	X2	X2	P2, Y2
4	X1	X1	P3, Y3
5	X0	X0	P4, Y4
6	TRIL	TRIL	P5, Y5
7	CLK L	CLK L	P6, Y6
8	CLK Y	CLK Y	P7, Y7
9	P0, Y0	N/C	P8, Y8
10	P1, Y1	P0, Y0	P9, Y9
11	P2, Y2	P1, Y1	P10, Y10
12	P3, Y3	P2, Y2	P11, Y11
13	P4, Y4	P3, Y3	P12, Y12
14	P5, Y5	P4, Y4	P13, Y13
15	P6, Y6	P5, Y5	P14, Y14
16	P7, Y7	P6, Y6	P15, Y15
17	P8, Y8	P7, Y7	N/C
18	P9, Y9	P8, Y8	P16
19	P10, Y10	P9, Y9	P17
20	P11, Y11	P10, Y10	P18
21	P12, Y12	P11, Y11	P19
22	P13, Y13	P12, Y12	P20
23	P14, Y14	P13, Y13	P21
24	P15, Y15	P14, Y14	P22
25	P16	P15, Y15	P23
26	P17	N/C	P24
27	P18	P16	P25
28	P19	P17	P26
29	P20	P18	P27
30	P21	P19	P28
31	P22	P20	P29
32	P23	P21	P30
33	P24	P22	P31
34	P25	P23	N/C

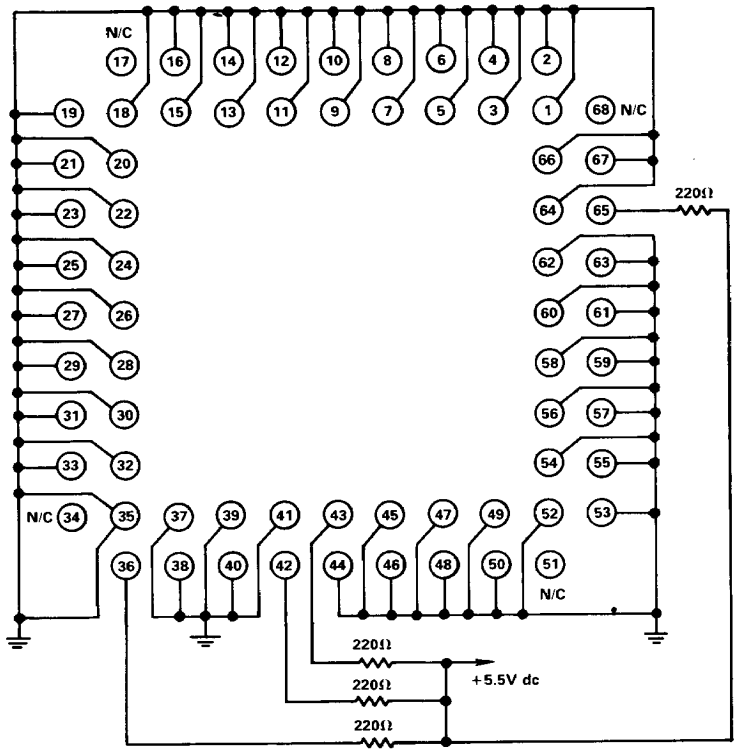
PIN NO.	FUNCTION		
	DIP	LCC	PIN-GRID
35	P26	P24	CLK M
36	P27	P25	TRIM
37	P28	P26	FA
38	P29	P27	FT
39	P30	P28	GND
40	P31	P29	GND
41	CLK M	P30	GND
42	TRIM	P31	V_{DD}
43	FA	N/C	V_{DD}
44	FT	CLK M	TCY
45	GND	TRIM	TCX
46	GND	FA	RND
47	GND	FT	CLK X
48	V_{DD}	GND	X15
49	V_{DD}	GND	X14
50	TCY	GND	X13
51	TCX	V_{DD}	N/C
52	RND	V_{DD}	X12
53	CLK X	TCY	X11
54	X15	TCX	X10
55	X14	RND	X9
56	X13	CLK X	X8
57	X12	X15	X7
58	X11	X14	X6
59	X10	X13	X5
60	X9	N/C	X4
61	X8	X12	X3
62	X7	X11	X2
63	X6	X10	X1
64	X5	X9	X0
65	N/A	X8	TRIL
66	N/A	X7	CLK L
67	N/A	X6	CLK Y
68	N/A	X5	N/C

3.2.4 Microcircuit Technology Group.

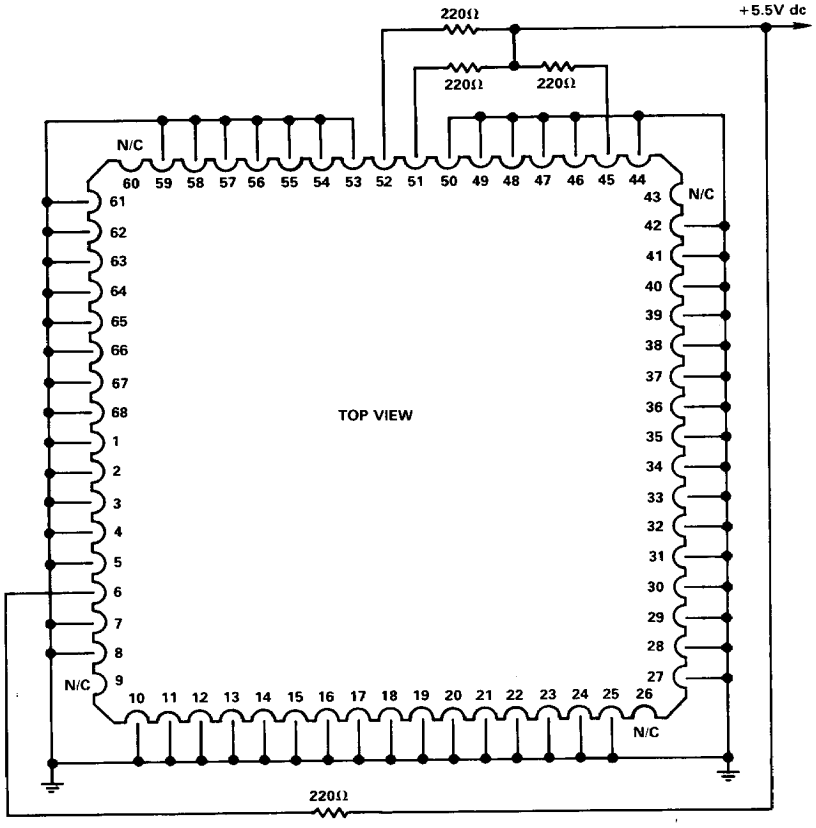
This microcircuit is covered by technology group (105).

4.2.1 Life Test/Burn-In Circuit.

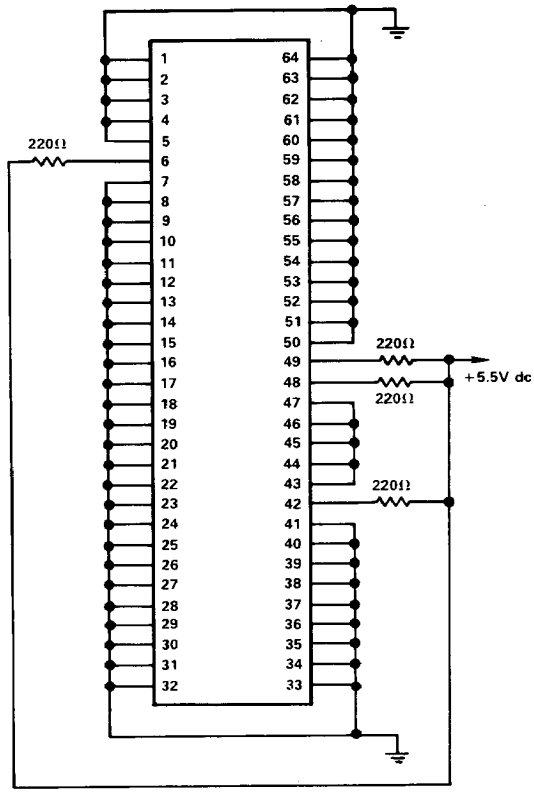
Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



ADSP-1016AG Life Test and Burn-In Circuit



ADSP-1016AE Life Test and Burn-In Circuit



ADSP-1016AD Life Test and Burn-In Circuit

REV. E

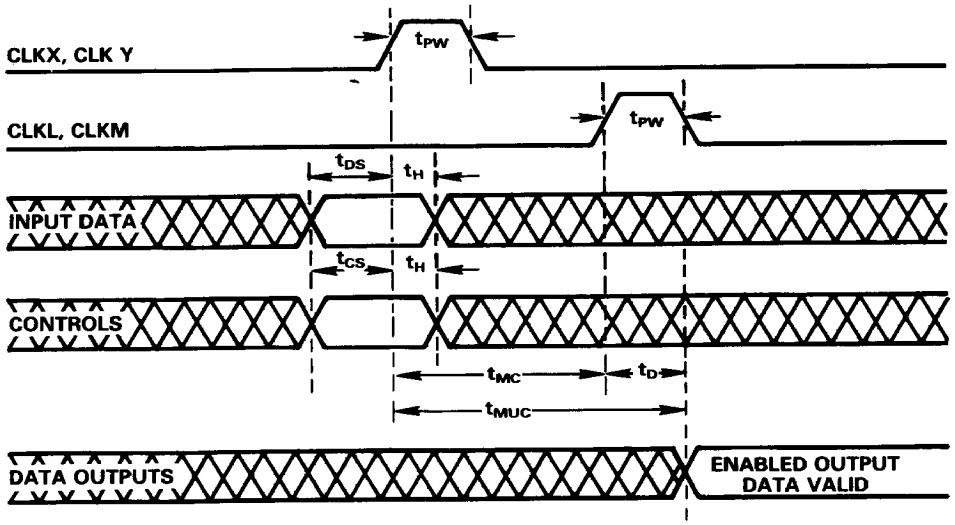


Figure 1. ADSP-1016A Timing Diagram

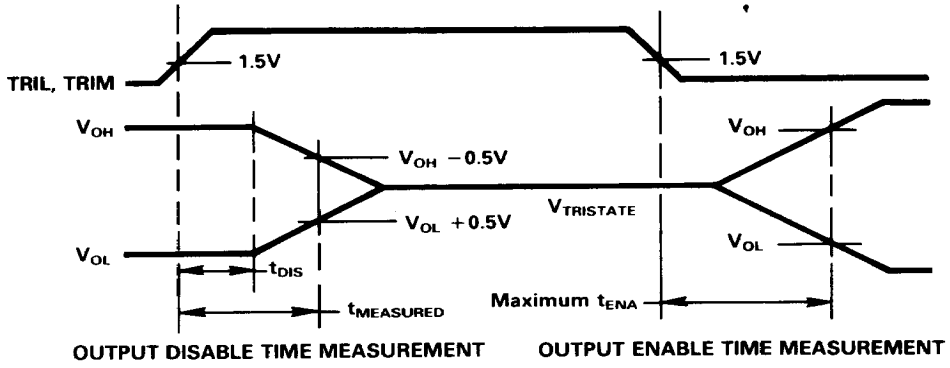


Figure 2. Three-State Disable and Enable Timing

Output disable time, t_{DIS}, is measured from the time the output enable control signal reaches 1.5 V to the time when all outputs have ceased driving. This is calculated by measuring the time, $t_{MEASURED}$, from the same starting point to when the output voltages have changed by 0.5 V toward +1.5 V. From the tester capacitive loading, C_L, and the measured current, i_L, the decay time, t_{DECAY}, can be approximated to first order by:

$$t_{DECAY} = \frac{C_L \cdot 0.5\ V}{i_L}$$

from which

$$t_{DIS} = t_{MEASURED} - t_{DECAY}$$

is calculated. Disable times are longest at the highest specified temperature.

The maximum output enable time, maximum t_{ENA}, is also measured from output enable control signal at 1.5 V to the time when all outputs have reached TTL input levels (V_{OH} or V_{OL}). This could also be considered as "data valid." Maximum enable times are longest at the highest specified temperature.

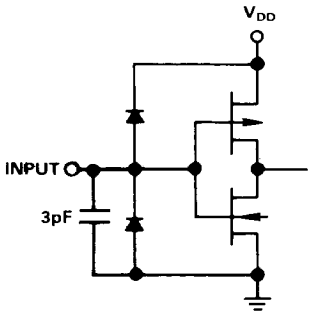


Figure 3. Equivalent Input Circuit

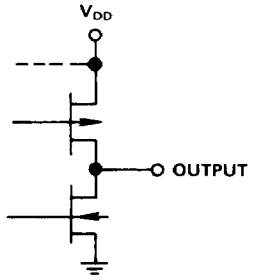


Figure 4. Equivalent Output Circuit

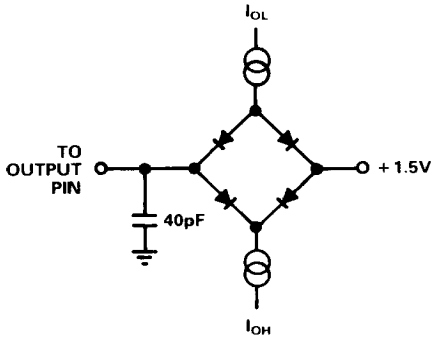


Figure 5. Normal Load Circuit for AC Measurements