1.1 Scope.

This specification covers the detail requirements for a monolithic CMOS 24×24-bit digital multiplier integrated circuit.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
−1	ADSP-1024ASG/883B
−2	ADSP-1024ATG/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline: G-84A.

1.3 Absolute Maximum Ratings.

Supply Voltage	−0.3 V to 7 V
Input Voltage	−0.3 V to V_{DD}
Output Voltage	−0.3 V to V_{DD}
Operating Temperature Range (Ambient)	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering 10 sec)	+300°C

1.5 Thermal Characteristics.

Maximum Thermal Resistance θ_{JC}: see MIL-M-38510, Appendix C.

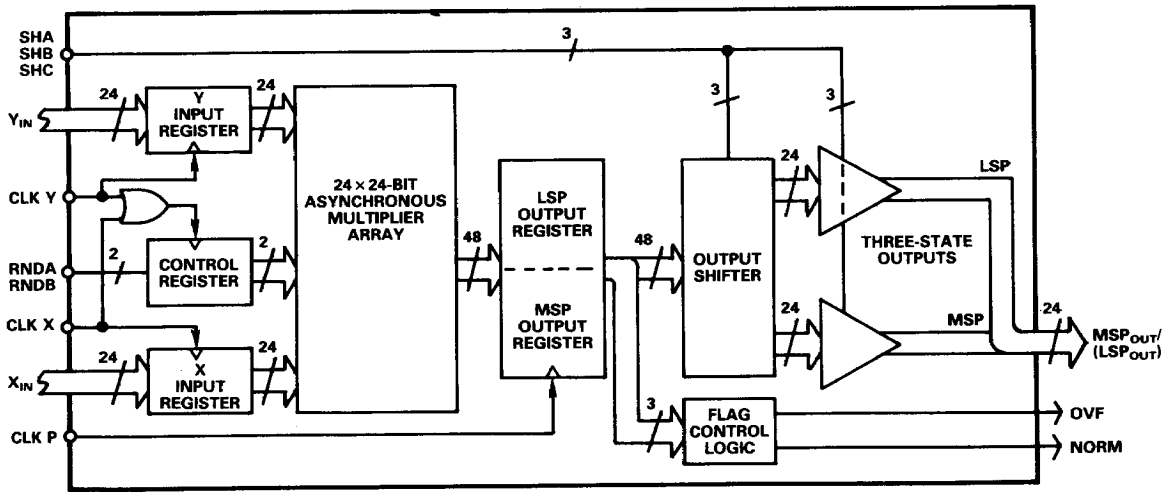
ADSP-1024A – SPECIFICATIONS

Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 9	Sub Group 10, 11	Test Condition[1]	Units
Digital Input High Voltage	V_{IH}	−1, 2	2.2	2.2	2.2			V_{DD} = max	V min
Digital Input Low Voltage	V_{IL}	−1, 2	0.8	0.8	0.8			V_{DD} = min	V max
Digital Output High Voltage	V_{OH}	−1, 2	2.4	2.4	2.4			V_{DD} = min I_{OH} = −4.0 mA	V min
Digital Output Low Voltage	V_{OL}	−1, 2	0.6	0.6	0.6			V_{DD} = min I_{OL} = +4.0 mA	V max
Digital Input High Current	I_{IH}	−1, 2	10	10	10			V_{DD} = max V_{IN} = +5.0 V	μA max
Digital Input Low Current	I_{IL}	−1, 2	10	10	10			V_{DD} = max V_{IN} = 0.0 V	μA max
Three-State Leakage Current Low	I_{OZL}	−1, 2	50	50	50			V_{DD} = max V_{IL} = 0 V (High Z)	μA max
Three-State Leakage Current High	I_{OZH}	−1, 2	50	50	50			V_{DD} = max V_{IH} = max (High Z)	μA max
Supply Current*	I_{DD1}	−1, 2	75	90	90			V_{DD} = max; TTL Inputs; f = max	mA max
	I_{DD2}	−1, 2	35	40	40			V_{DD} = max All V_{IN} = 2.4 V	mA max
Output Delay*	t_D	−1, 2	30			40	40	Note 2	ns max
Three-State Enable* (High Z to Low)	t_{ENA}	−1	35			40	40	Notes 2 and 3	ns max
		−2	30			35	35		
Three-State Disable* (Low to High Z)	t_{DIS}	−1	35			40	40	Notes 2 and 3	ns max
		−2	30			35	35		
Clock Pulse Width	t_{PW}	−1, 2	15			15	15	Note 2	ns min
Input Setup Time*	t_S	−1	30			35	35	Note 2	ns min
		−2	25			30	30		
Input Hold Time	t_H	−1, 2	3			3	3	Note 2	ns min
Clock to OVF Valid*	t_{DOVF}	−1	30			40	40	Note 2	ns max
		−2	25			35	35		
Clock to NORM Valid*	t_{DNRM}	−1	30			40	40	Note 2	ns max
		−2	25			35	35		
Clocked Multiply Time*	t_{MC}	−1	120			150	150	Note 2	ns max
		−2	95			120	120		

NOTES
*Indicates that a limit for this parameter has changed from REV. A.
[1]T_A = +25°C; V_{DD} = +4.5 V min to +5.5 V max (unless otherwise noted).
[2]TTL inputs of 0 V and +3.0 V; V_{DD} = +4.5 V, rise time = 5 ns, and timing transitions, per Figure 1, measured at +1.5 V (unless otherwise noted).
[3]Transitions measured per Figure 2.

Table 1.

3.2.1 Functional Block Diagrams and Terminal Assignments.



Pin Assignments

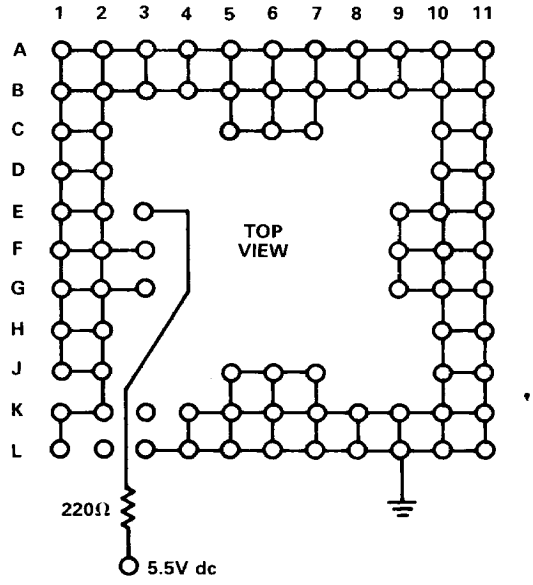
FUNCTION	PIN NO.	FUNCTION	PIN NO.
X20	C6	P16, P40	J6
X21	C5	P15, P39	L6
X22	A5	P14, P38	L7
X23	B5	P13, P37	K7
CLKX	A6	P12, P36	J7
CLKY	A4	P11, P35	L8
RNDB	B4	P10, P34	K8
RNDA	A3	P9, P33	L9
Y0	A2	P8, P32	L10
Y1	B3	P7, P31	K9
Y2	A1	P6, P30	L11
Y3	B2	P5, P29	K10
Y4	C2	P4, P28	J10
Y5	B1	P3, P27	K11
Y6	C1	P2, P26	J11
Y7	D2	P1, P25	H10
Y8	D1	P0, P24	H11
Y9	F2	SHA	G9
Y10	E2	SHB	G10
Y11	E1	SHC	G11
V_{DD}	E3	CLKP	F10
Y12	F3	GND	F9
Y13	F1	X0	E9
Y14	G1	X1	E11
Y15	G2	X2	E10
Y16	G3	X3	F11
Y17	H1	X4	D11
Y18	H2	X5	D10
Y19	J1	X6	C11
Y20	K1	X7	B11
Y21	J2	X8	C10
Y22	L1	X9	A11
Y23	K2	X10	B10
OVF	K3	X11	B9
NORM	L2	X12	A10
P23, P47	L3	X13	A9
P22, P46	K4	X14	B8
P21, P45	L4	X15	A8
P20, P44	K6	X16	C7
P19, P43	K5	X17	B7
P18, P42	L5	X18	A7
P17, P41	J5	X19	B6

3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (105).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



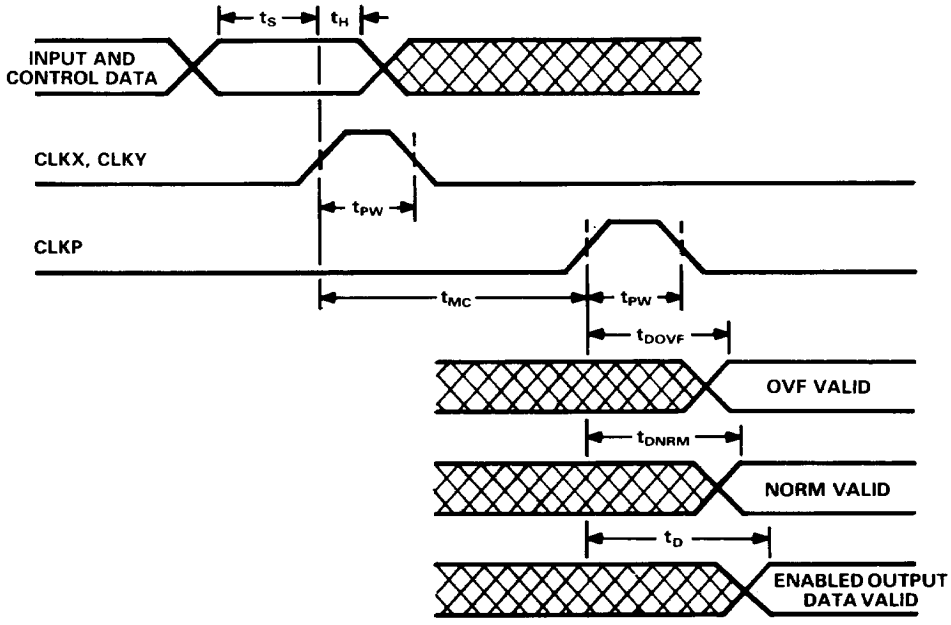


Figure 1. ADSP-1024A Timing Diagram

REV. B

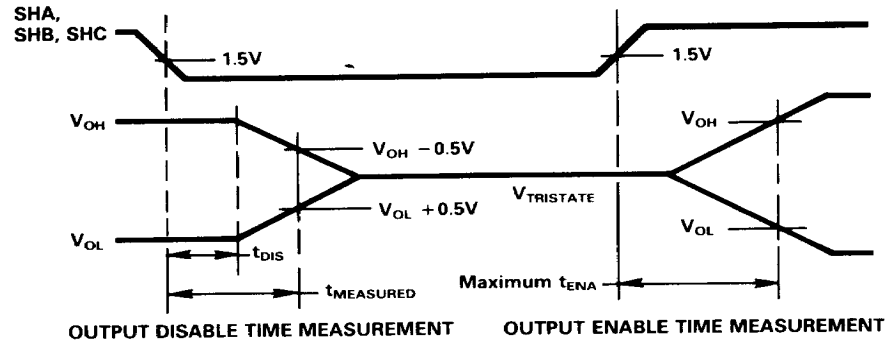


Figure 2. Three-State Disable and Enable Timing

Output disable time, t_{DIS}, is measured from the time the output enable control signal reaches 1.5 V to the time when all outputs have ceased driving. This is calculated by measuring the time, $t_{MEASURED}$, from the same starting point to when the output voltages have changed by 0.5 V toward +1.5 V. From the tester capacitive loading, C_L, and the measured current, i_L, the decay time, t_{DECAY}, can be approximated to first order by:

$$t_{DECAY} = \frac{C_L \cdot 0.5\ V}{i_L}$$

from which

$$t_{DIS} = t_{MEASURED} - t_{DECAY}$$

is calculated. Disable times are longest at the highest specified temperature.

The maximum output enable time, maximum t_{ENA}, is also measured from output enable control signal at 1.5 V to the time when all outputs have reached TTL input levels (V_{OH} or V_{OL}). This could also be considered as "data valid." Maximum enable times are longest at the highest specified temperature.

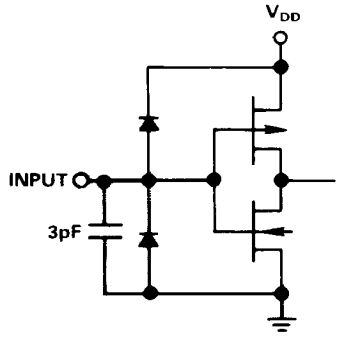


Figure 3. Equivalent Input Circuit

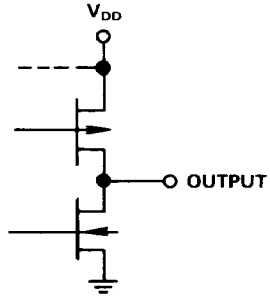


Figure 4. Equivalent Output Circuit

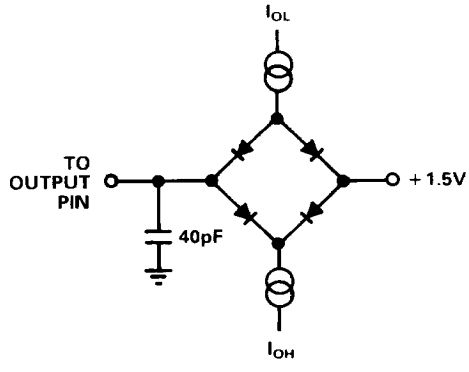


Figure 5. Normal Load Circuit for AC Measurements