

1.1 Scope.

This specification covers the requirements for a CMOS monolithic program sequencer.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
– 1	ADSP-1401SD/883B
– 2	ADSP-1401TD/883B

1.2.3 Case Outline.

See Appendix I of General Specification ADI-M-1000: package outline: D-48A.

1.3 Absolute Maximum Ratings.

Supply Voltage	– 0.3V to 7V
Input Voltage	– 0.3V to V_{DD}
Output Voltage	– 0.3V to V_{DD}
Operating Temperature Range (Ambient)	– 55°C to + 125°C
Storage Temperature Range	– 65°C to + 150°C
Lead Temperature (Soldering 10sec)	+ 300°C

1.5 Thermal Characteristics.

Thermal Resistance θ_{JC} : see MIL-M-38510, Appendix C.

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ADSP-1401 – SPECIFICATIONS

Parameter	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 9	Sub Group 10, 11	Test Condition ¹	Units
Digital Input High Voltage	V _{IH}	– 1, 2	2.0	2.0	2.0			V _{DD} = max	V min
Clock Input High Voltage	V _{IHC}	– 1, 2	3.0	3.0	3.0			V _{DD} = max	V min
Digital Input Low Voltage	V _{IL}	– 1, 2	0.8	0.8	0.8			V _{DD} = min	V max
Digital Output High Voltage	V _{OH}	– 1, 2	2.4	2.4	2.4			V _{DD} = min I _{OH} = – 1mA	V min
Digital Output Low Voltage	V _{OL}	– 1, 2	0.6	0.6	0.6			V _{DD} = min I _{OL} = +3mA	V max
Digital Input High Current	I _{IH}	– 1, 2	10	10	10			V _{DD} = max V _{IN} = +5.0V	μA max
Digital Input Low Current	I _{IL}	– 1, 2	10	10	10			V _{DD} = max V _{IN} = 0.0V	μA max
Three-State Leakage Current Low	I _{OZL}	– 1, 2	50	50	50			V _{DD} = max V _{IN} = 0V	μA max
Three-State Leakage Current High	I _{OZH}	– 1, 2	50	50	50			V _{DD} = max V _{IN} = max	μA max
Supply Current*	I _{DD1}	– 1, 2	90	115	115			V _{DD} = max; TTL Inputs; f = max	mA max
	I _{DD2}	– 1, 2	35	65	65			All V _{IN} = 2.4V	mA max
Clock HI*	t _{HI}	– 1	50			60	60	Note 2	ns min
		– 2	40			50	50	Note 2	ns min
Clock LO*	t _{LO}	– 1	40			50	50	Note 2	ns min
		– 2	30			40	40	Note 2	ns min
Instruction Setup Time*	t _{IS}	– 1	36			45	45	Note 2	ns min
		– 2	30			40	40	Note 2	ns min
Data Setup Time*	t _{DS}	– 1, 2	10			15	15	Note 2	ns min
Input Signal Hold Time	t _{IH}	– 1, 2	3			3	3	Note 2	ns min
Address Delay* ³	t _{AD}	– 1	35			45	45	Note 2, C = 50pF	ns max
		– 2	25			35	35	Note 2, C = 50pF	ns max
Address Hold Time*	t _{AH}	– 1, 2	3			1	1	Note 2	ns min
Output Data Delay*	t _{ODD}	– 1	50			60	60	Note 2, C = 30pF	ns max
		– 2	35			45	45	Note 2, C = 30pF	ns max
Output Data Disable Time*	t _{ODIS}	– 1	20			25	25	Note 2	ns max
		– 2	15			20	20	Note 2	ns max
Input Flag Setup Time (IR0 Masked)	t _{IFSM}	– 1	15			20	20	Note 2, IR0 Masked	ns min
		– 2	10			15	15	Note 2, IR0 Masked	ns min
Input Flag Setup Time* (No Constraints)	t _{IFSU}	– 1	30			35	35	Note 2	ns min
		– 2	26			30	30		

Table 1. (Continued on next page)

REV. B

Parameter	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 9	Sub Group 10, 11	Test Condition ¹	Units
Upper Interrupts Setup Time* (IR8-5)	t_{UIRS}	- 1	30			35	35	Note 2	ns min
		- 2	25			30	30		
Lower Interrupts Setup Time* (IR4-1)	t_{LIRS}	- 1	20			25	25	Note 2	ns min
		- 2	15			20	20		
Three-State (TTR) Setup Time*	t_{TSS}	- 1, 2	10			15	15	Note 2	ns min
Three-State (TTR) Overlap Time (with Trap)*	t_{TSOV}	- 1, 2	15			5	5	Note 2	ns max
Three-State (TTR) Disable Delay*	t_{TSE}	- 1	20			25	25	Notes 2, 4	ns max
		- 2	15			20	20		
Idle-to-Three-State Enable Delay*	t_{IDL3}	- 1	20			25	25	Notes 2, 4	ns max
		- 2	15			20	20		
Trap (TTR) Overlap Time (with Three-State)	t_{TROV}	- 1, 2	10			10	10	Notes 2, 4	ns max
Trap (TTR) to Address Delay*	t_{TRAD}	- 1	60			70	70	Notes 2, 4	ns max
		- 2	45			55	55		

NOTES

*Indicates that a limit for this parameter has changed from REV. A.

¹ $T_A = +25^\circ\text{C}$; $V_{DD} = +4.5\text{V min to } +5.5\text{V max}$ (unless otherwise noted).

²Input levels are GND and +3.0V; $V_{DD} = +4.5\text{V}$. Rise times are 5ns. Input timing reference levels and output reference levels are measured at +1.5V except for three-state reference levels, which are shown in Figure 2.

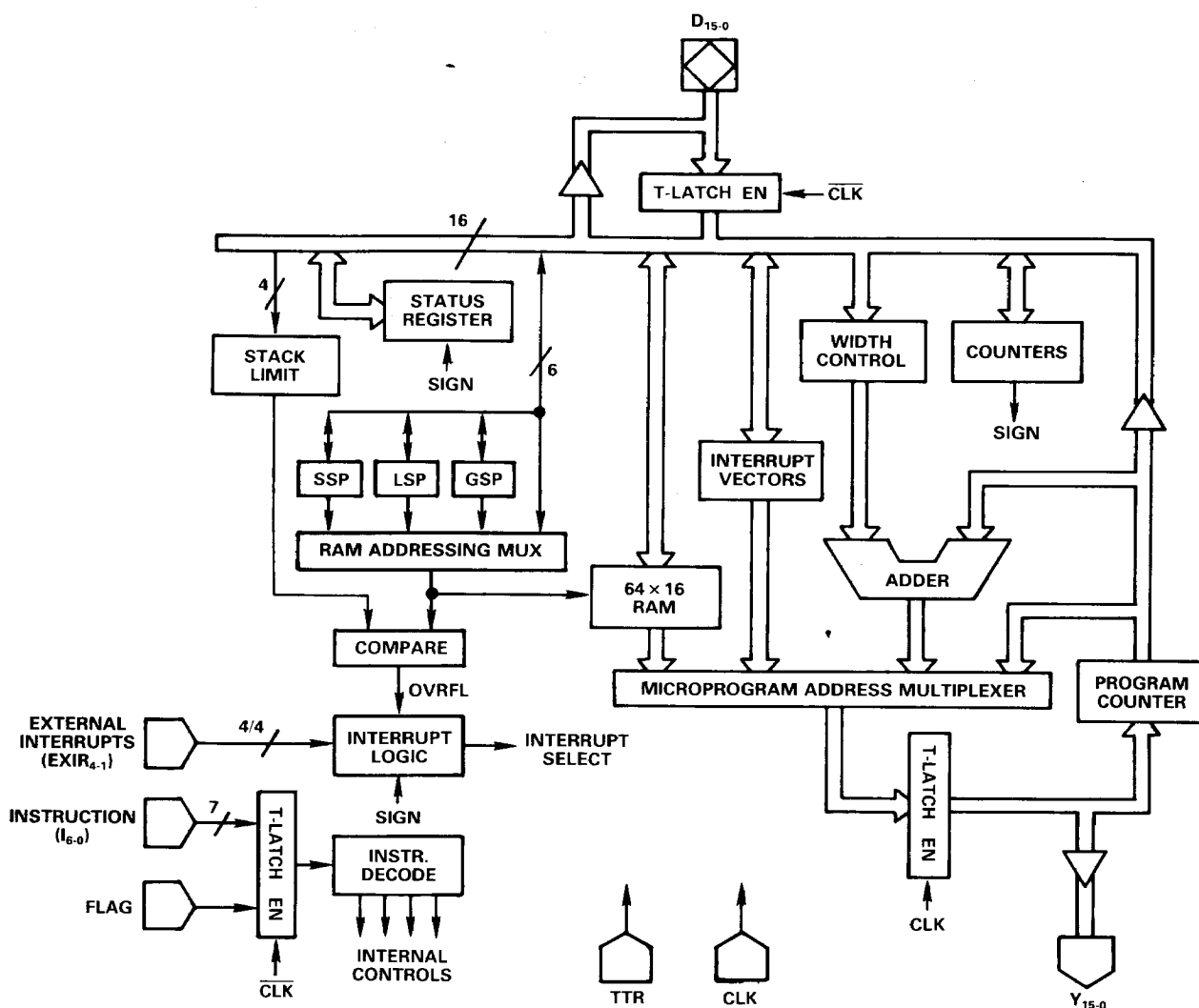
³Transitions measured per Figure 2.

⁴Address delays may be derated from the specified 50pF test loading by adding 7ns/50pF for increased capacitive loading.

Table 1.

ADSP-1401

3.2.1 Functional Block Diagram and Terminal Assignments.



Pin Assignments

PIN	FUNCTION	PIN	FUNCTION
1	D7	25	Y6
2	D8	26	Y5
3	D9	27	Y4
4	D10	28	Y3
5	D11	29	Y2
6	D12	30	Y1
7	D13	31	Y0
8	D14	32	I0
9	D15	33	I1
10	EXIR1	34	I2
11	EXIR2	35	I3
12	GND	36	I4
13	EXIR3	37	V _{DD}
14	EXIR4	38	I5
15	TTR	39	I6
16	Y15	40	FLAG
16	Y14	41	CLK
18	Y13	42	D0
19	Y12	43	D1
20	Y11	44	D2
21	Y10	45	D3
22	Y9	46	D4
23	Y8	47	D5
24	Y7	48	D6

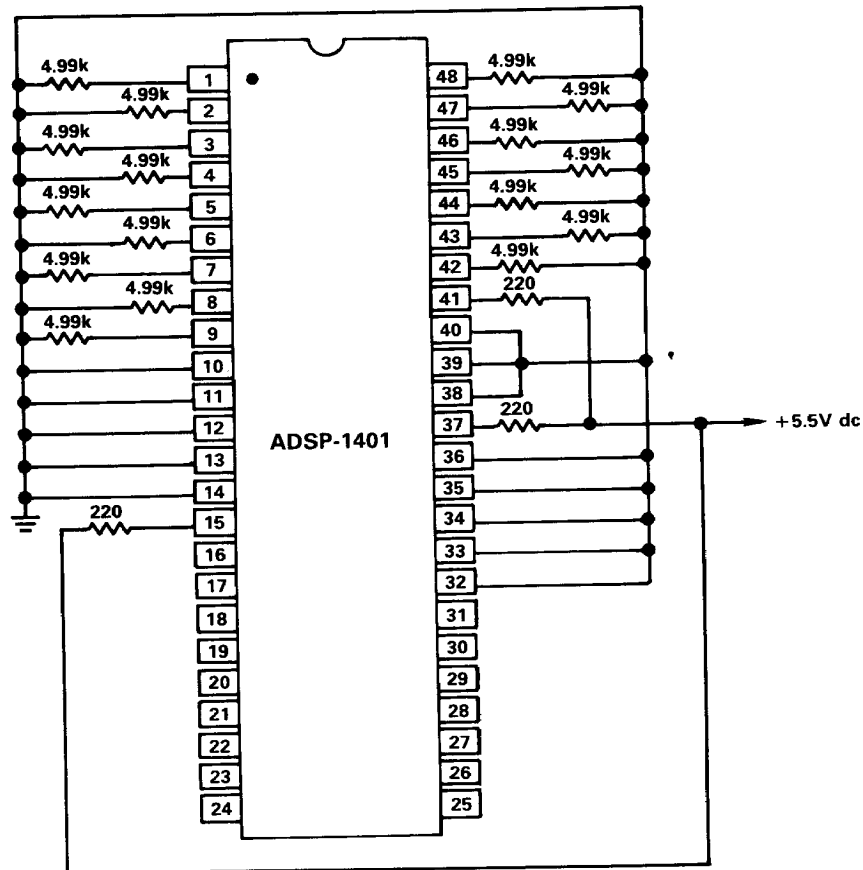
REV. B

3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (105).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



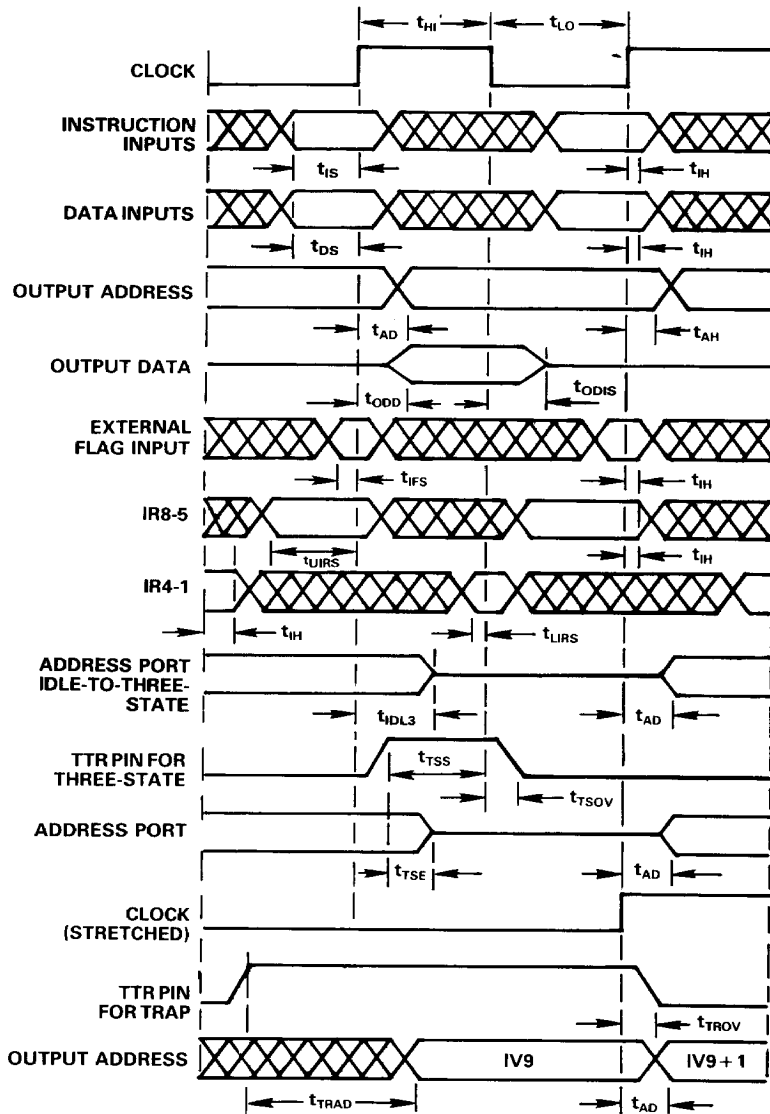


Figure 1. ADSP-1401 Timing Diagram

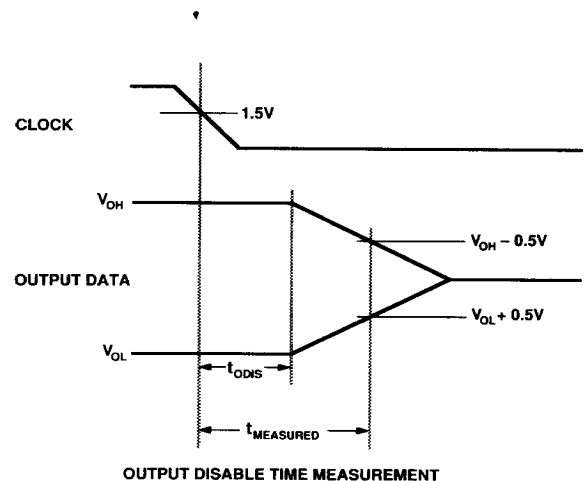


Figure 2. Three-State Reference Levels

Output disable time is measured from the time CLK reaches 1.5V to the time when all outputs have ceased driving. This is calculated by measuring the time, t_{MEASURED} , from the same starting point to when the output voltages have changed by 0.5V toward +1.5V. From the tester capacitive loading, C_L , and the measured current, i_L , the decay time, t_{DECAY} , can be approximated to first order by:

$$t_{\text{DECAY}} = \frac{C_L \cdot 0.5V}{i_L}$$

from which

$$t_{\text{ODIS}} = t_{\text{MEASURED}} - t_{\text{DECAY}}$$

is calculated. Disable times are longest at the highest specified temperature.

Mnemonic	Opcode (I ₄₋₀)	Description		
Jump and Branch Instructions:			Status Register Operations:	
JPCOF	001 0101	IF FLAG: JUMP PC (<i>self</i>)	RDSR	010 1110 READ SR
JPCNF	011 0101	IF NOT FLAG: JUMP PC (<i>self</i>)	WRSR	001 1100 WRITE SR
JTWO	101 cc01	IF COND: JUMP PC+2 (<i>skip</i>)	PSSR	010 0001 PUSH SR ONTO SS
JDA	111 cc11	IF COND: JUMP DATA, ABSOLUTE	PPSR	010 0010 POP SR FROM SS
JDR	111 cc01	IF COND: JUMP DATA, RELATIVE	Counter Operations:	
JDI	101 cc10	IF COND: JUMP DATA, INDIRECT	WRCNTR	011 10i i WRITE C _i
JDRST	100 11i i	IF SIGN OF C _i : JUMP DATA, C _i <= R _i ; ELSE, C _i <= C _i - 1	CLRS	001 0100 CLEAR SIGN BIT
*JRC	110 cci i	IF COND: JUMP R _i	SETS	011 0100 SET SIGN BIT
JRS	110 11i i	IF SIGN OF C _i : JUMP R _i , C _i <= C _i - 1	PSCNTR	000 10i i PUSH C _i ONTO SS
JSA	111 cc00	IF COND: JUMP SUB, ABSOLUTE	PPCNTR	001 10i i POP C _i FROM SS
JSR	111 cc10	IF COND: JUMP SUB, RELATIVE	DCCNTR	011 00i i DECREMENT C _i
RTN	101 cc11	IF COND: RETURN FROM SUB	IFCDEC	101 cc00 IF COND: DECREMENT C ₀
*BRANCH	100 cci i	IF SIGN OF C _i : JUMP R _i ; ELSE, C _i <= C _i - 1, IF COND: JUMP DATA	Interrupt Control:	
Stack Operations:			CCIR	001 0001 CLEAR CURRENT INTERRUPT
<i>Subroutine Stack</i>			CAIR	000 0001 CLEAR ALL INTERRUPTS
PSDSS	001 1110	PUSH DATA ONTO SS	RTNIR	000 0011 RETURN FROM INTERRUPT
PPSSD	011 1110	POP SS TO DATA PORT	RDIV	010 1101 READ INTERRUPT VECTOR
WRSSP	000 1110	WRITE SSP	WRIV	000 1101 WRITE INTERRUPT VECTOR AND INCREMENT IVP
RDSSP	010 1100	READ SSP	IRMB	001 0011 IR MASK BITWISE CLEAR
DSSP	000 0010	DECREMENT SSP	IRMS	001 0010 IR MASK BITWISE SET
<i>Register Stack</i>			DISIR	001 0110 DISABLE INTERRUPTS
SGSP	000 0111	SELECT GSP	ENAIR	011 0110 ENABLE INTERRUPTS
SLSP	000 0110	SELECT LSP	SLIR	001 0111 SELECT LATCHED INTERRUPTS
RDRSP	010 1111	READ RSP	STIR	011 0111 SELECT TRANSPARENT INTERRUPTS
WRRSP	000 1100	WRITE RSP	SLRIVP	001 1101 WRITE SLR <= D ₅₋₂ AND IVP <= D ₁₅₋₁₂
PSPC	010 0011	PUSH PC ONTO RS	Relative Address Width Controls:	
PSGSP	000 0101	PUSH GSP ONTO SS	REL16	010 0100 SELECT 16-BIT RELATIVE ADDRESSING
PPGSP	000 0100	POP GSP FROM SS	REL12	010 0111 SELECT 12-BIT RELATIVE ADDRESSING
PSDRS	001 1111	PUSH DATA ONTO RS	REL8	010 0110 SELECT 8-BIT RELATIVE ADDRESSING
PPRSD	011 1111	POP RS TO DATA PORT	Miscellaneous Instructions:	
AIRSP	010 10i i	ADD i TO RSP	CONT	000 0000 CONTINUE
SIRSP	000 1111	SUBTRACT 1 FROM RSP	IDLE	001 0000 IDLE
S4RSP	011 1100	SUBTRACT 4 FROM RSP	IHC	010 0101 ENABLE INSTRUCTION HOLD CONTROL
			WCS	010 0000 WRITE CONTROL STORE

The SIGN condition is precluded from instructions prefixed with “*.”

Table 2. ADSP-1401 Instruction Set

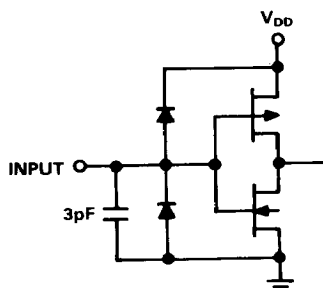


Figure 3. Equivalent Input Circuit

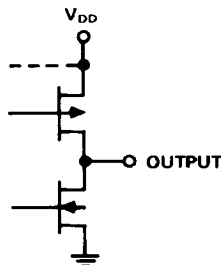


Figure 4. Equivalent Output Circuit

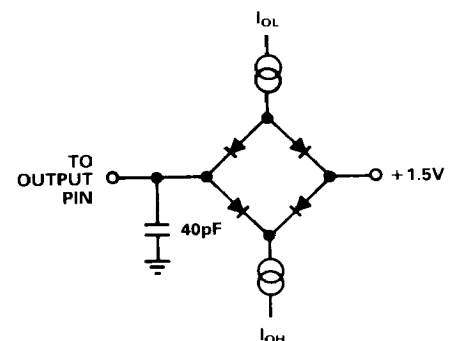


Figure 5. Normal Load for AC Measurements

REV. B