ANALOG DEVICES

BLACKfin™ Embedded Processor

Preliminary Technical Data ADSP-21532

FEATURES

300 MHz High-Performance MSA DSP Core
- **Two 16-Bit MACs, Two 40-Bit ALUs, Four 8-Bit Video ALUs, 40-Bit Shifter**
- **RISC-Like Register and Instruction Model for Ease of Programming and Compiler-Friendly Support**
- **Advanced Debug, Trace, and Performance- Monitoring Support**

On-chip Voltage Regulation from 2.25 V to 3.6 V Input
3.3 V-Tolerant I/O
-40 °C to 105 °C Case Temperature Range
160-Lead Mini-BGA Package

MEMORY

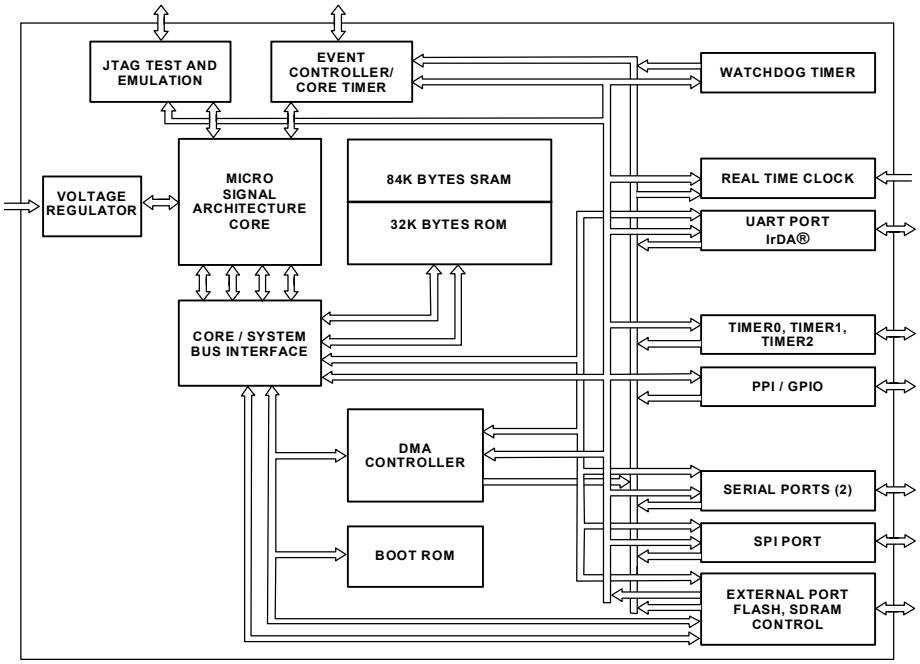
116K Bytes of On-Chip Memory:
- **16K Bytes of Instruction SRAM/Cache**
- **32K Bytes of Instruction SRAM**
- **32K Bytes of Instruction ROM**
- **32K Bytes of Data SRAM/Cache**
- **4K Bytes of Scratchpad SRAM**

Two Dual-Channel Memory DMA Controllers
Memory Management Unit Providing Memory Protection
External Memory Controller with Glueless Support for SDRAM, SRAM, FLASH, and ROM
Flexible Memory Booting Options From SPI, External Memory, or Internal ROM

PERIPHERALS

Parallel Peripheral Interface (PPI)/GPIO, Supporting ITU-R 656 Video Data Formats
Two Dual-Channel, Full-Duplex Synchronous Serial Ports, Supporting Eight Stereo I^2S Channels
12 Channel DMA Controller
SPI-compatible Port
Three Timer/Counters with PWM Support
UART with Support for IrDA®
Event Handler
Real-Time Clock
Watchdog Timer
Debug/JTAG Interface
On-Chip PLL Capable of 1x To 31x Frequency Multiplication

FUNCTIONAL BLOCK DIAGRAM



REV. PrD

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General Note
This data sheet provides preliminary information for the ADSP-21532 Blackfin™ processor[1].

GENERAL DESCRIPTION

The ADSP-21532 is a member of the Blackfin family of products, incorporating the Analog Devices/Intel Micro Signal Architecture (MSA). Blackfin processors combine a dual-MAC state-of-the-art DSP (Digital Signal Processor) engine, the advantages of a clean, orthogonal RISC-like microprocessor instruction set, and single-instruction, multiple-data (SIMD) multimedia capabilities into a single instruction-set architecture.

By integrating a rich set of industry-leading system peripherals and memory, Blackfin processors are the platform of choice for next-generation applications that require RISC-like programmability, multimedia support and leading-edge signal processing in one integrated package.

Portable Low-Power Architecture

Blackfin processors provide world-class power management and performance. Blackfin processors are designed in a low power and low voltage design methodology and feature Dynamic Power Management, the ability to vary both the voltage and frequency of operation to significantly lower overall power consumption. Varying the voltage and frequency can result in a substantial reduction in power consumption, compared with just varying the frequency of operation. This translates into longer battery life for portable appliances.

System Integration

The ADSP-21532 is a highly integrated system-on-a-chip solution for the next generation of digital communication and portable Internet appliances. By combining industry-standard interfaces with a high performance Digital Signal Processing core, users can develop cost-effective solutions quickly without the need for costly external components. The ADSP-21532 system peripherals include a UART port, an SPI port, two serial ports (SPORTs), four general purpose timers (three with PWM capability), a real-time clock, a watchdog timer, and a Parallel Peripheral Interface.

ADSP-21532 Peripherals

The ADSP-21532 contains a rich set of peripherals connected to the core via several high bandwidth buses, providing flexibility in system configuration as well as excellent overall system performance (see the block diagram on page 1). The general-purpose peripherals include functions such as UART, Timers with PWM (Pulse Width Modulation) and pulse measurement capability, general purpose flag I/O pins, a Real-Time Clock, and a Watchdog Timer. This set of functions satisfies a wide variety of typical system support needs and is augmented by the system expansion capabilities of the part. In addition to these general-purpose peripherals, the ADSP-21532 contains high-speed serial and parallel ports for interfacing to a variety of audio, video, and modem codec functions; an interrupt controller for flexible management of interrupts from the on-chip peripherals or external sources; and power management control functions to tailor the performance and power characteristics of the processor and system to many application scenarios.

All of the peripherals, except for general-purpose I/O, Real-Time Clock, and timers, are supported by a flexible DMA structure. There is also a separate memory DMA channel dedicated to data transfers between the DSP's various memory spaces, including external SDRAM and asynchronous memory. Multiple on-chip buses running at up to 133 MHz provide enough bandwidth to keep the processor core running along with activity on all of the on-chip and external peripherals.

The ADSP-21532 includes an on-chip voltage regulator in support of the Blackfin processor Dynamic Power Management capability. The voltage regulator provides a range of core voltage levels from a single 2.25 V to 3.6 V input. The voltage regulator can be bypassed at the user's discretion.

MSA DSP Core

As shown in Figure 1 on page 3, the MSA DSP core contains two 16-bit multipliers, two 40-bit accumulators, two 40-bit ALUs, four video ALUs, and a 40-bit shifter. The computation units process 8-bit, 16-bit, or 32-bit data from the register file.

The compute register file contains eight 32-bit registers. When performing compute operations on 16-bit operand data, the register file operates as 16 independent 16-bit registers. All operands for compute operations come from the multiported register file and instruction constant fields.

Each MAC can perform a 16-bit by 16-bit multiply in each cycle, accumulating the results into the 40-bit accumulators. Signed and unsigned formats, rounding, and saturation are supported.

The ALUs perform a traditional set of arithmetic and logical operations on 16-bit or 32-bit data. In addition, many special instructions are included to accelerate various signal processing tasks. These include bit operations such as field extract and population count, modulo 2^{32} multiply, divide primitives, saturation and rounding, and sign/exponent detection. The set of video instructions include byte alignment and packing operations, 16-bit and 8-bit adds with clipping, 8-bit average operations, and 8-bit subtract/absolute value/accumulate (SAA) operations. Also provided are the compare/select and vector search instructions.

For certain instructions, two 16-bit ALU operations can be performed simultaneously on register pairs (a 16-bit high half and 16-bit low half of a compute register). By also using the second ALU, quad 16-bit operations are possible.

[1] Blackfin is a trademark of Analog Devices, Inc.

The 40-bit shifter can perform shifts and rotates and is used to support normalization, field extract, and field deposit instructions.

The program sequencer controls the flow of instruction execution, including instruction alignment and decoding. For program flow control, the sequencer supports PC relative and indirect conditional jumps (with static branch prediction), and subroutine calls. Hardware is provided to support zero-overhead looping. The architecture is fully interlocked, meaning that the programmer need not manage the pipeline when executing instructions with data dependencies.

The address arithmetic unit provides two addresses for simultaneous dual fetches from memory. It contains a multiported register file consisting of four sets of 32-bit Index, Modify, Length, and Base registers (for circular buffering), and eight additional 32-bit pointer registers (for C-style indexed stack manipulation).

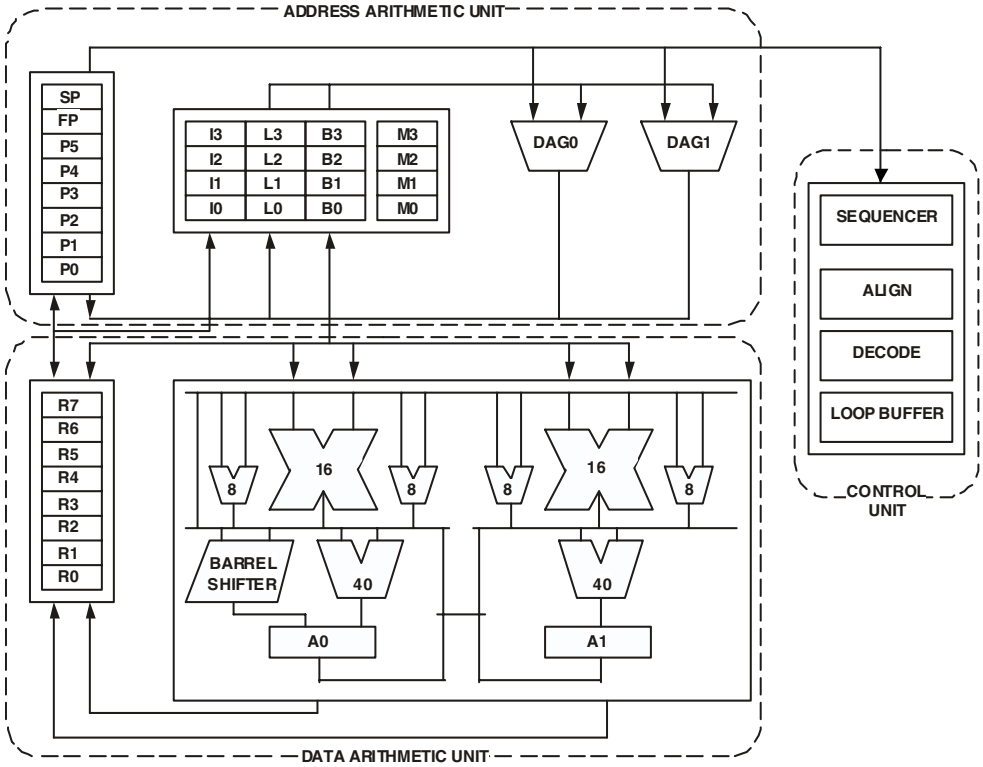


Figure 1. MSA DSP Core

Blackfin processors support a modified Harvard architecture in combination with a hierarchical memory structure. Level 1 (L1) memories are those that typically operate at the full processor speed with little or no latency. At the L1 level, the instruction memory holds instructions only. The two data memories hold data, and a dedicated scratchpad data memory stores stack and local variable information.

In addition, multiple L1 memory blocks are provided, offering a configurable mix of SRAM and cache. The Memory Management Unit (MMU) provides memory protection for individual tasks that may be operating on the core and can protect system registers from unintended access.

The architecture provides three modes of operation: User mode, Supervisor mode, and Emulation mode. User mode has restricted access to certain system resources, thus providing a protected software environment, while Supervisor mode has unrestricted access to the system and core resources.

The Blackfin processor instruction set has been optimized so that 16-bit opcodes represent the most frequently used instructions, resulting in excellent compiled code density. Complex DSP instructions are encoded into 32-bit opcodes, representing fully featured multifunction instructions. Blackfin processors support a limited multi-issue capability, where a 32-bit instruction can be issued in parallel with two 16-bit instructions, allowing the programmer to use many of the core resources in a single instruction cycle.

The Blackfin processor assembly language uses an algebraic syntax for ease of coding and readability. The architecture has been optimized for use in conjunction with the C/C++ compiler, resulting in fast and efficient software implementations.

Memory Architecture

The ADSP-21532 views memory as a single unified 4G byte address space, using 32-bit addresses. All resources, including internal memory, external memory, and I/O control registers, occupy separate sections of this common address space. The memory portions of this address space are arranged in a hierarchical structure to provide a good cost/performance balance of some very fast, low-latency on-chip memory as cache or SRAM, and larger, lower-cost and performance off-chip memory systems. See Figure 2.

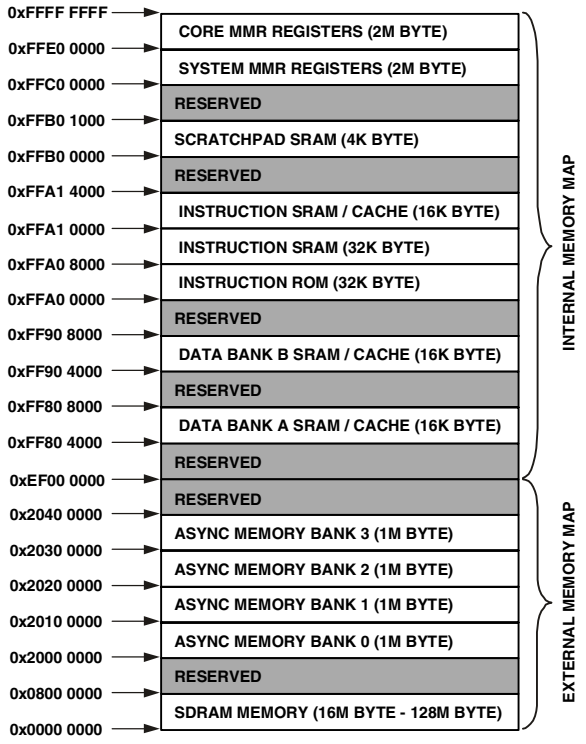


Figure 2. Internal/External Memory Map

The L1 memory system is the primary highest-performance memory available to the Blackfin processor. The off-chip memory system, accessed through the External Bus Interface Unit (EBIU), provides expansion with SDRAM, flash memory, and SRAM, optionally accessing up to 132M bytes of physical memory.

The memory DMA controller provides high-bandwidth data-movement capability. It can perform block transfers of code or data between the internal memory and the external memory spaces.

Internal (On-chip) Memory

The ADSP-21532 has three blocks of on-chip memory providing high-bandwidth access to the core.

The first is the L1 instruction memory, consisting of 48K bytes SRAM, of which 16K bytes can be configured as a four-way set-associative cache. The first memory block also includes 32K bytes of user-definable ROM. This memory is accessed at full processor speed.

The second on-chip memory block is the L1 data memory, consisting of two banks of 16K bytes each. Each L1 data memory bank can be configured as 16K bytes SRAM or as 16K bytes two-way set-associative cache. This memory block is accessed at full processor speed.

The third memory block is a 4K byte scratchpad SRAM which runs at the same speed as the L1 memories, but is only accessible as data SRAM and cannot be configured as cache memory.

External (Off-Chip) Memory

External memory is accessed via the EBIU. This 16-bit interface provides a glueless connection to a bank of synchronous DRAM (SDRAM) as well as up to four banks of asynchronous memory devices including FLASH, EPROM, ROM, SRAM, and memory mapped I/O devices.

The PC133-compliant SDRAM controller can be programmed to interface to up to 128M bytes of SDRAM.

The asynchronous memory controller can be programmed to control up to four banks of devices with very flexible timing parameters for a wide variety of devices. Each bank occupies a 1M byte segment regardless of the size of the devices used, so that these banks will only be contiguous if each is fully populated with 1M byte of memory.

I/O Memory Space

Blackfin processors do not define a separate I/O space. All resources are mapped through the flat 32-bit address space. On-chip I/O devices have their control registers mapped into memory-mapped registers (MMRs) at addresses near the top of the 4G byte address space. These are separated into two smaller blocks, one which contains the control MMRs for all core functions, and the other which contains the registers needed for setup and control of the on-chip peripherals outside of the core. The MMRs are accessible only in supervisor mode and appear as reserved space to on-chip peripherals.

Booting

The ADSP-21532 contains a small boot kernel, which configures the appropriate peripheral for booting. If the ADSP-21532 is configured to boot from boot ROM memory space, the DSP starts executing from the on-chip boot ROM. For more information, see Booting Modes on page 12.

Event Handling

The event controller on the ADSP-21532 handles all asynchronous and synchronous events to the processor. The ADSP-21532 provides event handling that supports both nesting and prioritization. Nesting allows multiple event service routines to be active simultaneously. Prioritization ensures that servicing of a higher-priority event takes precedence over servicing of a lower-priority event. The controller provides support for five different types of events:

- Emulation – An emulation event causes the processor to enter emulation mode, allowing command and control of the processor via the JTAG interface.
- Reset – This event resets the processor.
- Non-Maskable Interrupt (NMI) – The NMI event can be generated by the software watchdog timer or by the NMI input signal to the processor. The NMI event is frequently used as a power-down indicator to initiate an orderly shutdown of the system.
- Exceptions – Events that occur synchronously to program flow (i.e., the exception will be taken before the instruction is allowed to complete). Conditions such as data alignment violations and undefined instructions cause exceptions.
- Interrupts – Events that occur asynchronously to program flow. They are caused by input pins, timers, and other peripherals, as well as by an explicit software instruction.

Each event type has an associated register to hold the return address and an associated return-from-event instruction. When an event is triggered, the state of the processor is saved on the supervisor stack.

The ADSP-21532 Event Controller consists of two stages, the Core Event Controller (CEC) and the System Interrupt Controller (SIC). The Core Event Controller works with the System Interrupt Controller to prioritize and control all system events. Conceptually, interrupts from the peripherals enter into the SIC, and are then routed directly into the general-purpose interrupts of the CEC.

Core Event Controller (CEC)

The CEC supports nine general-purpose interrupts (IVG15–7), in addition to the dedicated interrupt and exception events. Of these general-purpose interrupts, the two lowest-priority interrupts (IVG15–14) are recommended to be reserved for software interrupt handlers, leaving seven prioritized interrupt inputs to support the peripherals of the ADSP-21532. Table 1 describes the inputs to the CEC, identifies their names in the Event Vector Table (EVT), and lists their priorities.

Table 1. Core Event Controller (CEC)

Priority (0 is Highest)	Event Class	EVT Entry
0	Emulation/Test Control	EMU
1	Reset	RST
2	Non-Maskable Interrupt	NMI
3	Exception	EVX
4	Reserved	-
5	Hardware Error	IVHW
6	Core Timer	IVTMR
7	General Interrupt 7	IVG7
8	General Interrupt 8	IVG8
9	General Interrupt 9	IVG9
10	General Interrupt 10	IVG10
11	General Interrupt 11	IVG11
12	General Interrupt 12	IVG12
13	General Interrupt 13	IVG13
14	General Interrupt 14	IVG14
15	General Interrupt 15	IVG15

System Interrupt Controller (SIC)

The System Interrupt Controller provides the mapping and routing of events from the many peripheral interrupt sources to the prioritized general-purpose interrupt inputs of the CEC. Although the ADSP-21532 provides a default mapping, the user can alter the mappings and priorities of interrupt events by writing the appropriate values into the

Interrupt Assignment Registers (IAR). Table 2 describes the inputs into the SIC and the default mappings into the CEC.

Table 2. System Interrupt Controller (SIC)

Peripheral Interrupt Event	Default Mapping
PLL Wakeup	IVG7
DMA Error	IVG7
PPI Error	IVG7
SPORT 0 Error	IVG7
SPORT 1 Error	IVG7
SPI Error	IVG7
UART Error	IVG7
Real-Time Clock	IVG8
DMA Channel 0 (PPI)	IVG8
DMA Channel 1 (SPORT 0 RX)	IVG9
DMA Channel 2 (SPORT 0 TX)	IVG9
DMA Channel 3 (SPORT 1 RX)	IVG9
DMA Channel 4 (SPORT 1 TX)	IVG9
DMA Channel 5 (SPI)	IVG10
DMA Channel 6 (UART RX)	IVG10
DMA Channel 7 (UART TX)	IVG10
Timer 0	IVG11
Timer 1	IVG11
Timer 2	IVG11
PF Interrupt A	IVG12
PF Interrupt B	IVG12
DMA Channels 8 and 9 (Memory DMA Stream 1)	IVG13
DMA Channels 10 and 11 (Memory DMA Stream 0)	IVG13
Software Watchdog Timer	IVG13

Event Control

The ADSP-21532 provides the user with a very flexible mechanism to control the processing of events. In the CEC, three registers are used to coordinate and control events. Each register is 16 bits wide:

- CEC Interrupt Latch Register (ILAT) – The ILAT register indicates when events have been latched. The appropriate bit is set when the processor has latched the event and cleared when the event has been accepted into the system. This register is updated automatically by the controller, but it may be written only when its corresponding IMASK bit is cleared.
- CEC Interrupt Mask Register (IMASK) – The IMASK register controls the masking and unmasking of individual events. When a bit is set in the IMASK register, that event is unmasked and will be processed by the CEC when asserted. A cleared bit in the IMASK register masks the event, preventing the processor from servicing the event even though the event may be latched in the ILAT register. This register may be read or written while in supervisor mode. (Note that general-purpose interrupts can be globally enabled and disabled with the STI and CLI instructions, respectively.)
- CEC Interrupt Pending Register (IPEND) – The IPEND register keeps track of all nested events. A set bit in the IPEND register indicates the event is currently active or nested at some level. This register is updated automatically by the controller but may be read while in supervisor mode.

The SIC allows further control of event processing by providing three 32-bit interrupt control and status registers. Each register contains a bit corresponding to each of the peripheral interrupt events shown in Table 2 on page 6.

- SIC Interrupt Mask Register (SIC_IMASK)– This register controls the masking and unmasking of each peripheral interrupt event. When a bit is set in the register, that peripheral event is unmasked and will be processed by the system when asserted. A cleared bit in the register masks the peripheral event, preventing the processor from servicing the event.
- SIC Interrupt Status Register (SIC_ISR) – As multiple peripherals can be mapped to a single event, this register allows the software to determine which peripheral event source triggered the interrupt. A set bit indicates the peripheral is asserting the interrupt, and a cleared bit indicates the peripheral is not asserting the event.
- SIC Interrupt Wakeup Enable Register (SIC_IWR) – By enabling the corresponding bit in this register, a peripheral can be configured to wake up the processor, should the core be idled when the event is generated. (For more information, see Dynamic Power Management on page 10.)

Because multiple interrupt sources can map to a single general-purpose interrupt, multiple pulse assertions can occur simultaneously, before or during interrupt processing for an interrupt event already detected on this interrupt input. The IPEND register contents are monitored by the SIC as the interrupt acknowledgement.

The appropriate ILAT register bit is set when an interrupt rising edge is detected (detection requires two core clock cycles). The bit is cleared when the respective IPEND register bit is set. The IPEND bit indicates that the event has entered into the processor pipeline. At this point the CEC will recognize and queue the next rising edge event on the corresponding event input. The minimum latency from the rising edge transition of the general-purpose interrupt to the IPEND output asserted is three core clock cycles; however, the latency can be much higher, depending on the activity within and the state of the processor.

DMA Controllers

The ADSP-21532 has multiple, independent DMA controllers that support automated data transfers with minimal overhead for the DSP core. DMA transfers can occur

between the ADSP-21532's internal memories and any of its DMA-capable peripherals. Additionally, DMA transfers can be accomplished between any of the DMA-capable peripherals and external devices connected to the external memory interfaces, including the SDRAM controller and the asynchronous memory controller. DMA-capable peripherals include the SPORTs, SPI port, UART, and PPI. Each individual DMA-capable peripheral has at least one dedicated DMA channel.

The ADSP-21532 DMA controller supports both 1-dimensional (1D) and 2-dimensional (2D) DMA transfers. DMA transfer initialization can be implemented from registers or from sets of parameters called descriptor blocks.

The 2D DMA capability supports arbitrary row and column sizes up to 64K elements by 64K elements, and arbitrary row and column step sizes up to +/- 32K elements. Furthermore, the column step size can be less than the row step size, allowing implementation of interleaved data streams. This feature is especially useful in video applications where data can be de-interleaved on the fly.

Examples of DMA types supported by the ADSP-21532 DMA controller include:

- A single, linear buffer that stops upon completion
- A circular, auto-refreshing buffer that interrupts on each full or fractionally full buffer
- 1-D or 2-D DMA using a linked list of descriptors
- 2-D DMA using an array of descriptors, specifying only the base DMA address within a common page

In addition to the dedicated peripheral DMA channels, there are two memory DMA channels provided for transfers between the various memories of the ADSP-21532 system. This enables transfers of blocks of data between any of the memories—including external SDRAM, ROM, SRAM, and flash memory—with minimal processor intervention. Memory DMA transfers can be controlled by a very flexible descriptor-based methodology or by a standard register-based autobuffer mechanism.

Real-Time Clock

The ADSP-21532 Real-Time Clock (RTC) provides a robust set of digital watch features, including current time, stopwatch, and alarm. The RTC is clocked by a 32.768 KHz crystal external to the ADSP-21532. The RTC peripheral has dedicated power supply pins so that it can remain powered up and clocked even when the rest of the processor is in a low-power state. The RTC provides several programmable interrupt options, including interrupt per second, minute, hour, or day clock ticks, interrupt on programmable stopwatch countdown, or interrupt at a programmed alarm time.

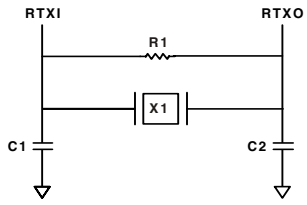
The 32.768 KHz input clock frequency is divided down to a 1 Hz signal by a prescaler. The counter function of the timer consists of four counters: a 60-second counter, a 60-minute counter, a 24-hour counter, and an 32,768-day counter.

When enabled, the alarm function generates an interrupt when the output of the timer matches the programmed value in the alarm control register. There are two alarms: The first alarm is for a time of day. The second alarm is for a day and time of that day.

The stopwatch function counts down from a programmed value, with one-second resolution. When the stopwatch is enabled and the counter underflows, an interrupt is generated.

Like the other peripherals, the RTC can wake up the ADSP-21532 processor from a low-power state upon generation of any RTC wakeup event.

Connect RTC pins RTXI and RTXO with external components as shown in Figure 3.



SUGGESTED COMPONENTS:
ECLIPTEK EC38J (THROUGH-HOLE PACKAGE)
EPSON MC405 12 pF LOAD (SURFACE MOUNT PACKAGE)
C1 = 22 pF
C2 = 22 pF
R1 = 10MV

NOTE: C1 AND C2 ARE SPECIFIC TO CRYSTAL SPECIFIED FOR X1. CONTACT CRYSTAL MANUFACTURER FOR DETAILS. C1 AND C2 SPECIFICATIONS ASSUME BOARD TRACE CAPACITANCE OF 3 pF.

Figure 3. External Components for RTC

Watchdog Timer

The ADSP-21532 includes a 32-bit timer that can be used to implement a software watchdog function. A software watchdog can improve system availability by forcing the processor to a known state through generation of a hardware reset, non-maskable interrupt (NMI), or general-purpose interrupt, if the timer expires before being reset by software. The programmer initializes the count value of the timer, enables the appropriate interrupt, then enables the timer. Thereafter, the software must reload the counter before it counts to zero from the programmed value. This protects the system from remaining in an unknown state where software, which would normally reset the timer, has stopped running due to an external noise condition or software error.

If configured to generate a hardware reset, the watchdog timer resets both the core and the ADSP-21532 peripherals. After a reset, software can determine if the watchdog was the source of the hardware reset by interrogating a status bit in the watchdog timer control register.

The timer is clocked by the system clock (SCLK), at a maximum frequency of f_{SCLK}.

Timers

There are four general-purpose programmable timer units in the ADSP-21532. Three timers have an external pin that can be configured either as a Pulse Width Modulator (PWM) or timer output, as an input to clock the timer, or as a mechanism for measuring pulse widths and periods of external events. These timers can be synchronized to an external clock input to the PF1 pin, an external clock input to the PPI_CLK pin, or to the internal SCLK.

The timer units can be used in conjunction with the UART to measure the width of the pulses in the data stream to provide an auto-baud detect function for a serial channel.

The timers can generate interrupts to the processor core providing periodic events for synchronization, either to the system clock or to a count of external signals.

In addition to the three general-purpose programmable timers, a fourth timer is also provided. This extra timer is clocked by the internal processor clock and is typically used as a system tick clock for generation of operating system periodic interrupts.

Serial Ports (SPORTs)

The ADSP-21532 incorporates two dual-channel synchronous serial ports (SPORT0 and SPORT1) for serial and multiprocessor communications. The SPORTs support the following features:

- I^2S capable operation.
- Bidirectional operation – Each SPORT has two sets of independent transmit and receive pins, enabling eight channels of I^2S stereo audio.
- Buffered (8-deep) transmit and receive ports – Each port has a data register for transferring data words to and from other DSP components and shift registers for shifting data in and out of the data registers.
- Clocking – Each transmit and receive port can either use an external serial clock or generate its own, in frequencies ranging from (f_{SCLK}/131,070) Hz to (f_{SCLK}/2) Hz.
- Word length – Each SPORT supports serial data words from 3 to 32 bits in length, transferred most-significant-bit first or least-significant-bit first.
- Framing – Each transmit and receive port can run with or without frame sync signals for each data word. Frame sync signals can be generated internally or externally, active high or low, and with either of two pulsewidths and early or late frame sync.
- Companding in hardware – Each SPORT can perform A-law or μ-law companding according to ITU recommendation G.711. Companding can be selected on the transmit and/or receive channel of the SPORT without additional latencies.
- DMA operations with single-cycle overhead – Each SPORT can automatically receive and transmit multiple buffers of memory data. The DSP can link or chain sequences of DMA transfers between a SPORT and memory.
- Interrupts – Each transmit and receive port generates an interrupt upon completing the transfer of a data word or after transferring an entire data buffer or buffers through DMA.
- Multichannel capability – Each SPORT supports 128 channels out of a 1024-channel window and is compatible with the H.100, H.110, MVIP-90, and HMVIP standards.

Serial Peripheral Interface (SPI) Port

The ADSP-21532 has an SPI-compatible port that enables the processor to communicate with multiple SPI-compatible devices.

The SPI interface uses three pins for transferring data: two data pins (Master Output-Slave Input, MOSI, and Master Input-Slave Output, MISO) and a clock pin (Serial Clock, SCK). An SPI chip select input pin ($\overline{\text{SPISS}}$) lets other SPI devices select the DSP, and seven SPI chip select output pins ($\overline{\text{SPISEL7–1}}$) let the DSP select other SPI devices. The SPI select pins are reconfigured Programmable Flag pins. Using these pins, the SPI port provides a full-duplex, synchronous serial interface, which supports both master/slave modes and multimaster environments.

The SPI port's baud rate and clock phase/polarities are programmable (see Figure 4), and it has an integrated DMA controller, configurable to support transmit or receive data streams. The SPI's DMA controller can only service unidirectional accesses at any given time.

$$SPI\ Clock\ Rate = \frac{f_{SCLK}}{2 \times SPIBAUD}$$

where SPIBAUD = 2 to 65,535

Figure 4. SPI Clock Rate Calculation

During transfers, the SPI port simultaneously transmits and receives by serially shifting data in and out on its two serial data lines. The serial clock line synchronizes the shifting and sampling of data on the two serial data lines.

UART Port

The ADSP-21532 provides a full-duplex Universal Asynchronous Receiver/Transmitter (UART) port, which is fully compatible with PC-standard UARTs. The UART port

provides a simplified UART interface to other peripherals or hosts, supporting full-duplex, DMA-supported, asynchronous transfers of serial data. The UART port includes support for 5 to 8 data bits, 1 or 2 stop bits, and none, even, or odd parity. The UART port supports two modes of operation:

- PIO (Programmed I/O) – The processor sends or receives data by writing or reading I/O-mapped UART registers. The data is double-buffered on both transmit and receive.
- DMA (Direct Memory Access) – The DMA controller transfers both transmit and receive data. This reduces the number and frequency of interrupts required to transfer data to and from memory. The UART has two dedicated DMA channels, one for transmit and one for receive. These DMA channels have lower default priority than most DMA channels because of their relatively low service rates.

The UART port's baud rate (see Figure 5), serial data format, error code generation and status, and interrupts are programmable:

- Supporting bit rates ranging from (f_{SCLK}/ 1,048,576) to (f_{SCLK}/16) bits per second.
- Supporting data formats from 7 to12 bits per frame.
- Both transmit and receive operations can be configured to generate maskable interrupts to the processor.

$$UART\ Clock\ Rate = \frac{f_{SCLK}}{16 \times D}$$

where D = 1 to 65,536

Figure 5. UART Clock Rate Calculation

In conjunction with the general-purpose timer functions, autobaud detection is supported.

The capabilities of the UART are further extended with support for the Infrared Data Association (IrDA®) Serial Infrared Physical Layer Link Specification (SIR) protocol.

Programmable Flags (PFx)
The ADSP-21532 has 16 bi-directional, general-purpose Programmable Flag (PF15–0) pins. Each programmable flag can be individually controlled by manipulation of the flag control, status and interrupt registers:

- Flag Direction Control Register – Specifies the direction of each individual PFx pin as input or output.
- Flag Control and Status Registers – The ADSP-21532 employs a “write one to modify” mechanism that allows any combination of individual flags to be modified in a single instruction, without affecting the level of any other flags. Four control registers are provided. One register is written in order to set flag values, one register is written in order to clear flag values, one register is written in order to toggle flag values, and one register is written in order to specify a flag value. Reading the flag status register allows software to interrogate the sense of the flags.
- Flag Interrupt Mask Registers – The two Flag Interrupt Mask Registers allow each individual PFx pin to function as an interrupt to the processor. Similar to the two Flag Control Registers that are used to set and clear individual flag values, one Flag Interrupt Mask Register sets bits to enable interrupt function, and the other Flag Interrupt Mask register clears bits to disable interrupt function. PFx pins defined as inputs can be configured to generate hardware interrupts, while output PFx pins can be triggered by software interrupts.
- Flag Interrupt Sensitivity Registers – The two Flag Interrupt Sensitivity Registers specify whether individual PFx pins are level- or edge-sensitive and specify—if edge-sensitive—whether just the rising edge or both the rising and falling edges of the signal are significant. One register selects the type of sensitivity, and one register selects which edges are significant for edge-sensitivity.

Parallel Peripheral Interface
The ADSP-21532 provides a Parallel Peripheral Interface (PPI) that can connect directly to parallel A/D and D/A converters, video encoders and decoders, and other general purpose peripherals. The PPI consists of a dedicated input clock pin, up to 3 frame synchronization pins, and up to 16 data pins. The input clock supports parallel data rates up to f_{SCLK}/2 MHz, and the synchronization signals can be configured as either inputs or outputs.

The PPI supports a variety of general purpose and ITU-R 656 modes of operation. In general purpose mode, the PPI provides half-duplex, bi-directional data transfer with up to 16 bits of data. Up to 3 frame synchronization signals are also provided. In ITU-R 656 mode, the PPI provides half-duplex, bi-directional transfer of 8- or 10-bit video data. Additionally, on-chip decode of embedded start-of-line (SOL) and start-of-field (SOF) preamble packets is supported.

General Purpose Mode Descriptions
The GP modes of the PPI are intended to suit a wide variety of data capture and transmission applications. Three distinct sub-modes are supported:

- Input Mode - Frame Syncs and data are inputs into the PPI.
- Frame Capture Mode - Frame Syncs are outputs from the PPI, but data are inputs.
- Output Mode - Frame Syncs and data are outputs from the PPI.

Input Mode
This mode is intended for ADC applications, as well as video communication with hardware signaling. In its simplest form, PPI_FS1 is an external frame sync input that

controls when to read data. The PPI_DELAY MMR allows for a delay (in PPI_CLK cycles) between reception of this frame sync and the initiation of data reads. The number of input data samples is user-programmable and defined by the contents of the PPI_COUNT register. Data widths of 8, 10, 11, 12, 13, 14, 15 and 16-bits are supported, as programmed by the PPI_CONTROL register.

Frame Capture Mode
This mode allows the video source(s) to act as a slave (e.g., for frame capture). The ADSP-21532 controls when to read from the video source(s). PPI_FS1 is an HSYNC output and PPI_FS2 is a VSYNC output.

Output Mode
This mode is used for transmitting video or other data with up to three output frame syncs. Typically, a single frame sync is appropriate for data converter applications, whereas two or three frame syncs could be used for sending video with hardware signaling.

ITU -R 656 Mode Descriptions
The ITU-R 656 modes of the PPI are intended to suit a wide variety of video capture, processing, and transmission applications. Three distinct sub-modes are supported:

- Active Video Only Mode
- Vertical Blanking Only Mode
- Entire Field Mode

Active Video Only Mode
This mode is used when only the active video portion of a field is of interest and not any of the blanking intervals. The PPI will not read in any data between the End of Active Video (EAV) and Start of Active Video (SAV) preamble symbols, or any data present during the vertical blanking intervals. In this mode, the control byte sequences are not stored to memory; they are filtered by the PPI. After synchronizing to the start of Field 1, the PPI will ignore incoming samples until it sees an SAV code. The user specifies the number of active video lines per frame (in PPI_COUNT register).

Vertical Blanking Interval Mode
In this mode, the PPI only transfers vertical blanking interval (VBI) data.

Entire Field Mode
In this mode, the entire incoming bit stream is read in through the PPI. This includes active video, control preamble sequences, and ancillary data that may be embedded in horizontal and vertical blanking intervals. Data transfer starts immediately after synchronization to Field 1.

Dynamic Power Management
The ADSP-21532 provides four operating modes, each with a different performance/power profile. In addition, Dynamic Power Management provides the control functions to dynamically alter the processor core supply voltage, further reducing power dissipation. Control of clocking to each of the ADSP-21532 peripherals also reduces power consumption. See Table 3 for a summary of the power settings for each mode.

Full-On Operating Mode – Maximum Performance
In the Full-On mode, the PLL is enabled and is not bypassed, providing capability for maximum operational frequency. This is the power-up default execution state in which maximum performance can be achieved. The processor core and all enabled peripherals run at full speed.

Active Operating Mode – Moderate Power Savings
In the Active mode, the PLL is enabled but bypassed. Because the PLL is bypassed, the processor's core clock (CCLK) and system clock (SCLK) run at the input clock (CLKIN) frequency. In this mode, the CLKIN to CCLK multiplier ratio can be changed, although the changes are not realized until the Full-On mode is entered. DMA access is available to appropriately configured L1 memories.

In the Active mode, it is possible to disable the PLL through the PLL Control register (PLL_CTL). If disabled, the PLL must be re-enabled before transitioning to the Full-On or Sleep modes.

Table 3. Power Settings

Mode	PLL	PLL Bypassed	Core Clock (CCLK)	System Clock (SCLK)
Full On	Enabled	No	Enabled	Enabled
Active	Enabled/ Disabled	Yes	Enabled	Enabled
Sleep	Enabled	–	Disabled	Enabled
Deep Sleep	Disabled	–	Disabled	Disabled

Sleep Operating Mode – High Power Savings
The Sleep mode reduces power dissipation by disabling the clock to the processor core (CCLK). The PLL and system clock (SCLK), however, continue to operate in this mode. Typically an external event or RTC activity will wake up the processor. When in the Sleep mode, assertion of wakeup will cause the processor to sense the value of the BYPASS bit in the PLL Control register (PLL_CTL). If BYPASS is disabled, the processor will transition to the Full On mode. If BYPASS is enabled, the processor will transition to the Active mode.

When in the Sleep mode, system DMA access to L1 memory is not supported.

Deep Sleep Operating Mode – Maximum Power Savings
The Deep Sleep mode maximizes power savings by disabling the clocks to the processor core (CCLK) and to all synchronous peripherals (SCLK). Asynchronous

peripherals, such as the RTC, may still be running but will not be able to access internal resources or external memory. This powered-down mode can only be exited by assertion of the reset interrupt ($\overline{\text{RESET}}$) or by an asynchronous interrupt generated by the RTC. When in Deep Sleep mode, assertion of $\overline{\text{RESET}}$ or the RTC asynchronous interrupt causes the processor to transition to the Full On mode.

Power Savings

As shown in Table 4, the ADSP-21532 supports three different power domains. The use of multiple power domains maximizes flexibility, while maintaining compliance with industry standards and conventions. By isolating the internal logic of the ADSP-21532 into its own power domain, separate from the RTC and other I/O, the processor can take advantage of Dynamic Power Management, without affecting the RTC or other I/O devices.

Table 4. Power Domains

Power Domain	VDD Range
All internal logic, except RTC	V_{DDINT}
RTC internal logic and crystal I/O	V_{DDRTC}
All other I/O	V_{DDEXT}

The power dissipated by a processor is largely a function of the clock frequency of the processor and the square of the operating voltage. For example, reducing the clock frequency by 25% results in a 25% reduction in power dissipation, while reducing the voltage by 25% reduces power dissipation by more than 40%. Further, these power savings are additive, in that if the clock frequency and supply voltage are both reduced, the power savings can be dramatic.

The Dynamic Power Management feature of the ADSP-21532 allows both the processor's input voltage (V_{DDINT}) and clock frequency (f_{CCLK}) to be dynamically controlled.

As explained above, the savings in power dissipation can be modeled by the following equations:

Power Savings Factor

$$= \frac{f_{CCLKRED}}{f_{CCLKNOM}} \times \left(\frac{V_{DDINTRED}}{V_{DDINTNOM}}\right)^2 \times \left(\frac{T_{RED}}{T_{NOM}}\right)$$

$$\%\ Power\ Savings\ =\ (1 - Power\ Savings\ Factor) \times 100\%$$

where the variables in the equations are:

- $f_{CCLKNOM}$ is the nominal core clock frequency
- $f_{CCLKRED}$ is the reduced core clock frequency
- $V_{DDINTNOM}$ is the nominal internal supply voltage
- $V_{DDINTRED}$ is the reduced internal supply voltage
- T_{NOM} is the duration running at $f_{CCLKNOM}$
- T_{RED} is the duration running at $f_{CCLKRED}$

Voltage Regulation

The ADSP-21532 provides an on-chip voltage regulator that can generate internal voltage levels from an external 2.25 V to 3.6 V supply. Figure 6 shows the typical external components required to complete the power management system. The regulator controls the internal logic voltage levels and is programmable with the Voltage Regulator Control Register (VR_CTL) in increments of 50 mV. The regulator can also be disabled and bypassed at the user's discretion.

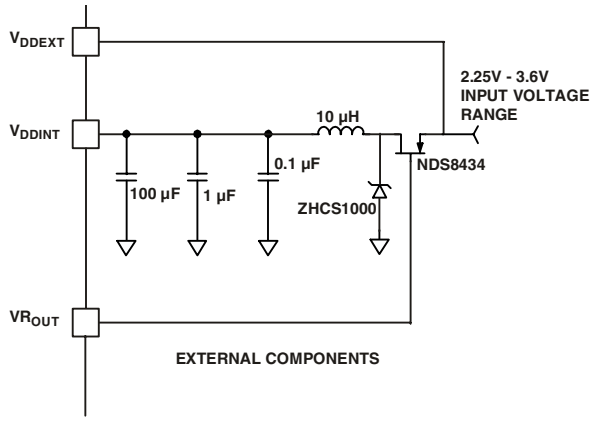


Figure 6. Voltage Regulator Circuit

Clock Signals

The ADSP-21532 can be clocked by an external crystal, a sine wave input, or a buffered, shaped clock derived from an external clock oscillator.

If an external clock is used, it should be a TTL compatible signal and must not be halted, changed, or operated below the specified frequency during normal operation. This signal is connected to the DSP's CLKIN pin. When an external clock is used, the XTAL pin must be left unconnected.

Alternatively, because the ADSP-21532 includes an on-chip oscillator circuit, an external crystal may be used. The crystal should be connected across the CLKIN and XTAL pins, with two capacitors connected as shown in Figure 7. Capacitor values are dependent on crystal type and should

be specified by the crystal manufacturer. A parallel-resonant, fundamental frequency, microprocessor-grade crystal should be used.

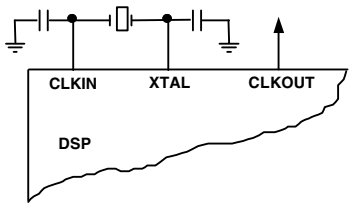


Figure 7. External Crystal Connections

As shown in Figure 8 on page 12, the core clock (CCLK) and system peripheral clock (SCLK) are derived from the input clock (CLKIN) signal. An on-chip PLL is capable of multiplying the CLKIN signal by a user programmable 1x to 31x multiplication factor. The default multiplier is 10x, but it can be modified by a software instruction sequence. On-the-fly frequency changes can be effected by simply writing to the PLL_DIV register.

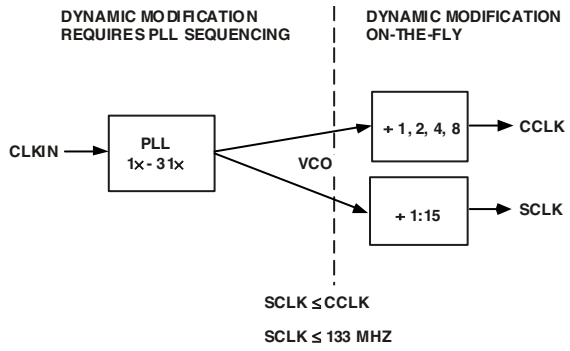


Figure 8. Frequency Modification Methods

All on-chip peripherals are clocked by the system clock (SCLK). The system clock frequency is programmable by means of the SSEL3–0 bits of the PLL_DIV register. The values programmed into the SSEL fields define a divide ratio between the PLL output (VCO) and the system clock. SCLK divider values are 1 through 15. Table 5 illustrates typical system clock ratios:

Table 5. Example System Clock Ratios

Signal Name SSEL3–0	Divider Ratio VCO/SCLK	Example Frequency Ratios (MHz)	
		VCO	SCLK
0001	1:1	100	100
0110	6:1	300	50
1111	15:1	300	20

The maximum frequency of the system clock is f_{SCLK}. Note that the divisor ratio must be chosen to limit the system clock frequency to its maximum of f_{SCLK}. The SSEL value can be changed dynamically without any PLL lock latencies by writing the appropriate values to the PLL divisor register (PLL_DIV).

The core clock (CCLK) frequency can also be dynamically changed by means of the CSEL1–0 bits of the PLL_DIV register. Supported CCLK divider ratios are 1, 2, 4, and 8, as shown in Table 6. This programmable core clock capability is useful for fast core frequency modifications.

Table 6. Core Clock Ratios

Signal Name CSEL1–0	Divider Ratio VCO/CCLK	Example Frequency Ratios	
		VCO	CCLK
00	1:1	300	300
01	2:1	300	150
10	4:1	200	50
11	8:1	200	25

Booting Modes

The ADSP-21532 has three mechanisms (listed in Table 7) for automatically loading internal L1 instruction memory after a reset. A fourth mode is provided to execute from external memory, bypassing the boot sequence.

Table 7. Booting Modes

BMODE1–0	Description
00	Execute from 16-bit external memory (Bypass Boot ROM)
01	Boot from 8-bit flash
10	Boot from SPI serial ROM (8-bit address range)
11	Boot from SPI serial ROM (16-bit address range)

The BMODE pins of the Reset Configuration Register, sampled during power-on resets and software-initiated resets, implement the following modes:

- Execute from 16-bit external memory – Execution starts from address 0x2000000 with 16-bit packing. The boot ROM is bypassed in this mode. All configuration settings are set for the slowest device possible (3-cycle hold time; 15-cycle R/W access times; 4-cycle setup).
- Boot from 8-bit external FLASH memory – The 8-bit FLASH boot routine located in boot ROM memory space is set up using Asynchronous Memory Bank 0. All configuration settings are set for the slowest device possible (3-cycle hold time; 15-cycle R/W access times; 4-cycle setup).

- Boot from SPI serial EEPROM (8-bit addressable) – The SPI uses the PF2 output pin to select a single SPI EPROM device, submits a read command at address 0x00, and begins clocking data into the beginning of L1 instruction memory. An 8-bit addressable SPI-compatible EPROM must be used.
- Boot from SPI serial EEPROM (16-bit addressable) – The SPI uses the PF2 output pin to select a single SPI EPROM device, submits a read command at address 0x0000, and begins clocking data into the beginning of L1 instruction memory. A 16-bit addressable SPI-compatible EPROM must be used.

For each of the boot modes, an 8-byte header is first read from an external memory device. The header specifies the number of bytes to be transferred and the memory destination address. Multiple memory blocks may be loaded by any boot sequence. Once all blocks are loaded, program execution commences from the start of L1 instruction SRAM (0xFFA0 8000). For customer specified ROM devices, the boot ROM is bypassed and execution begins from the start of L1 instruction ROM (0xFFA0 0000).

In addition, bit 4 of the Reset Configuration Register can be set by application code to bypass the normal boot sequence during a software reset. For this case, the processor jumps directly to the beginning of L1 instruction memory.

To augment the boot modes, a secondary software loader is provided that adds additional booting mechanisms. This secondary loader provides the capability to boot from 16-bit FLASH memory, fast FLASH, variable baud rate, and other sources.

Instruction Set Description

The Blackfin processor family assembly language instruction set employs an algebraic syntax designed for ease of coding and readability. The instructions have been specifically tuned to provide a flexible, densely encoded instruction set that compiles to a very small final memory size. The instruction set also provides fully featured multifunction instructions that allow the programmer to use many of the DSP core resources in a single instruction. Coupled with many features more often seen on microcontrollers, this instruction set is very efficient when compiling C and C++ source code. In addition, the architecture supports both user (algorithm/application code) and supervisor (O/S kernel, device drivers, debuggers, ISRs) modes of operation, allowing multiple levels of access to core DSP resources.

The assembly language, which takes advantage of the processor's unique architecture, offers the following advantages:

- Seamlessly integrated DSP/CPU features are optimized for both 8-bit and 16-bit operations.
- A multi-issue load/store modified-Harvard architecture, which supports two 16-bit MAC or four 8-bit ALU + two load/store + two pointer updates per cycle.
- All registers, I/O, and memory are mapped into a unified 4G byte memory space, providing a simplified programming model.
- Microcontroller features, such as arbitrary bit and bit-field manipulation, insertion, and extraction; integer operations on 8-, 16-, and 32-bit data-types; and separate user and supervisor stack pointers.
- Code density enhancements, which include intermixing of 16- and 32-bit instructions (no mode switching, no code segregation). Frequently used instructions are encoded in 16 bits.

Development Tools

The ADSP-21532 is supported with a complete set of CROSSCORE™ software and hardware development tools, including Analog Devices emulators and the VisualDSP++® development environment. The same emulator hardware that supports other Analog Devices DSPs also fully emulates the ADSP-21532.

The VisualDSP++ project management environment lets programmers develop and debug an application. This environment includes an easy-to-use assembler that is based on an algebraic syntax, an archiver (librarian/library builder), a linker, a loader, a cycle-accurate instruction-level simulator, a C/C++ compiler, and a C/C++ run-time library that includes DSP and mathematical functions. A key point for these tools is C/C++ code efficiency. The compiler has been developed for efficient translation of C/C++ code to Blackfin processor assembly. The Blackfin processor has architectural features that improve the efficiency of compiled C/C++ code.

Debugging both C/C++ and assembly programs with the VisualDSP++ debugger, programmers can:

- View mixed C/C++ and assembly code (interleaved source and object information)
- Insert breakpoints
- Set conditional breakpoints on registers, memory, and stacks
- Trace instruction execution
- Perform linear or statistical profiling of program execution
- Fill, dump, and graphically plot the contents of memory
- Perform source level debugging
- Create custom debugger windows

The VisualDSP++ IDE lets programmers define and manage DSP software development. Its dialog boxes and property pages let programmers configure and manage all development tools, including Color Syntax Highlighting in the VisualDSP++ editor. These capabilities permit programmers to:

- Control how the development tools process inputs and generate outputs.
- Maintain a one-to-one correspondence with the tool's command line switches.

The VisualDSP++ Kernel (VDK) incorporates scheduling and resource management tailored specifically to address the memory and timing constraints of DSP programming. These capabilities enable engineers to develop code more effectively, eliminating the need to start from the very beginning, when developing new application code. The VDK features include threads, critical and unscheduled regions, semaphores, events, and device flags. The VDK also supports priority-based, pre-emptive, cooperative and time-sliced scheduling approaches. In addition, the VDK was designed to be scalable. If the application does not use a specific feature, the support code for that feature is excluded from the target system.

Because the VDK is a library, a developer can decide whether to use it or not. The VDK is integrated into the VisualDSP++ development environment, but can also be used with standard command-line tools. When the VDK is used, the development environment assists the developer with many error-prone tasks and assists in managing system resources, automating the generation of various VDK based objects, and visualizing the system state, when debugging an application that uses the VDK.

Analog Devices' DSP emulators use the IEEE 1149.1 JTAG test access port of the ADSP-21532 to monitor and control the target board processor during emulation. The emulator provides full-speed emulation, allowing inspection and modification of memory, registers, and processor stacks. Non intrusive in-circuit emulation is assured by the use of the processor's JTAG interface—the emulator does not affect target system loading or timing.

In addition to the software and hardware development tools available from Analog Devices, third parties provide a wide range of tools supporting the Blackfin processor family. Hardware tools include the ADSP-21532 EZ-Kit standalone evaluation/development cards. Third Party software tools include DSP libraries, real-time operating systems, and block diagram design tools.

Designing an Emulator-Compatible DSP Board (Target)

The Analog Devices family of emulators are tools that the DSP developer needs to test and debug hardware and software systems. Analog Devices has supplied an IEEE 1149.1 JTAG Test Access Port (TAP) on the ADSP-21532. The emulator uses the TAP to access the internal features of the DSP, allowing the developer to load code, set breakpoints, observe variables, observe memory, and examine registers. The DSP must be halted to send data and commands, but once an operation has been completed by the emulator, the DSP system is set running at full speed with no impact on system timing.

To use these emulators, the target's design must include the interface between an Analog Devices' JTAG DSP and the emulation header on a custom DSP target board.

Target Board Header

The emulator interface to an Analog Devices' JTAG DSP is a 14-pin header, as shown in Figure 9 on page 14. The customer must supply this header on the target board in order to communicate with the emulator. The interface consists of a standard dual row 0.025" square post header, set on 0.1" x 0.1" spacing, with a minimum post length of 0.235". Pin 3 is the key position used to prevent the pod from being inserted backwards. This pin must be clipped on the target board.

Also, the clearance (length, width, and height) around the header must be considered. Leave a clearance of at least 0.15" and 0.10" around the length and width of the header, and reserve a height clearance to attach and detach the pod connector.

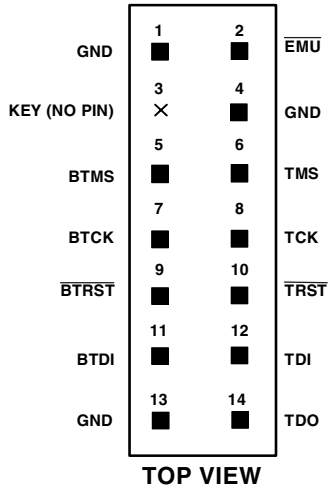


Figure 9. JTAG Target Board Connector for JTAG Equipped Analog Devices DSP (Jumpers in Place)

As can be seen in Figure 9, there are two sets of signals on the header. There are the standard JTAG signals TMS, TCK, TDI, TDO, $\overline{\text{TRST}}$, and $\overline{\text{EMU}}$ used for emulation purposes (via an emulator). There are also secondary JTAG signals BTMS, BTCK, BTDI, and $\overline{\text{BTRST}}$ that are optionally used for board-level (boundary scan) testing. These

secondary JTAG signals can be connected to a separate JTAG boundary scan controller, if used. If not used, tie them to ground as shown in Figure 10 on page 15.

When the emulator is not connected to this header, place jumpers across BTMS, BTCK, BTRST, and BTDI as shown in Figure 10. This holds the JTAG signals in the correct state to allow the DSP to run free. Remove all the jumpers when connecting the emulator to the JTAG header.

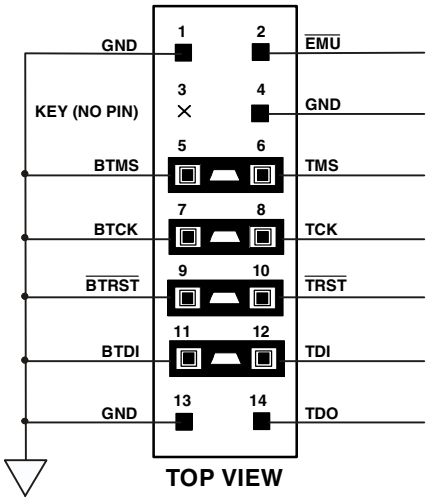


Figure 10. JTAG Target Board Connector with No Local Boundary Scan

JTAG Emulator Pod Connector

Figure 11 details the dimensions of the JTAG pod connector at the 14-pin target end. Figure 12 displays the keep-out area for a target board header. The keep-out area allows the pod connector to properly seat onto the target board header. This board area should contain no components (chips, resistors, capacitors, etc.). The dimensions are referenced to the center of the 0.25" square post pin.

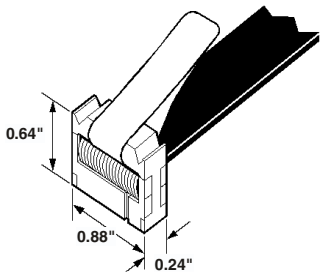


Figure 11. JTAG Pod Connector Dimensions

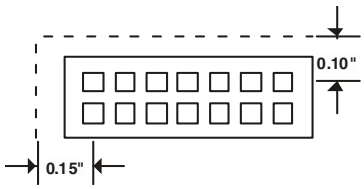


Figure 12. JTAG Pod Connector Keep-Out Area

PIN DESCRIPTIONS

ADSP-21532 pin definitions are listed in Table 8.

In order to maintain maximum functionality and reduce package size and pin count, some pins have dual, multiplexed functionality. In cases where pin functionality is reconfigurable, the default state is shown in plain text, while alternate functionality is shown in italics.

Table 8. Pin Descriptions

Pin Name	I/O	Function
Memory Interface		
ADDR19–1	O	Address Bus for Async/Sync Access
DATA15–0	I/O	Data Bus for Async/Sync Access
ABE1–0	O	Byte Enables
/SDQM1–0		/Data Masks for Async/Sync Access
BR	I	Bus Request
BG	O	Bus Grant
BGH	O	Bus Grant Hang
Asynchronous Memory Control		
AMS3–0	O	Bank Select
ARDY	I	Hardware Ready Control
AOE	O	Output Enable
ARE	O	Read Enable
AWE	O	Write Enable
Synchronous Memory Control		
SRAS	O	Row Address Strobe
SCAS	O	Column Address Strobe
SWE	O	Write Enable
SCKE	O	Clock Enable
CLKOUT	O	Clock Output
SA10	O	A10 Pin
SMS	O	Bank Select
Timers		
TMR0	I/O	Timer 0
TMR1/*PPI_FS1*	I/O	Timer 1/*PPI Frame Sync1*
TMR2/*PPI_FS2*	I/O	Timer 2/*PPI Frame Sync2*
Parallel Peripheral Interface Port/GPIO		
PF0/*SPISS*	I/O	Programmable Flag 0 /*SPI Slave Select Input*
PF1/*SPISEL1* /*TMRCLK*	I/O	Programmable Flag 1 /*SPI Slave Select Enable 1*/ *External Timer Reference*
PF2/*SPISEL2*	I/O	Programmable Flag 2 /*SPI Slave Select Enable 2*
PF3/*SPISEL3* /*PPI_FS3*	I/O	Programmable Flag 3 /*SPI Slave Select Enable 3* /*PPI Frame Sync 3*

Table 8. Pin Descriptions (Continued)

Pin Name	I/O	Function
PF4/*SPISEL4 /PPI15*	I/O	Programmable Flag 4 */SPI Slave Select Enable 4 / PPI 15*
PF5/*SPISEL5 /PPI14*	I/O	Programmable Flag 5 */SPI Slave Select Enable 5 / PPI 14*
PF6/*SPISEL6 /PPI13*	I/O	Programmable Flag 6 */SPI Slave Select Enable 6 / PPI 13*
PF7/*SPISEL7 /PPI12*	I/O	Programmable Flag 7 */SPI Slave Select Enable 7 / PPI 12*
PF8/*PPI11*	I/O	Programmable Flag 8/*PPI 11*
PF9/*PPI10*	I/O	Programmable Flag 9/*PPI 10*
PF10/*PPI9*	I/O	Programmable Flag 10/*PPI 9*
PF11/*PPI8*	I/O	Programmable Flag 11/*PPI 8*
PF12/*PPI7*	I/O	Programmable Flag 12/*PPI 7*
PF13/*PPI6*	I/O	Programmable Flag 13/*PPI 6*
PF14/*PPI5*	I/O	Programmable Flag 14/*PPI 5*
PF15/*PPI4*	I/O	Programmable Flag 15/*PPI 4*
PPI3–0	I/O	PPI3–0
PPI_CLK	I	PPI Clock
Serial Ports		
RSCLK0	I/O	SPORT0 Receive Serial Clock
RFS0	I/O	SPORT0 Receive Frame Sync
DR0PRI	I	SPORT0 Receive Data Primary
DR0SEC	I	SPORT0 Receive Data Secondary
TSCLK0	I/O	SPORT0 Transmit Serial Clock
TFS0	I/O	SPORT0 Transmit Frame Sync
DT0PRI	O	SPORT0 Transmit Data Primary
DT0SEC	O	SPORT0 Transmit Data Secondary
RSCLK1	I/O	SPORT1 Receive Serial Clock
RFS1	I/O	SPORT1 Receive Frame Sync
DR1PRI	I	SPORT1 Receive Data Primary
DR1SEC	I	SPORT1 Receive Data Secondary
TSCLK1	I/O	SPORT1 Transmit Serial Clock
TFS1	I/O	SPORT1 Transmit Frame Sync
DT1PRI	O	SPORT1 Transmit Data Primary
DT1SEC	O	SPORT1 Transmit Data Secondary
SPI Port		
MOSI	I/O	Master Out Slave In
MISO	I/O	Master In Slave Out
SCK	I/O	SPI Clock
UART Port		
RX	I	UART Receive
TX	O	UART Transmit
Real Time Clock		
RTXI	I	RTC Crystal Input
RTXO	O	RTC Crystal Output
JTAG Port		
TCK	I	JTAG Clock
TDO	O	JTAG Serial Data Out
TDI	I	JTAG Serial Data In
TMS	I	JTAG Mode Select
$\overline{\text{TRST}}$	I	JTAG Reset
$\overline{\text{EMU}}$	O	Emulation Output
Clock		
CLKIN	I	Clock/Crystal Input
XTAL	O	Crystal Output

Table 8. Pin Descriptions (Continued)

Pin Name	I/O	Function
Mode Controls		
$\overline{\text{RESET}}$	I	Reset
NMI	I	Non-maskable Interrupt
BMODE1–0	I	Boot Mode Strap
Voltage Regulator		
VROUT	O	External FET Drive
Supplies		
V_{DDEXT}	P	I/O Power Supply
V_{DDINT}	P	Internal Power Supply (regulated from 2.25 V to 3.6 V input)
V_{DDRTC}	P	Real Time Clock Power Supply
GND	G	External Ground

SPECIFICATIONS

RECOMMENDED OPERATING CONDITIONS

Parameter [1]	K Grade Parameter	Min	Nominal	Max	Unit
V_{DDEXT}	External Supply Voltage	2.25	2.5 or 3.3	3.6	V
V_{DDRTC}	Real Time Clock Power Supply Voltage	2.25		3.6	V
V_{IH}	High Level Input Voltage[2], @ V_{DDEXT} = max	2.0		3.6	V
V_{IL}	Low Level Input Voltage[2], @ V_{DDEXT} = min	–0.3		0.6	V
T_{CASE}	Case Operating Temperature	–40		105	°C

[1] Specifications subject to change without notice.

[2] The ADSP-21532 is 3.3 V tolerant (always accepts up to 3.6 V maximum V_{IH}), but voltage compliance (on outputs, V_{OH}) depends on the input V_{DDEXT}, because V_{OH} (max) approximately equals V_{DDEXT} (max). This 3.3 V tolerance applies to bi-directional pins (DATA15-0, TMR2-0, PF15-0, PPI3-0, RSCLK1-0, TSCLK1-0, RFS1-0, TFS1-0, MOSI, MISO, SCK) and input only pins ($\overline{BR}$, ARDY, PPI_CLK, DR0PRI, DR0SEC, DR1PRI, DR1SEC, RX, RTXI, TCK, TDI, TMS, $\overline{TRST}$, CLKIN, $\overline{RESET}$, NMI, and BMODE1-0).

ELECTRICAL CHARACTERISTICS

Parameter[1]		Test Conditions	Min	Max	Unit
V_{OH}	High Level Output Voltage[2]	@ V_{DDEXT} = 3.0V, I_{OH} = –0.5 mA	2.4		V
V_{OL}	Low Level Output Voltage[2]	@ V_{DDEXT} = 3.0V, I_{OL} = 2.0 mA		0.4	V
I_{IH}	High Level Input Current[3]	@ V_{DDEXT} = max, V_{IN} = V_{DD} max		TBD	µA
I_{IL}	Low Level Input Current[4]	@ V_{DDEXT} = max, V_{IN} = 0 V		TBD	µA
I_{OZH}	Three-State Leakage Current[4]	@ V_{DDEXT} = max, V_{IN} = V_{DD} max		TBD	µA
I_{OZL}	Three-State Leakage Current[5]	@ V_{DDEXT} = max, V_{IN} = 0 V		TBD	µA
C_{IN}	Input Capacitance[5, 6]	f_{IN} = 1 MHz, T_{CASE} = 25°C, V_{IN} = 2.5 V		TBD	pF

[1] Specifications subject to change without notice.

[2] Applies to output and bidirectional pins.

[3] Applies to input pins.

[4] Applies to three-statable pins.

[5] Applies to all signal pins.

[6] Guaranteed, but not tested.

ABSOLUTE MAXIMUM RATINGS

External (I/O) Supply Voltage[1] (V_{DDEXT}) . . . . −0.3 to +4.0 V
Input Voltage[1] . . . . . −0.5 to 3.6 V
Output Voltage Swing[1] . . . . . −0.5 to V_{DDEXT}+0.5 V
Load Capacitance[1] . . . . . 200 pF
Core Clock[1] . . . . . 300 MHz
Peripheral Clock (SCLK)[1] . . . . . 133 MHz
Storage Temperature Range[1] . . . . . −65° to +150°C
Lead Temperature (5 seconds)[1] . . . . . .185°C

[1]Stresses greater than those listed above may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD SENSITIVITY

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADSP-21532 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

TIMING SPECIFICATIONS

The tables and figures on the following pages describe the timing characteristics of the ADSP-21532.

Clock and Reset Timing

Table 9 and Figure 13 describe clock and reset operations. Per ABSOLUTE MAXIMUM RATINGS on page 18, combinations of CLKIN and clock multipliers must not select core/peripheral clocks in excess of 300/133 MHz.

Table 9. Clock and Reset Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{CKIN}	CLKIN Period	30.0	100.0	ns
t_{CKINL}	CLKIN Low Pulse[1]	10.0		ns
t_{CKINH}	CLKIN High Pulse[1]	10.0		ns
t_{WRST}	$\overline{\text{RESET}}$ Asserted Pulsewidth Low[2]	11 t_{CKIN}		ns
Switching Characteristics				
t_{SCLKD}	CLKOUT Delay from CLKIN	TBD	TBD	ns
t_{SCLK}	CLKOUT Period[3]	7.5		ns

[1] Applies to bypass mode and non-bypass mode.
[2] Applies after power-up sequence is complete. At power-up, the processor's internal phase-locked loop requires no more than 2000 CLKIN cycles, while $\overline{\text{RESET}}$ is asserted, assuming stable power supplies and CLKIN (not including start-up time of external clock oscillator).
[3] The figure below shows a x2 ratio between t_{CKIN} and t_{SCLK}, but the ratio has many programmable options. For more information, see the System Design chapter of the ADSP-21532 *DSP Hardware Reference*.

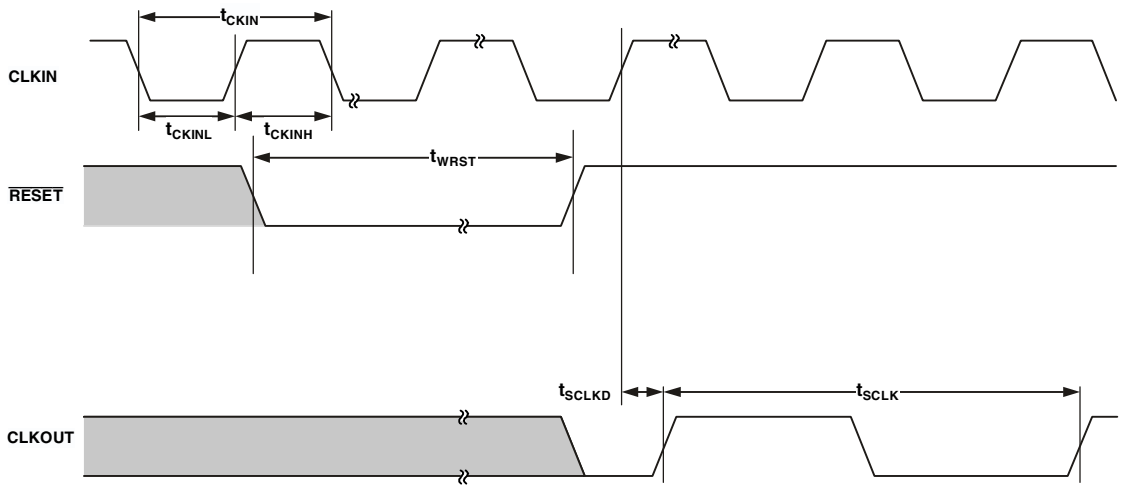


Figure 13. Clock and Reset Timing

Asynchronous Memory Read Cycle Timing

Table 10. Asynchronous Memory Read Cycle Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{SDAT}	DATA15–0 Setup Before CLKOUT	2.1		ns
t_{HDAT}	DATA15–0 Hold After CLKOUT	0.8		ns
t_{SARDY}	ARDY Setup Before CLKOUT	5.5		ns
t_{HARDY}	ARDY Hold After CLKOUT	0.0		ns
Switching Characteristic				
t_{DO}	Output Delay After CLKOUT[1]		6.0	ns
t_{HO}	Output Hold After CLKOUT [1]	0.8		ns

[1] Output pins include $\overline{AMS3-0}$, $\overline{ABE1-0}$, ADDR19–1, $\overline{AOE}$, $\overline{ARE}$.

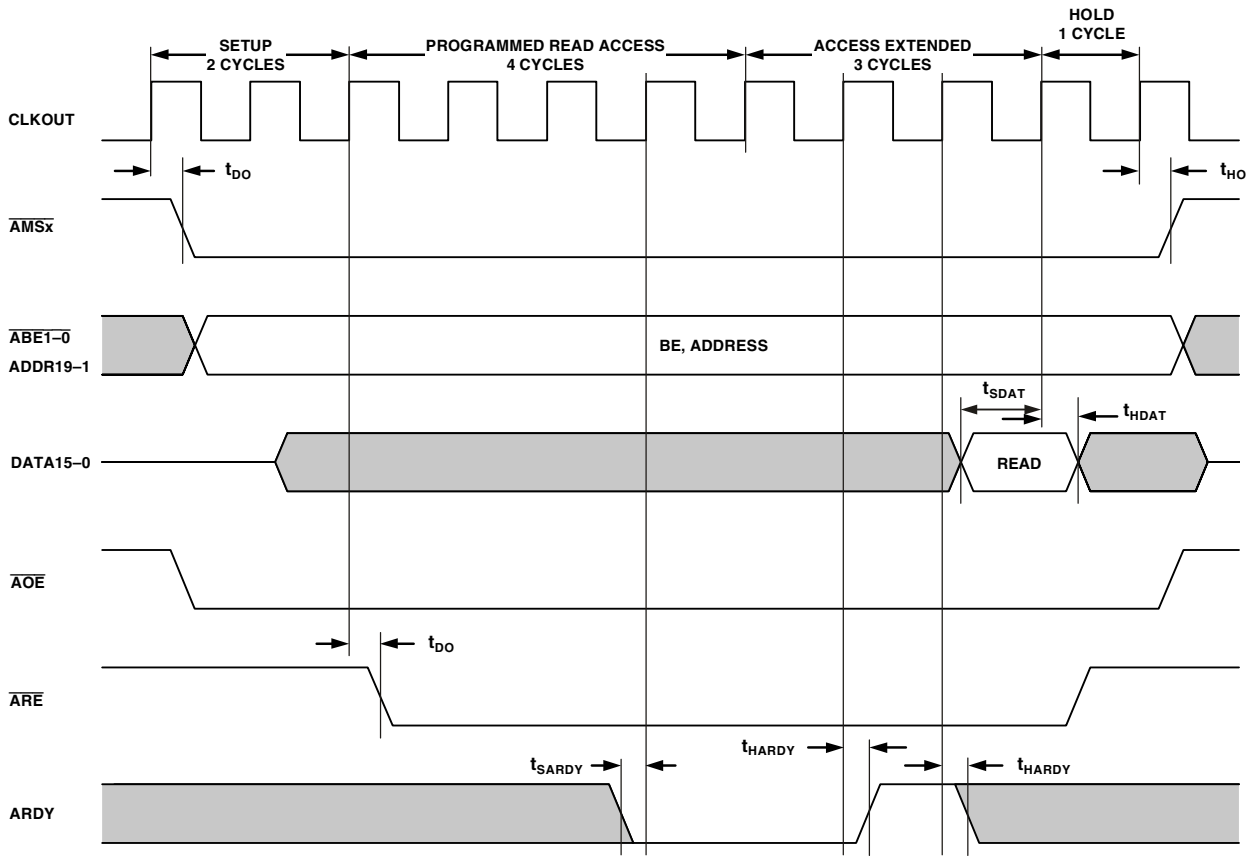


Figure 14. Asynchronous Memory Read Cycle Timing

Asynchronous Memory Write Cycle Timing

Table 11. Asynchronous Memory Write Cycle Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{SARDY}	ARDY Setup Before CLKOUT	5.5		ns
t_{HARDY}	ARDY Hold After CLKOUT	0.0		ns
t_{DDAT}	DATA15–0 Disable After CLKOUT		6.0	ns
t_{ENDAT}	DATA15–0 Enable After CLKOUT	1.0		ns
Switching Characteristic				
t_{DO}	Output Delay After CLKOUT[1]		6.0	ns
t_{HO}	Output Hold After CLKOUT [1]	0.8		ns

[1] Output pins include $\overline{AMS}$3–0, $\overline{ABE}$1–0, ADDR19–1, DATA15–0, $\overline{AOE}$, $\overline{AWE}$.

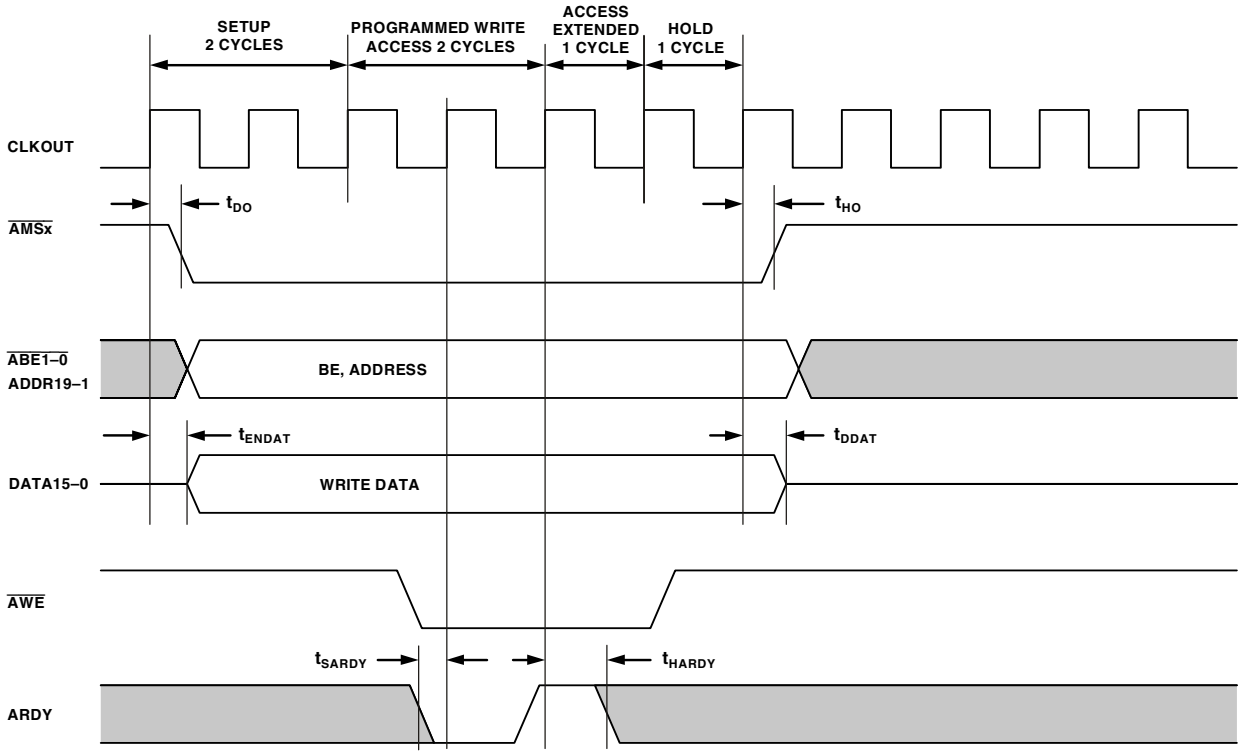


Figure 15. Asynchronous Memory Write Cycle Timing

SDRAM Interface Timing

Table 12. SDRAM Interface Timing

Parameter		Min	Max	Unit
Timing Requirement				
t_{SSDAT}	DATA Setup Before CLKOUT	2.1		ns
t_{HSDAT}	DATA Hold After CLKOUT	0.8		ns
Switching Characteristic				
t_{SCLK}	CLKOUT Period	7.5		ns
t_{SCLKH}	CLKOUT Width High	2.5		ns
t_{SCLKL}	CLKOUT Width Low	2.5		ns
t_{DCAD}	Command, ADDR, Data Delay After CLKOUT[1]		6.0	ns
t_{HCAD}	Command, ADDR, Data Hold After CLKOUT[1]	0.8		ns
t_{DSDAT}	Data Disable After CLKOUT		6.0	ns
t_{ENSDAT}	Data Enable After CLKOUT	1.0		ns

[1] Command pins include: $\overline{SRAS}$, $\overline{SCAS}$, $\overline{SWE}$, SDQM, $\overline{SMS}$, SA10, SCKE.

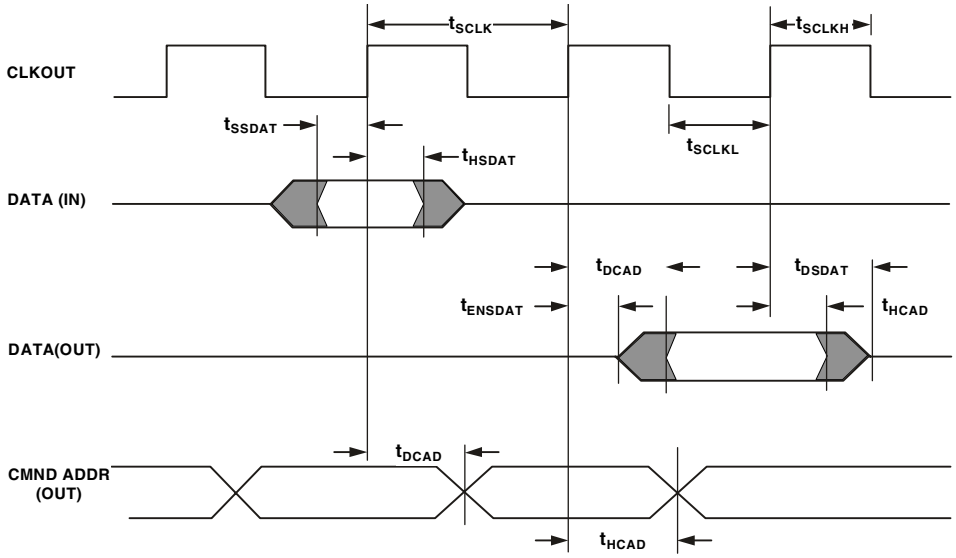


Figure 16. SDRAM Interface Timing

External Port Bus Request and Grant Cycle Timing

Table 13 and Figure 17 describe external port bus request and bus grant operations.

Table 13. External Port Bus Request and Grant Cycle Timing

Parameter[1, 2]		Min	Max	Unit
Timing Requirements				
t_{BS}	$\overline{BR}$ asserted to CLKOUT high setup	4.6		ns
t_{BH}	CLKOUT high to $\overline{BR}$ de-asserted hold time	0.0		ns
Switching Characteristics				
t_{SD}	CLKOUT high to $\overline{xMS}$, address, and $\overline{RD}/\overline{WR}$ disable		4.3	ns
t_{SE}	CLKOUT low to $\overline{xMS}$, address, and $\overline{RD}/\overline{WR}$ enable		4.0	ns
t_{DBG}	CLKOUT high to $\overline{BG}$ asserted setup		2.2	ns
t_{EBG}	CLKOUT high to $\overline{BG}$ de-asserted hold time		2.2	ns
t_{DBH}	CLKOUT high to $\overline{BGH}$ asserted setup		2.4	ns
t_{EBH}	CLKOUT high to $\overline{BGH}$ de-asserted hold time		2.4	ns

[1]These are preliminary timing parameters that are based on worst-case operating conditions.
[2]The pad loads for these timing parameters are 20 pF.

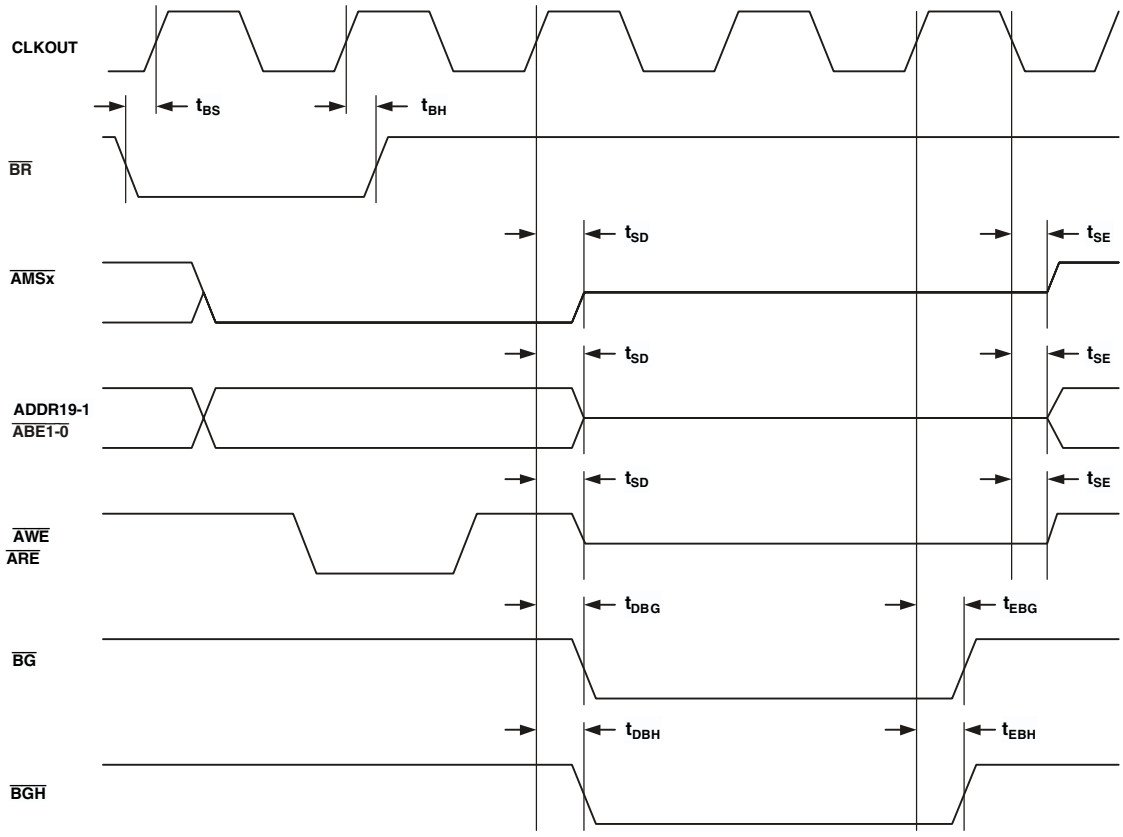


Figure 17. External Port Bus Request and Grant Cycle Timing

Parallel Peripheral Interface Timing

Table 14 and Figure 18 on page 24, Figure 19 on page 25, and Figure 20 on page 25 describe Parallel Peripheral Interface operations.

Table 14. Parallel Peripheral Interface Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{PCLKW}	PPI_CLK Width			
	GP Frame Capture and GP Input Modes	6.0		ns
	GP Output Mode	10.0		ns
t_{PCLK}	PPI_CLK Period[1]			
	GP Frame Capture and GP Input Modes	15.0		ns
	GP Output Mode	25.0		ns
Timing Requirements - GP Input and Frame Capture Modes				
t_{SDRE}	Receive Data Setup Before PPI_CLK[2]	3.0		ns
t_{HDRE}	Receive Data Hold After PPI_CLK[2]	3.0		ns
Switching Characteristics - GP Output and Frame Capture Modes				
t_{DFSE}	FS Delay After PPI_CLK[3]		12.0	ns
t_{DDTE}	Transmit Data Delay After PPI_CLK[3] (GP Output Mode)		12.0	ns
t_{HDTE}	Transmit Data Hold After PPI_CLK[3]	5.0		ns
t_{FS1D}	Delay Between FS1 and Valid Data	1	65536	PPI_CLK periods
t_{FS12}	Delay Between FS2 and FS1[4]	0		PPI_CLK periods
t_{FS13}	Delay Between FS1 and FS3 (GP Output Mode)	0		PPI_CLK periods

[1]PPI_CLK frequency cannot exceed $f_{SCLK}/2$
[2]Referenced to sample edge.
[3]Referenced to drive edge.
[4]FS2 period must be an integer multiple of FS1 period.

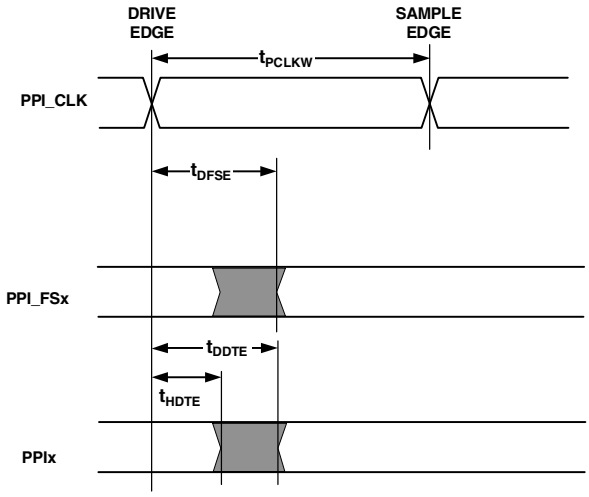


Figure 18. GP Output Mode Timing

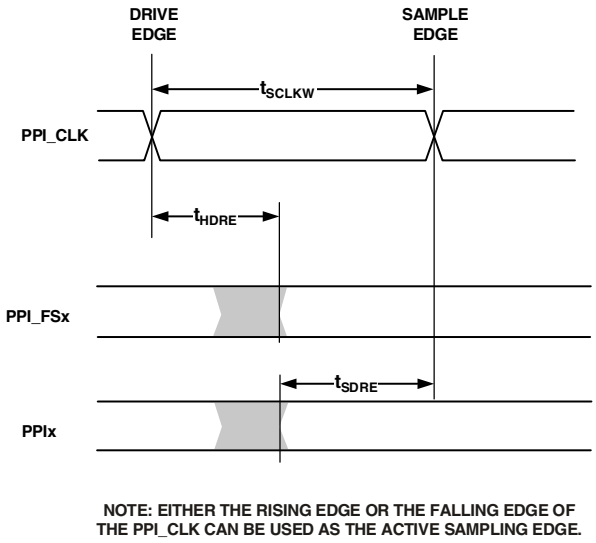


Figure 19. GP Input and Frame Capture Mode Timing

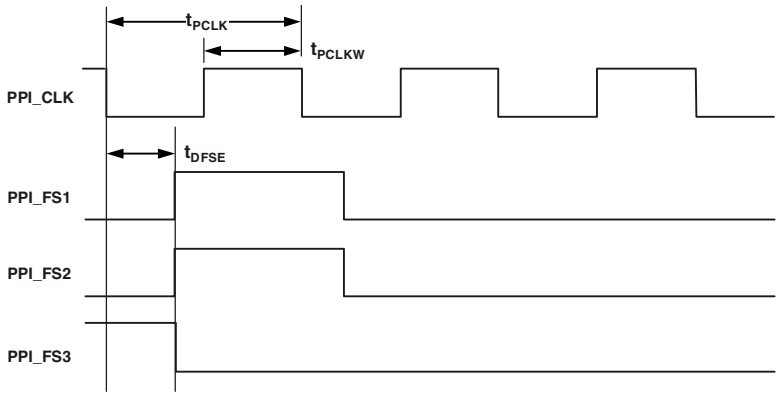


Figure 20. General Purpose Frame Capture and Output Mode Timing

Serial Ports

Table 15. Serial Ports—External Clock

Parameter		Min	Max	Unit
Timing Requirements				
t_{SFSE}	TFS/RFS Setup Before TSCLK/RSCLK[1]	3.0		ns
t_{HFSE}	TFS/RFS Hold After TSCLK/RSCLK[1]	3.0		ns
t_{SDRE}	Receive Data Setup Before RSCLK[1]	3.0		ns
t_{HDRE}	Receive Data Hold After RSCLK[1]	3.0		ns
t_{SCLKEW}	TSCLK/RSCLK Width	4.5		ns
t_{SCLKE}	TSCLK/RSCLK Period	15.0		ns

[1]Referenced to sample edge.

Table 16. Serial Ports—Internal Clock

Parameter		Min	Max	Unit
Timing Requirements				
t_{SFSI}	TFS/RFS Setup Before TSCLK/RSCLK[1]	6.0		ns
t_{HFSI}	TFS/RFS Hold After TSCLK/RSCLK[1]	0.0		ns
t_{SDRI}	Receive Data Setup Before RSCLK[1]	6.0		ns
t_{HDRI}	Receive Data Hold After RSCLK[1]	0.0		ns
t_{SCLKEW}	TSCLK/RSCLK Width	4.5		ns
t_{SCLKE}	TSCLK/RSCLK Period	15.0		ns

[1]Referenced to sample edge.

Table 17. Serial Ports—External Clock

Parameter		Min	Max	Unit
Switching Characteristics				
t_{DFSE}	TFS/RFS Delay After TSCLK/RSCLK (Internally Generated TFS/RFS)[1]		10.0	ns
t_{HOFSE}	TFS/RFS Hold After TSCLK/RSCLK (Internally Generated TFS/RFS)[1]	0.0		ns
t_{DDTE}	Transmit Data Delay After TSCLK[1]		10.0	ns
t_{HDTE}	Transmit Data Hold After TSCLK[1]	0.0		ns

[1]Referenced to drive edge.

Table 18. Serial Ports—Internal Clock

Parameter		Min	Max	Unit
Switching Characteristics				
t_{DFSI}	TFS/RFS Delay After TSCLK/RSCLK (Internally Generated TFS/RFS)[1]		4.0	ns
t_{HOFSI}	TFS/RFS Hold After TSCLK/RSCLK (Internally Generated TFS/RFS)[1]	0.0		ns
t_{DDTI}	Transmit Data Delay After TSCLK[1]		4.0	ns
t_{HDTI}	Transmit Data Hold After TSCLK[1]	0.0		ns
t_{SCLKIW}	TSCLK/RSCLK Width	4.5		ns

[1]Referenced to drive edge.

Table 19. Serial Ports—Enable and Three-State

Parameter		Min	Max	Unit
Switching Characteristics				
t_{DTENE}	Data Enable Delay from External TSCLK[1]	5.0		ns
t_{DDTTE}	Data Disable Delay from External TSCLK[1]		12.0	ns
t_{DTENI}	Data Enable Delay from Internal TSCLK	2.0		ns
t_{DDTTI}	Data Disable Delay from Internal TSCLK[1]		5.0	ns

[1]Referenced to drive edge.

Table 20. External Late Frame Sync

Parameter		Min	Max	Unit
Switching Characteristics				
$t_{DDTLFSE}$	Data Delay from Late External TFS or External RFS with MCE = 1, MFD = 0[1,2]		10.5	ns
$t_{DTENLFSE}$	Data Enable from late FS or MCE = 1, MFD = 0[1,2]	3.5		ns

[1]MCE = 1, TFS enable and TFS valid follow $t_{DDTENFS}$ and $t_{DDTLFSE}$.
[2]If external RFS/TFS setup to RSCLK/TSCLK > $t_{SCLKE}/2$ then $t_{DDTLSCK}$ and $t_{DTENLSCK}$ apply, otherwise $t_{DDTLFSE}$ and $t_{DTENLFS}$ apply.

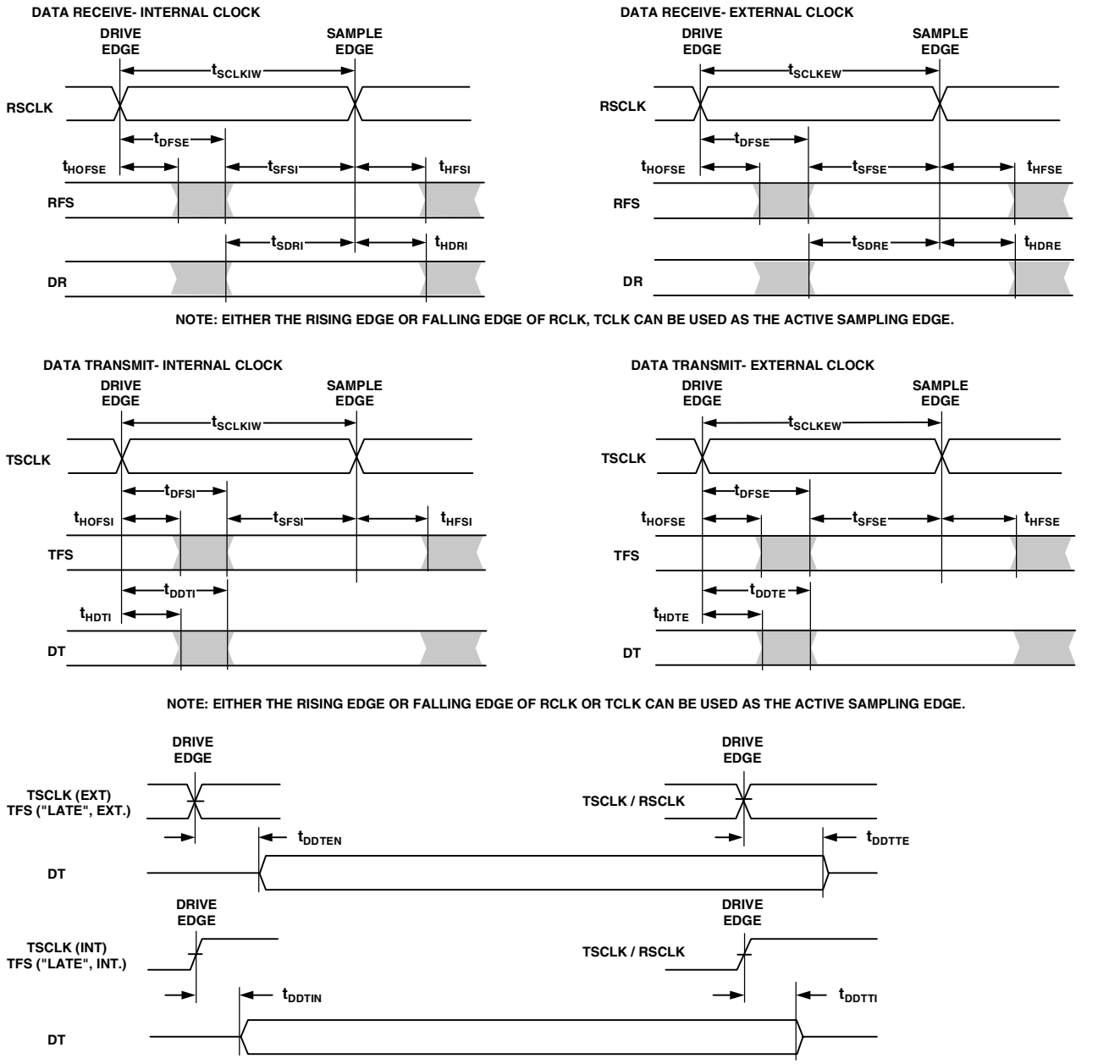
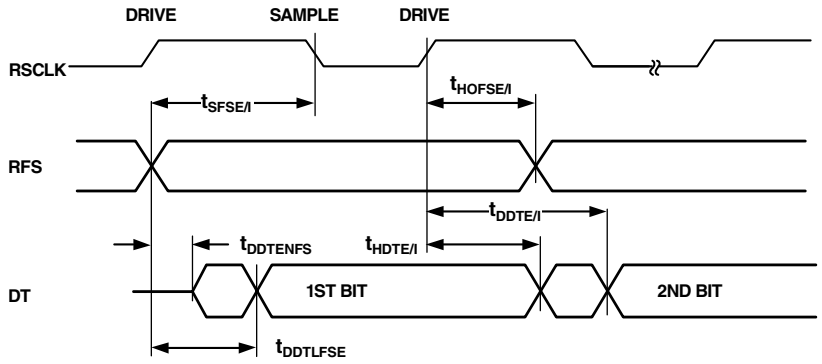


Figure 21. Serial Ports

EXTERNAL RFS WITH MCE = 1, MFD = 0



LATE EXTERNAL TFS

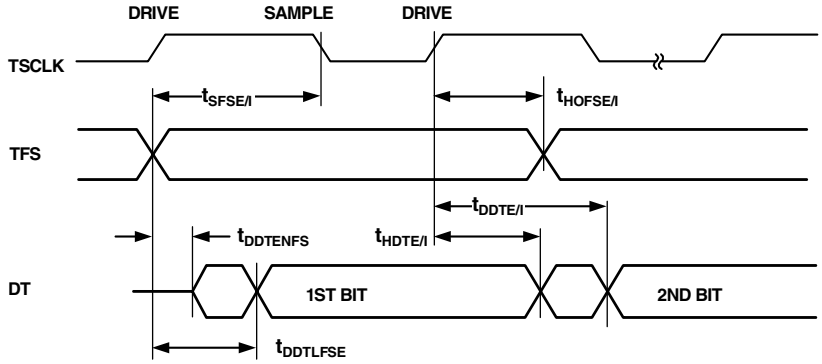


Figure 22. External Late Frame Sync (Frame Sync Setup < t_{SCLKE}/2)

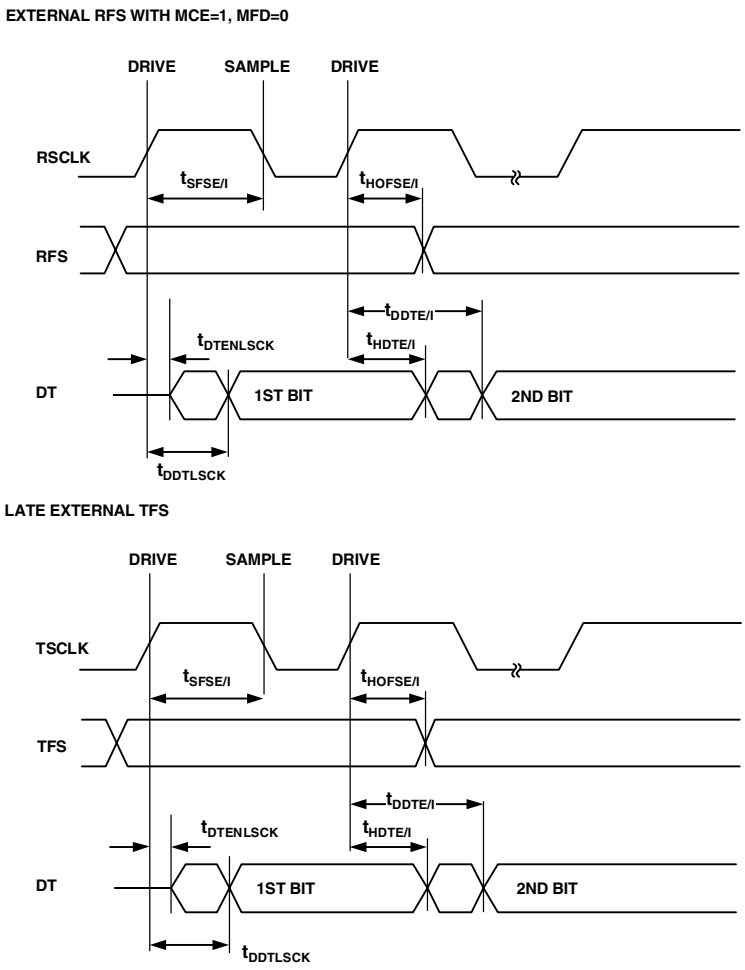


Figure 23. External Late Frame Sync (Frame Sync Setup > $t_{SCLKE}/2$)

Serial Peripheral Interface (SPI) Port—Master Timing

Table 21 and Figure 24 describe SPI port master operations.

Table 21. Serial Peripheral Interface (SPI) Port—Master Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{SSPID}	Data input valid to SCK edge (data input setup)	6.0		ns
t_{HSPID}	SCK sampling edge to data input invalid	0		ns
Switching Characteristics				
t_{SDSCIM}	$\overline{\text{SPISELx}}$ low to first SCK edge (x=0 or 1)	$2t_{SCLK}$-1.5		ns
t_{SPICHM}	Serial clock high period	$2t_{SCLK}$-1.5		ns
t_{SPICLM}	Serial clock low period	$2t_{SCLK}$-1.5		ns
t_{SPICLK}	Serial clock period	$4t_{SCLK}$-1.5		ns
t_{HDSM}	Last SCK edge to $\overline{\text{SPISELx}}$ high (x=0 or 1)	$2t_{SCLK}$-1.5		ns
t_{SPITDM}	Sequential transfer delay	$2t_{SCLK}$-1.5		ns
t_{DDSPID}	SCK edge to data out valid (data out delay)	0	6	ns
t_{HDSPID}	SCK edge to data out invalid (data out hold)	0	5	ns

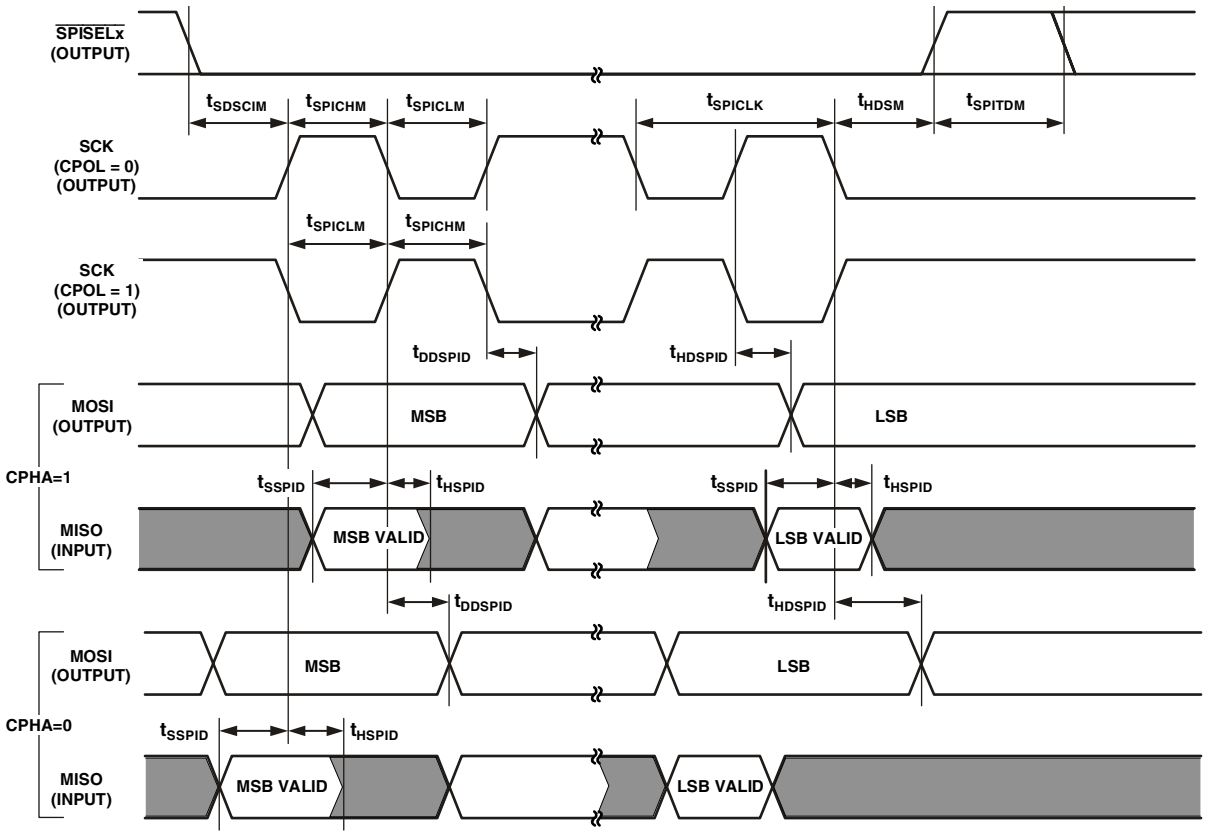


Figure 24. Serial Peripheral Interface (SPI) Port—Master Timing

Serial Peripheral Interface (SPI) Port—Slave Timing

Table 22 and Figure 25 describe SPI port slave operations.

Table 22. Serial Peripheral Interface (SPI) Port—Slave Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{SPICHS}	Serial clock high period	$2t_{SCLK}$-1.5		ns
t_{SPICLS}	Serial clock low period	$2t_{SCLK}$-1.5		ns
t_{SPICLK}	Serial clock period	$4t_{SCLK}$-1.5		ns
t_{HDS}	Last SCK edge to $\overline{\text{SPISS}}$ not asserted	$2t_{SCLK}$-1.5		ns
t_{SPITDS}	Sequential Transfer Delay	$2t_{SCLK}$-1.5		ns
t_{SDSCI}	$\overline{\text{SPISS}}$ assertion to first SCK edge	$2t_{SCLK}$-1.5		ns
t_{SSPID}	Data input valid to SCK edge (data input setup)	1.6		ns
t_{HSPID}	SCK sampling edge to data input invalid	1.6		ns
Switching Characteristics				
t_{DSOE}	$\overline{\text{SPISS}}$ assertion to data out active	0	8	ns
t_{DSDHI}	$\overline{\text{SPISS}}$ deassertion to data high impedance	0	8	ns
t_{DDSPID}	SCK edge to data out valid (data out delay)	0	10	ns
t_{HDSPID}	SCK edge to data out invalid (data out hold)	0	10	ns

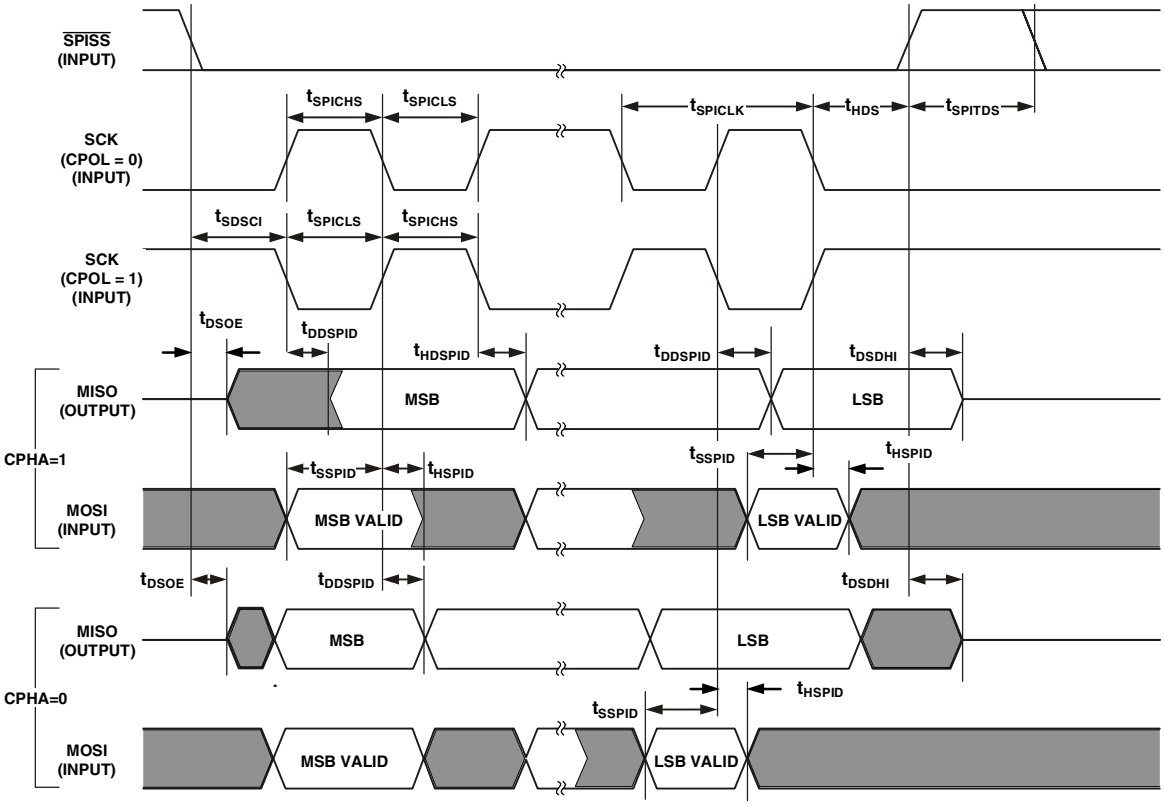


Figure 25. Serial Peripheral Interface (SPI) Port—Slave Timing

Universal Asynchronous Receiver-Transmitter (UART) Port—Receive and Transmit Timing

Figure 26 describes UART port receive and transmit operations. The maximum baud rate is SCLK/16. As shown in Figure 26 there is some latency between the generation internal UART interrupts and the external data operations. These latencies are negligible at the data transmission rates for the UART.

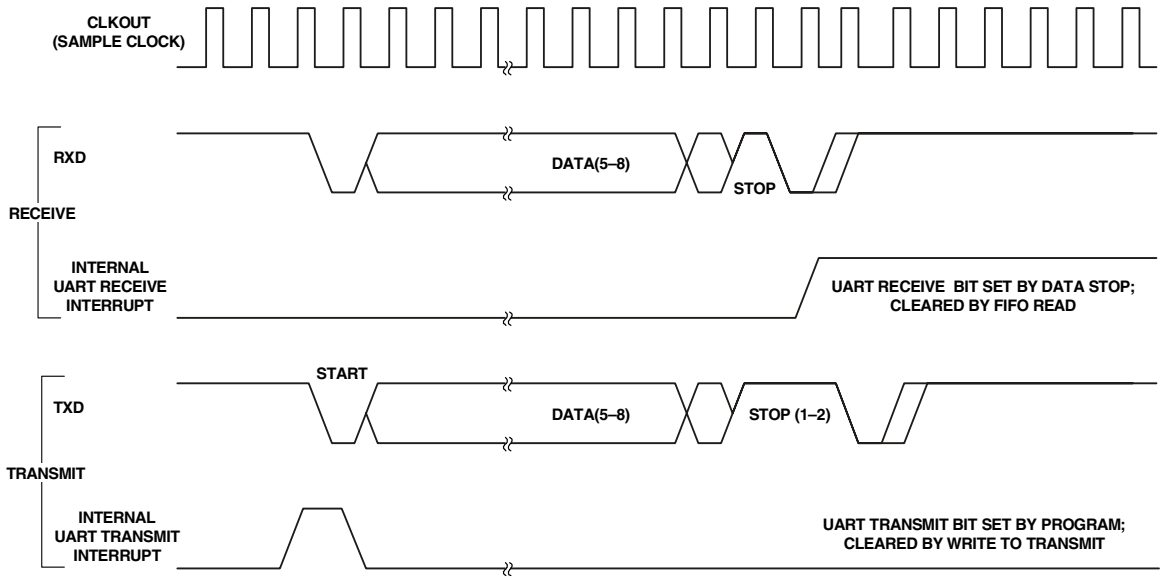


Figure 26. UART Port—Receive and Transmit Timing

Timer Cycle Timing

Table 23 and Figure 27 describe timer expired operations. The input signal is asynchronous in "width capture mode" and "external clock mode" and has an absolute maximum input frequency of $f_{SCLK}/2$ MHz.

Table 23. Timer Cycle Timing

Parameter		Min	Max	Unit
Timing Characteristics				
t_{WL}	Timer Pulsewidth Input Low[1]	1		SCLK cycles
t_{WH}	Timer Pulsewidth Input High[1]	1		SCLK cycles
Switching Characteristic				
t_{HTO}	Timer Pulsewidth Output[2]	1	$(2^{32}–1)$	SCLK cycles

[1]The minimum pulsewidths apply for TMRx input pins in width capture and external clock modes. They also apply to the PF1 or PPI_CLK input pins in PWM output mode.
[2]The minimum time for t_{HTO} is one cycle, and the maximum time for t_{HTO} equals $(2^{32}–1)$ cycles.

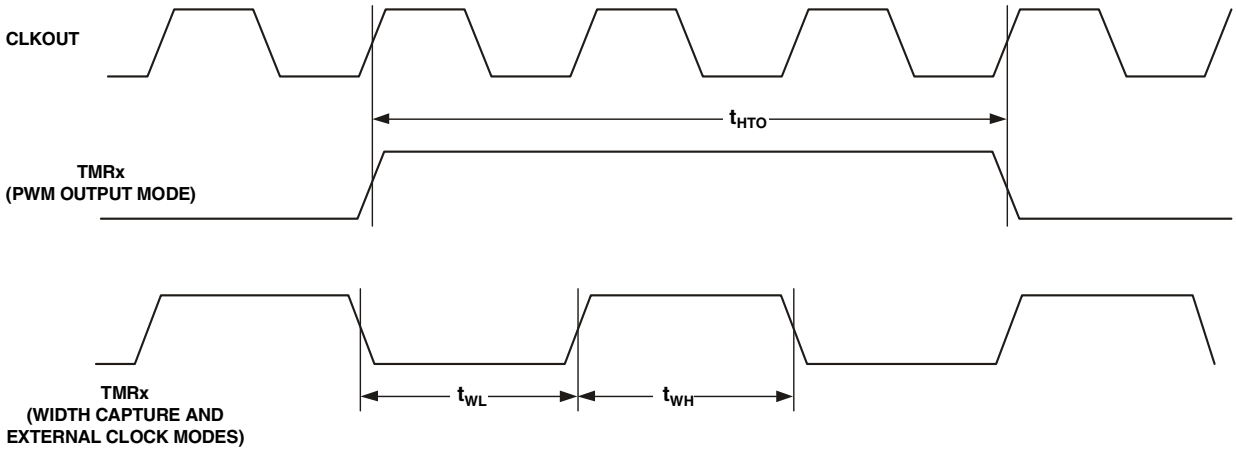


Figure 27. Timer PWM_OUT Cycle Timing

Programmable Flags Cycle Timing

Table 24 and Figure 28 describe programmable flag operations.

Table 24. Programmable Flags Cycle Timing

Parameter		Min	Max	Unit
Timing Requirement				
t_{WFI}	Flag input pulsewidth	t_{SCLK} + 1		ns
Switching Characteristic				
t_{DFO}	Flag output delay from CLKOUT low		6	ns

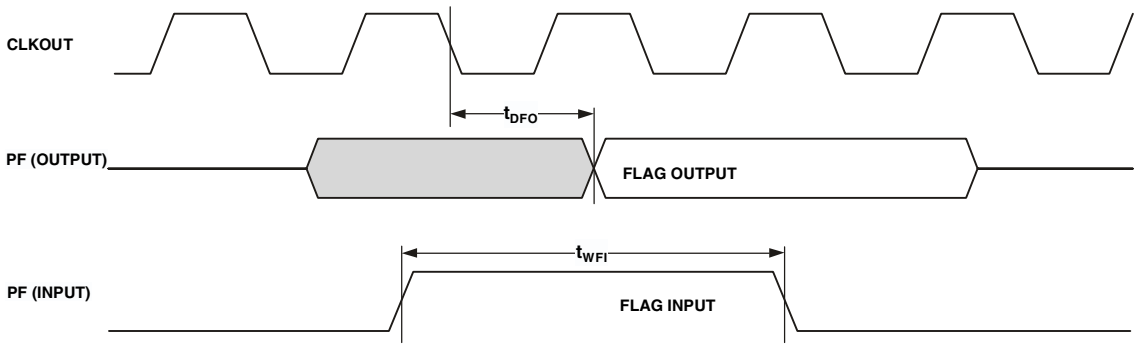


Figure 28. Programmable Flags Cycle Timing

JTAG Test And Emulation Port Timing

Table 25 and Figure 29 describe JTAG port operations.

Table 25. JTAG Port Timing

Parameter		Min	Max	Unit
Timing Parameters				
t_{TCK}	TCK Period	20		ns
t_{STAP}	TDI, TMS Setup Before TCK High	4		ns
t_{HTAP}	TDI, TMS Hold After TCK High	4		ns
t_{SSYS}	System Inputs Setup Before TCK Low[1]	4		ns
t_{HSYS}	System Inputs Hold After TCK Low[1]	5		ns
t_{TRSTW}	$\overline{\text{TRST}}$ Pulsewidth[2]	4		TCK cycles
Switching Characteristics				
t_{DTDO}	TDO Delay from TCK Low		10	ns
t_{DSYS}	System Outputs Delay After TCK Low[3]	0	12	ns

[1] System Inputs=DATA15-0, ARDY, TMR2-0, PF15-0, PPI_CLK, RSCLK0-1, RFS0-1, DR0PRI, DR0SEC, TSCLK0-1, TFS0-1, DR1PRI, DR1SEC, MOSI, MISO, SCK, RX, $\overline{\text{RESET}}$, NMI, BMODE1-0, $\overline{\text{BR}}$, PP3-0.
[2] 50 MHz max.
[3] System Outputs=DATA15-0, ADDR19-1, $\overline{\text{ABE1-0}}$, $\overline{\text{AOE}}$, $\overline{\text{ARE}}$, $\overline{\text{AWE}}$, $\overline{\text{AMS3-0}}$, $\overline{\text{SRAS}}$, $\overline{\text{SCAS}}$, $\overline{\text{SWE}}$, SCKE, CLKOUT, SA10, $\overline{\text{SMS}}$, TMR2-0, PF15-0, RSCLK0-1, RFS0-1, TSCLK0-1, TFS0-1, DT0PRI, DT0SEC, DT1PRI, DT1SEC, MOSI, MISO, SCK, TX, $\overline{\text{BG}}$, $\overline{\text{BGH}}$, PPI3-0.

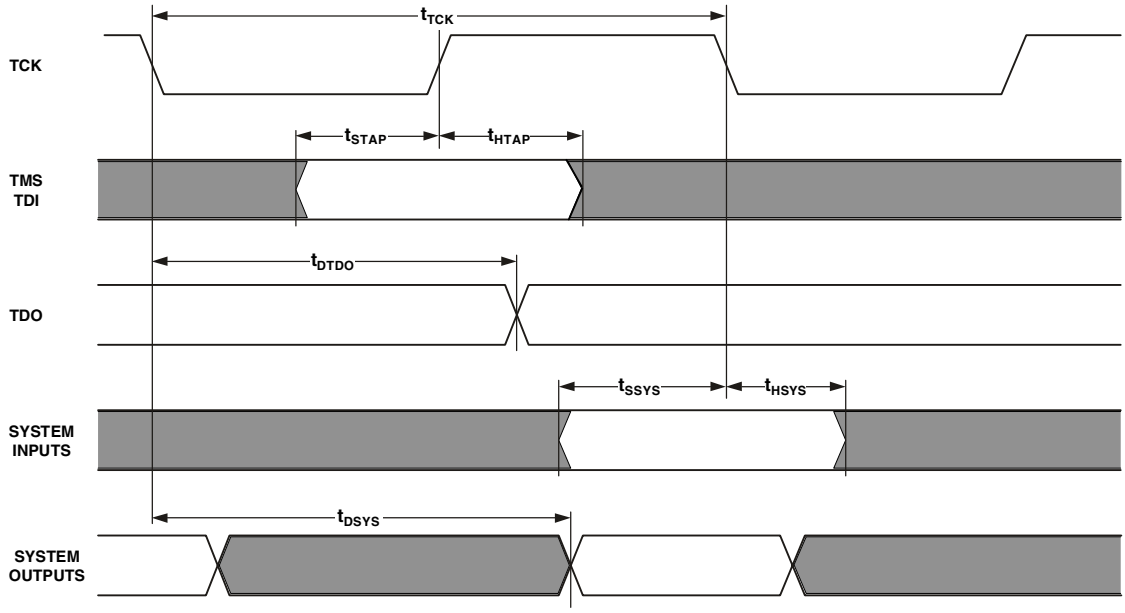


Figure 29. JTAG Port Timing

ADSP-21532 160-LEAD BGA PINOUT

Table 26 lists the BGA pinout by signal name. Table 27 on page 38 lists the pinout by lead number.

Table 26. 160-Lead BGA Lead Assignment (Alphabetically by Signal)

Signal	Lead Number	Signal	Lead Number	Signal	Lead Number	Signal	Lead Number
$\overline{\text{ABE0}}$	H13	DATA12	M5	GND	L6	SCK	D1
$\overline{\text{ABE1}}$	H12	DATA13	N5	GND	L8	SCKE	B13
ADDR1	J14	DATA14	P5	GND	L10	$\overline{\text{SMS}}$	C13
ADDR10	M13	DATA15	P4	GND	M4	$\overline{\text{SRAS}}$	D13
ADDR11	M14	DATA2	P9	GND	M10	$\overline{\text{SWE}}$	D12
ADDR12	N14	DATA3	M8	GND	P14	TCK	P2
ADDR13	N13	DATA4	N8	MISO	E2	TDI	M3
ADDR14	N12	DATA5	P8	MOSI	D3	TDO	N3
ADDR15	M11	DATA6	M7	NMI	B10	TFS0	H3
ADDR16	N11	DATA7	N7	PF0	D2	TFS1	E1
ADDR17	P13	DATA8	P7	PF1	C1	TMR0	L2
ADDR18	P12	DATA9	M6	PF10	A4	TMR1	M1
ADDR19	P11	DR0PRI	K1	PF11	A5	TMR2	K2
ADDR2	K14	DR0SEC	J2	PF12	B5	TMS	N2
ADDR3	L14	DR1PRI	G3	PF13	B6	$\overline{\text{TRST}}$	N1
ADDR4	J13	DR1SEC	F3	PF14	A6	TSCLK0	J1
ADDR5	K13	DT0PRI	H1	PF15	C6	TSCLK1	F1
ADDR6	L13	DT0SEC	H2	PF2	C2	TX	K3
ADDR7	K12	DT1PRI	F2	PF3	C3	VDDEXT	A1
ADDR8	L12	DT1SEC	E3	PF4	B1	VDDEXT	C7
ADDR9	M12	$\overline{\text{EMU}}$	M2	PF5	B2	VDDEXT	C12
$\overline{\text{AMS0}}$	E14	GND	A10	PF6	B3	VDDEXT	D5
$\overline{\text{AMS1}}$	F14	GND	A14	PF7	B4	VDDEXT	D9
$\overline{\text{AMS2}}$	F13	GND	B11	PF8	A2	VDDEXT	F12
$\overline{\text{AMS3}}$	G12	GND	C4	PF9	A3	VDDEXT	G4
$\overline{\text{AOE}}$	G13	GND	C5	PPI0	C8	VDDEXT	J4
ARDY	E13	GND	C11	PPI1	B8	VDDEXT	J12
$\overline{\text{ARE}}$	G14	GND	D4	PPI2	A7	VDDEXT	L7
$\overline{\text{AWE}}$	H14	GND	D7	PPI3	B7	VDDEXT	L11
$\overline{\text{BG}}$	P10	GND	D8	PPI_CLK	C9	VDDEXT	P1
$\overline{\text{BGH}}$	N10	GND	D10	$\overline{\text{RESET}}$	C10	VDDINT	D6
BMODE0	N4	GND	D11	RFS0	J3	VDDINT	E4
BMODE1	P3	GND	F4	RFS1	G2	VDDINT	E11
$\overline{\text{BR}}$	D14	GND	F11	RSCLK0	L1	VDDINT	J11
CLKIN	A12	GND	G11	RSCLK1	G1	VDDINT	L4
CLKOUT	B14	GND	H4	RTXI	A9	VDDINT	L9
DATA0	M9	GND	H11	RTXO	A8	VDDRTC	B9
DATA1	N9	GND	K4	RX	L3	VROUT	A13
DATA10	N6	GND	K11	SA10	E12	VROUT	B12
DATA11	P6	GND	L5	$\overline{\text{SCAS}}$	C14	XTAL	A11

Table 27. 160-Lead BGA Lead Assignment (Numerically by Lead Number)

Lead Number	Signal	Lead Number	Signal	Lead Number	Signal	Lead Number	Signal
A1	VDDEXT	C13	$\overline{SMS}$	H1	DT0PRI	M3	TDI
A2	PF8	C14	$\overline{SCAS}$	H2	DT0SEC	M4	GND
A3	PF9	D1	SCK	H3	TFS0	M5	DATA12
A4	PF10	D2	PF0	H4	GND	M6	DATA9
A5	PF11	D3	MOSI	H11	GND	M7	DATA6
A6	PF14	D4	GND	H12	$\overline{ABE1}$	M8	DATA3
A7	PPI2	D5	VDDEXT	H13	$\overline{ABE0}$	M9	DATA0
A8	RTXO	D6	VDDINT	H14	$\overline{AWE}$	M10	GND
A9	RTXI	D7	GND	J1	TSCLK0	M11	ADDR15
A10	GND	D8	GND	J2	DR0SEC	M12	ADDR9
A11	XTAL	D9	VDDEXT	J3	RFS0	M13	ADDR10
A12	CLKIN	D10	GND	J4	VDDEXT	M14	ADDR11
A13	VROUT	D11	GND	J11	VDDINT	N1	$\overline{TRST}$
A14	GND	D12	$\overline{SWE}$	J12	VDDEXT	N2	TMS
B1	PF4	D13	$\overline{SRAS}$	J13	ADDR4	N3	TDO
B2	PF5	D14	$\overline{BR}$	J14	ADDR1	N4	BMODE0
B3	PF6	E1	TFS1	K1	DR0PRI	N5	DATA13
B4	PF7	E2	MISO	K2	TMR2	N6	DATA10
B5	PF12	E3	DT1SEC	K3	TX	N7	DATA7
B6	PF13	E4	VDDINT	K4	GND	N8	DATA4
B7	PPI3	E11	VDDINT	K11	GND	N9	DATA1
B8	PPI1	E12	SA10	K12	ADDR7	N10	$\overline{BGH}$
B9	VDDRTC	E13	$\overline{ARDY}$	K13	ADDR5	N11	ADDR16
B10	NMI	E14	$\overline{AMS0}$	K14	ADDR2	N12	ADDR14
B11	GND	F1	TSCLK1	L1	RSCLK0	N13	ADDR13
B12	VROUT	F2	DT1PRI	L2	TMR0	N14	ADDR12
B13	SCKE	F3	DR1SEC	L3	RX	P1	VDDEXT
B14	CLKOUT	F4	GND	L4	VDDINT	P2	TCK
C1	PF1	F11	GND	L5	GND	P3	BMODE1
C2	PF2	F12	VDDEXT	L6	GND	P4	DATA15
C3	PF3	F13	$\overline{AMS2}$	L7	VDDEXT	P5	DATA14
C4	GND	F14	$\overline{AMS1}$	L8	GND	P6	DATA11
C5	GND	G1	RSCLK1	L9	VDDINT	P7	DATA8
C6	PF15	G2	RFS1	L10	GND	P8	DATA5
C7	VDDEXT	G3	DR1PRI	L11	VDDEXT	P9	DATA2
C8	PPI0	G4	VDDEXT	L12	ADDR8	P10	$\overline{BG}$
C9	PPI_CLK	G11	GND	L13	ADDR6	P11	ADDR19
C10	$\overline{RESET}$	G12	$\overline{AMS3}$	L14	ADDR3	P12	ADDR18
C11	GND	G13	$\overline{AOE}$	M1	TMR1	P13	ADDR17
C12	VDDEXT	G14	$\overline{ARE}$	M2	$\overline{EMU}$	P14	GND

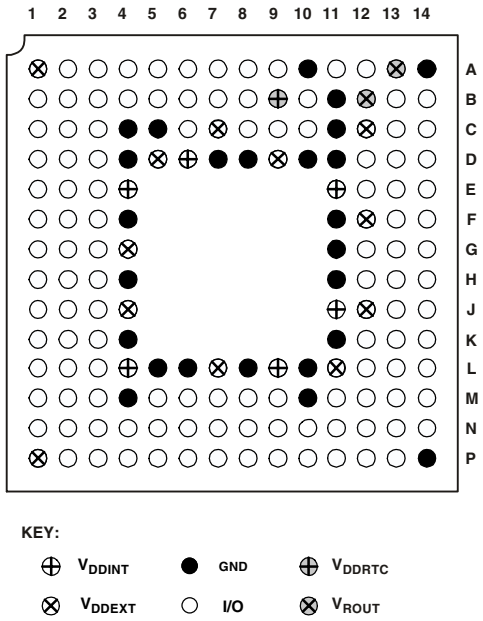


Figure 30. 160-Ball Metric BGA Pin Configuration (Top View)

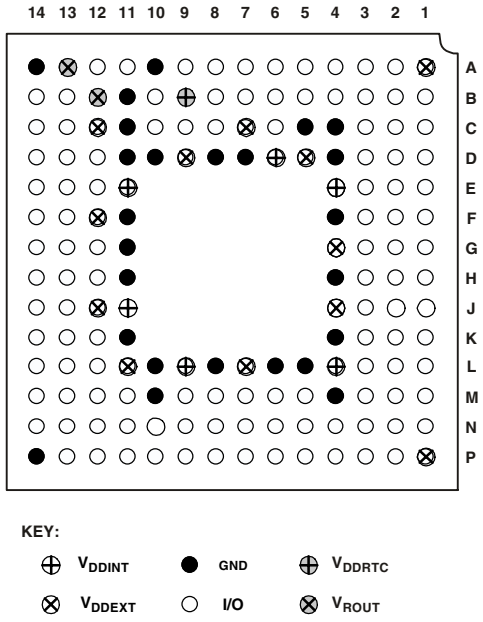
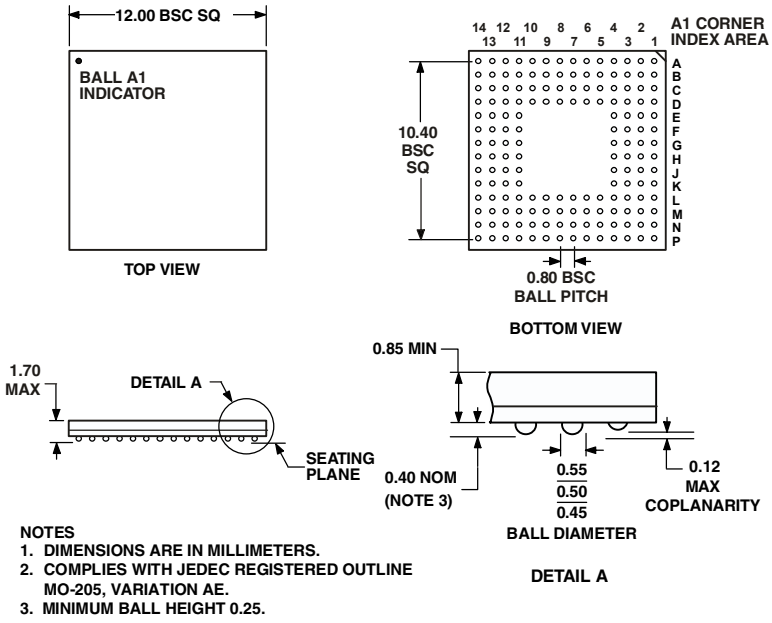


Figure 31. 160-Ball Metric BGA Pin Configuration (Bottom View)

OUTLINE DIMENSIONS

Dimensions in the outline dimension figure on page 40 are shown in millimeters.

160-LEAD METRIC PLASTIC BALL GRID ARRAY (MINI-BGA) (BC-160)



ORDERING GUIDE

Table 28.

Part Number	Case Temperature Range	Instruction Rate	Operating Voltage
ADSP-21532SBBC-300	–40°C to 105°C	300 MHz	On-chip voltage regulation from 2.25 V to 3.6 V input