1.1 Scope.

This specification covers the detail requirements for a CMOS monolithic 32-bit and 64-bit IEEE Standard 754 format floating-point multiplier.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
−1	ADSP-3210SG/883B
−2	ADSP-3210TG/883B
−3	ADSP-3210UG/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline: G-100A.

1.3 Absolute Maximum Ratings.

Supply Voltage	−0.3V to 7V
Input Voltage	−0.3V to V_{DD}
Output Voltage	−0.3V to V_{DD}
Operating Temperature Range (Ambient)	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering 10sec)	+300°C

1.5 Thermal Characteristics.

Maximum Thermal Resistance θ_{JC}: see MIL-M-38510, Appendix C.

ADSP-3210 – SPECIFICATIONS

Parameter	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 9	Sub Group 10, 11	Test Condition[1]	Units
Digital Input High Voltage	V_{IH}	–1, 2, 3	2.0	2.0	2.0			V_{DD} = max	V min
Digital Input High Voltage, CLK and Asynchronous Controls (RESET, MSWSEL, OEN)	V_{IHA}	–1, 2, 3	3.0	3.0	3.0			V_{DD} = max	V min
Digital Input Low Voltage	V_{IL}	–1, 2, 3	0.8	0.8	0.8			V_{DD} = min	V max
Digital Output High Voltage	V_{OH}	–1, 2, 3	2.4	2.4	2.4			V_{DD} = min I_{OH} = –1mA	V min
Digital Output Low Voltage*	V_{OL}	–1, 2, 3	0.4	0.6	0.6			V_{DD} = min I_{OL} = +4mA	V max
Digital Input High Current	I_{IH}	–1, 2, 3	10	10	10			V_{DD} = max V_{IN} = +5.0V	µA max
Digital Input Low Current	I_{IL}	–1, 2, 3	10	10	10			V_{DD} = max V_{IN} = 0.0V	µA max
Three-State Leakage Current	I_{OZ}	–1, 2, 3	50	50	50			V_{DD} = max High Z, V_{IN} = 0V or max	µA max
Supply Current	I_{DD1}	–1	150	200	200			@ max Clock Rate, TTL Inputs	mA max
	I_{DD2}	–2, 3	50	60	60			All V_{IN} = 2.4V	mA max
Clock Cycle	t_{CY}	–1	125			150	150	Note 2	ns max
		–2	100			125	125		
		–3	60			75	75		
Clock LO	t_{CL}	–1, 2, 3	20			30	30	Note 2	ns min
Clock HI	t_{CH}	–1, 2, 3	20			30	30	Note 2	ns min
Data & Control Setup	t_{DS}	–1	20			25	25	Note 2	ns min
		–2, 3	15			20	20		
Data & Control Hold	t_{DH}	–1, 2, 3	3			3	3	Note 2	ns min
Data Output Delay	t_{DO}	–1	30			35	35	Note 2	ns max
		–2, 3	25			30	30		
Status Output Delay	t_{SO}	–1	30			35	35	Note 2	ns max
		–2, 3	25			30	30		
MSWSEL-to-Data Delay	t_{ENO}	–1	25			30	30	Note 2	ns max
		–2, 3	20			25	25		
Three-State Disable Delay*	t_{DIS}	–1	18			25	25	Notes 2 & 3	ns max
		–2, 3	15			20	20		
Three-State Enable Delay*	t_{ENA}	–1	25			30	30	Notes 2, 3 & 4	ns max
		–2, 3	20			25	25		
RESET Setup*	t_{SU}	–1	20			25	25	Note 2	ns min
		–2, 3	15			25	25		
RESET Pulse Duration*	t_{RS}	–1, 2, 3	50			75	75	Note 2	ns min

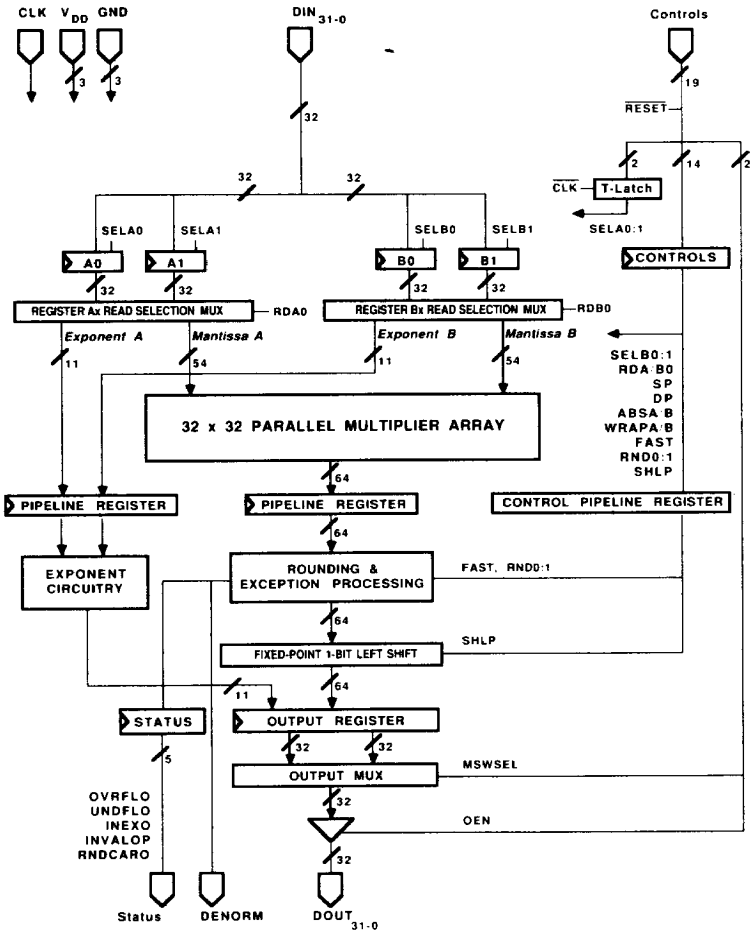
Table 1. (Continued on next page)

Parameter	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 9	Sub Group 10, 11	Test Condition[1]	Units
Operation Time (With or Without Direct Operand Feed):	t_{OPD}								
32-Bit Multiplication		−1	125			150	150	Note 2	ns max
		−2	100			125	125		
		−3	60			75	75		
64-Bit Multiplication		−1	500			600	600	Note 2	ns max
		−2	400			500	500		
		−3	240			300	300		
Hold Setup	t_{HS}	−1	20			22	22	Note 2	ns min
		−2, 3	15			18	18		
Hold Hold	t_{HH}	−1, 2, 3	3			3	3	Note 2	ns min
Total Latency[5] (With Direct Operand Feed):	t_{LAD}								
32-Bit Multiplication		−1	363			435	435	Note 2	ns max
		−2	290			363	363		
		−3	190			238	238		
64-Bit Multiplication		−1	738			885	885	Note 2	ns max
		−2	590			738	738		
		−3	370			463	463		

NOTES
*Indicates that a limit for this parameter has changed from REV. A.
[1]T_A = +25°C; V_{DD} = +4.5V min to +5.5V max (unless otherwise noted).
[2]Input levels are GND and +3.0V; V_{DD} = +4.5V, and timing transitions per Figures 1 through 7, measured at +1.5V.
[3]Transitions measured per Figure 1.
[4]3ns min.
[5]Total latency = (data setup + processing + output delay of MSW) in Direct Operand Feed Mode.

Table 1.

3.2.1 Functional Block Diagram and Terminal Assignments.



Pin Assignments

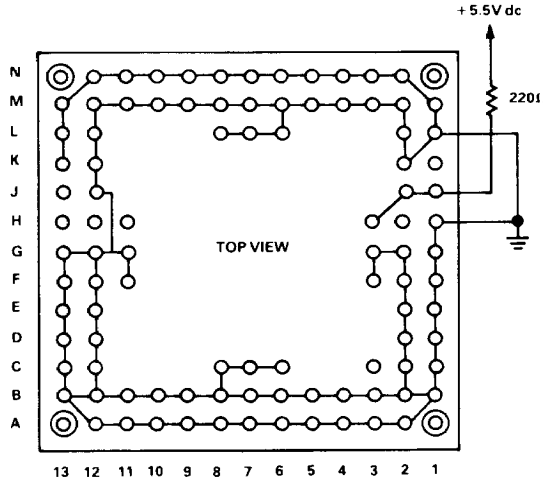
PIN	FUNCTION	PIN	FUNCTION
B2	DIN3	M12	DOUT28
B1	DIN2	M13	DOUT29
C2	DIN1	L12	DOUT30
C1	DIN0	L13	DOUT31
D2	WRAPB	K12	GND
D1	RDB0	K13	GND
E2	SELB0	J12	GND
E1	SELB1	J13	DENORM
F3	ABSB	H11	INVALOP
F2	DP	H12	OVRFLO
F1	SP	H13	UNDFLO
G2	CLK	G12	OEN
G3	RESET	G11	MSWSEL
G1	RND1	G13	SHLP
H1	RND0	F13	FAST
H2	RNDCARO	F12	ABSA
H3	VDD	F11	SELA1
J1	VDD	E13	SELA0
J2	VDD	E12	RDA0
K1	INEXO	D13	WRAPA
K2	DOUT0	D12	DIN31
L1	DOUT1	C13	DIN30
M1	DOUT2	B13	DIN29
L2	DOUT3	C12	DIN28
N1	N/C	A13	N/C
M2	DOUT4	B12	DIN27
N2	DOUT5	A12	DIN26
M3	DOUT6	B11	DIN25
N3	DOUT7	A11	DIN24
M4	DOUT8	B10	DIN23
N4	DOUT9	A10	DIN22
M5	DOUT10	B9	DIN21
N5	DOUT11	A9	DIN20
L6	DOUT12	C8	DIN19
M6	DOUT13	B8	DIN18
N6	DOUT14	A8	DIN17
M7	DOUT15	B7	DIN16
L7	DOUT16	C7	DIN15
N7	DOUT17	A7	DIN14
N8	DOUT18	A6	DIN13
M8	DOUT19	B6	DIN12
L8	DOUT20	C6	DIN11
N9	DOUT21	A5	DIN10
M9	DOUT22	B5	DIN9
N10	DOUT23	A4	DIN8
M10	DOUT24	B4	DIN7
N11	DOUT25	A3	DIN6
N12	DOUT26	A2	DIN5
M11	DOUT27	B3	DIN4
N13	N/C	A1	N/C

3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (105).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



REV. B

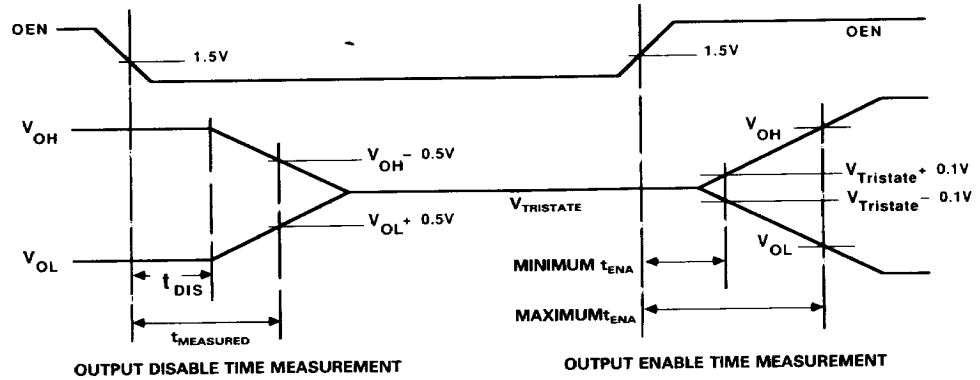


Figure 1. ADSP-3210 Three-State Disable and Enable Timing

Output disable time, t_{DIS}, is measured from the time the output enable control signal reaches 1.5 V to the time when all outputs have ceased driving. This is calculated by measuring the time, $t_{MEASURED}$, from the same starting point to when the output voltages have changed by 0.5 V toward +1.5 V. From the tester capacitive loading, C_L, and the measured current, i_L, the decay time, t_{DECAY}, can be approximated to first order by:

$$t_{DECAY} = \frac{C_L \cdot 0.5\ V}{i_L}$$

from which

$$t_{DIS} = t_{MEASURED} - t_{DECAY}$$

is calculated. Disable times are longest at the highest specified temperature.

The minimum output enable time, minimum t_{ENA}, is the earlist that outputs begin to drive. It is measured from the control signal OEN reaching 1.5 V to the point at which the fastest outputs have changed by 0.1 V from $V_{TRISTATE}$ toward their final output voltages. Minimum enable times are shortest at the lowest specified temperature.

The maximum output enable time, maximum t_{ENA}, is also measured from output enable control signal at 1.5 V to the time when all outputs have reached TTL input levels (V_{OH} or V_{OL}). This could also be considered as "data valid." Maximum enable times are longest at the highest specified temperature.

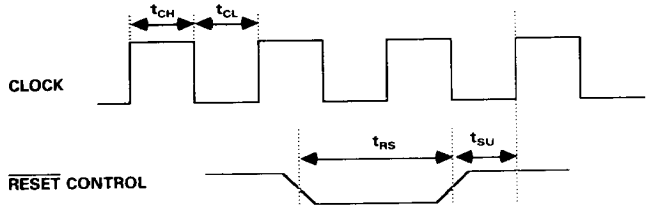


Figure 2. ADSP-3210 Reset Timing

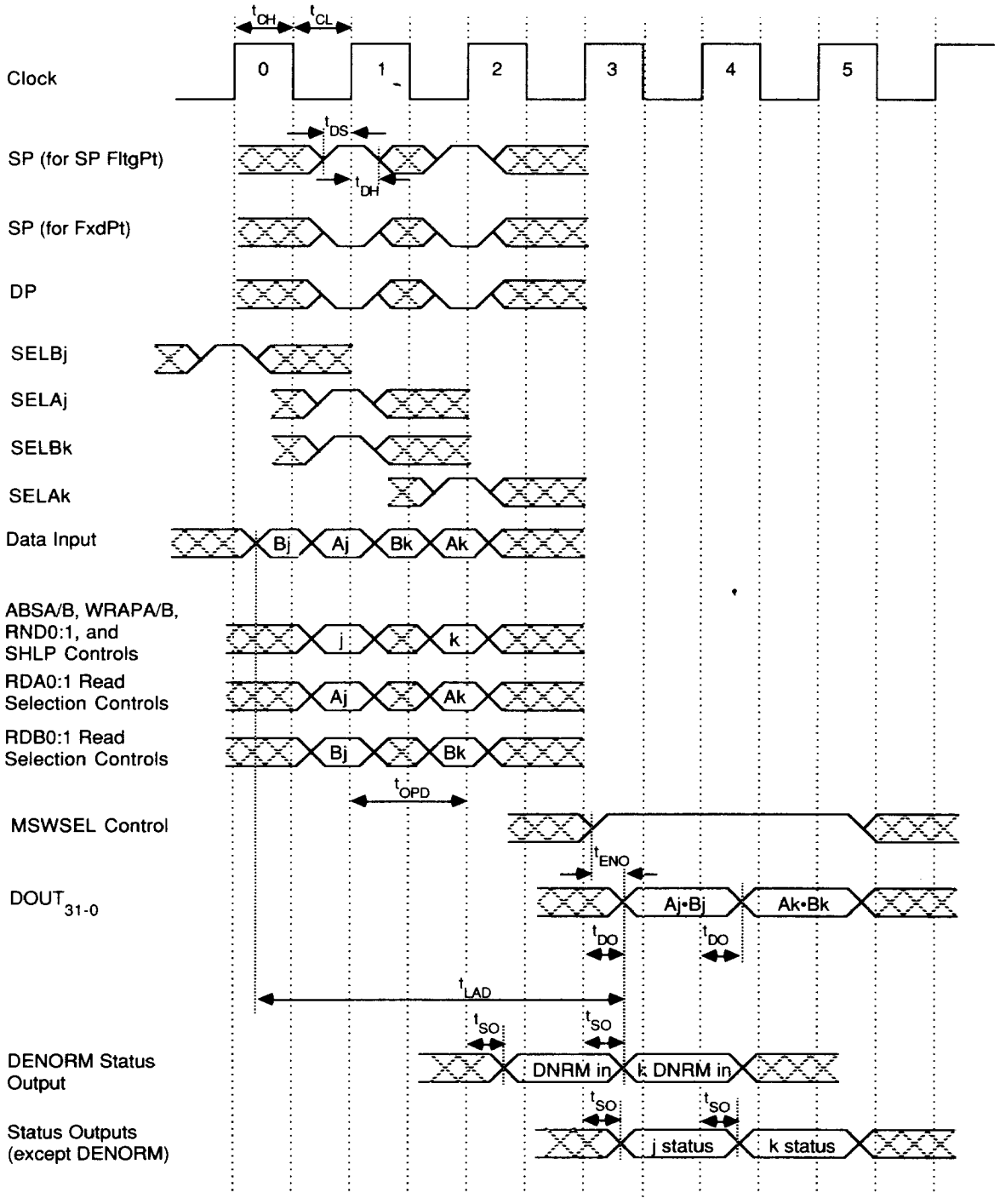


Figure 3. ADSP-3210 32-Bit Single-Precision Floating-Point and Fixed-Point Multiplications

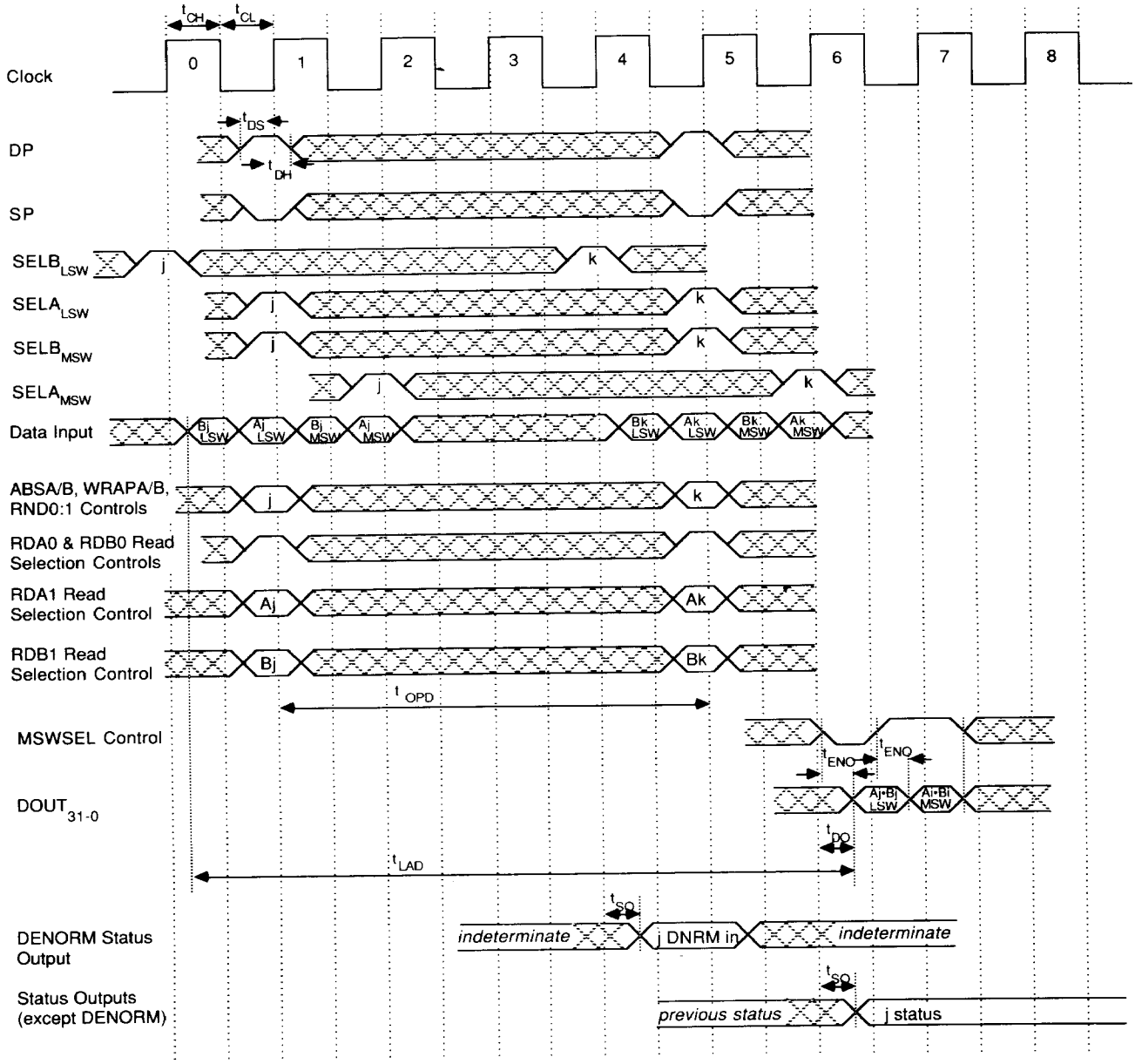


Figure 4. ADSP-3210 64-Bit Double-Precision Floating-Point Multiplications

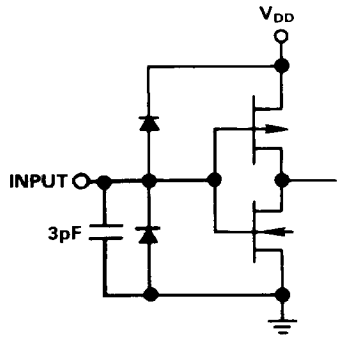


Figure 5. Equivalent Input Circuits

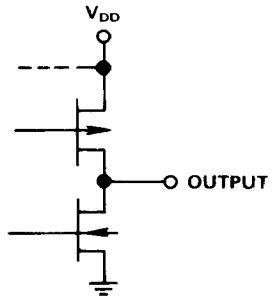


Figure 6. Equivalent Output Circuits

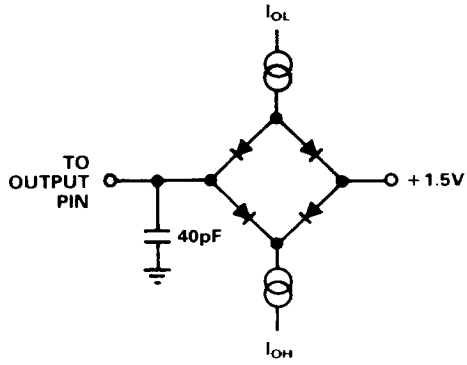


Figure 7. Normal Load for AC Measurements

INSTRUCTION	WRAPA	WRAPB	COMMENT
A*B	0	0	Multiply Normalized Floating Point Operands A Times B.
WA*B	1	0	Multiply Wrapped Operand A Times Operand B.
A*WB	0	1	Multiply Operand A Times Wrapped Operand B.
WA*WB	1	1	Multiply Wrapped Operand A Times Wrapped Operand B.

Table 2. ADSP-3210 Instruction Set

5.0 Notation Used in the Tables Below:

RN = Round to the Nearest Number
RP = Round toward Plus Infinity
RM = Round toward Minus Infinity
RZ = Round toward Zero

NORM = Normalized number
DNRM = Denormalized number. A Denormalized number is treated as zero internally.
WNRM = Wrapped number. A wrapped number is a number with a normalized fraction and an exponent that has been decremented through zero to take on a twos complement negative value.

UNRM = Unnormalized number. An Unnormal is an Underflowed and Wrapped Number. An UNRM can result from a multiplication of 1 or 2 Wrapped Numbers.
NORM.MAX = Maximum Normalized Number Representable in the Destination Format
NORM.MIN = Minimum Normalized Number Representable in the Destination Format
OVF = Overflowed Number
UNDF = Underflowed Number
INV = Invalid Operand
INF = Infinity
OK = No Exception Status Generated

In the tables below, the first mnemonic in each box describes the flag that is set, the second is the result on the DOUT pins.

A operand \ B operand	ZERO		DNRM		WRAP		NORM		INF		NAN	
	result	*status*	*result*	*status*	*result*	*status*	*result*	*status*	*result*	*status*	*result*	*status*
ZERO	ZERO		ZERO		ZERO		ZERO		NAN	INVALOP	NAN	INVALOP
DNRM	ZERO		ZERO	DENORM	ZERO	DENORM	ZERO	DENORM	INF		NAN	INVALOP
WRAP	ZERO		ZERO	DENORM	UNRM	UNDFLO	NORM WRAP UNRM	 UNDFLO UNDFLO	INF		NAN	INVALOP
NORM	ZERO		ZERO	DENORM	NORM WRAP UNRM	 UNDFLO UNDFLO	INF,NORM,MAX[1] NORM WRAP	OVRFLO UNDFLO	INF		NAN	INVALOP
INF	NAN	INVALOP	INF		INF		INF		INF		NAN	INVALOP
NAN	NAN	INVALOP	NAN	INVALOP	NAN	INVALOP	NAN	INVALOP	NAN	INVALOP	NAN	INVALOP

1. Either INF or NORM.MAX, depending on rounding mode. See "Round Controls."

Table 3. ADSP-3210 Floating-Point Multiplication (IEEE Mode)

A operand \ B operand	ZERO		DNRM		NORM		INF		NAN	
	result	*status*	*result*	*status*	*result*	*status*	*result*	*status*	*result*	*status*
ZERO	ZERO		ZERO		ZERO		NAN	INVALOP	NAN	INVALOP
DNRM	ZERO		ZERO	DENORM	ZERO	DENORM	NAN	INVALOP	NAN	INVALOP
NORM	ZERO		ZERO	DENORM	INF,NORM,MAX[1] NORM ZERO	OVRFLO UNDFLO	INF		NAN	INVALOP
INF	NAN	INVALOP	INF	INVALOP	INF		INF		NAN	INVALOP
NAN	NAN	INVALOP	NAN	INVALOP	NAN	INVALOP	NAN	INVALOP	NAN	INVALOP

1. Either INF or NORM.MAX, depending on rounding mode. See "Round Controls."
2. In FAST mode, WRAP inputs are illegal.

Table 4. ADSP-3210 Floating-Point Multiplication (FAST Mode)