CMOS 170 MHz True-Color Graphics 10-Bit Video RAM-DACs

ADV7150/ADV7152

T-52-33-43

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FEATURES

170 MHz Pipelined Operation
Triple 10-Bit D/A Converters
Triple 256 × 10 (256 × 30) Color Palette RAM
On-Chip Clock Control Circuit
Palette Priority Select Registers
RS-343A/RS-170 Compatible Analog Outputs
TTL Compatible Digital Inputs
Standard MPU I/O Interface
  10-Bit Parallel Structure
  8+2 Byte Structure
Pixel Data Serializer
  Multiplexed Pixel Input Ports; 1:1, 2:1, 4:1 (ADV7150)
  Multiplexed Pixel Input Ports; 1:1, 2:1 (ADV7152)
+5 V CMOS Monolithic Construction
160-Pin PQFP (ADV7150)
100-Pin PQFP (ADV7152)

SPEED GRADES

170 MHz
135 MHz
110 MHz
85 MHz

MODES FOR ALL SPEED GRADES

24-Bit True Color
Three 8-Bit Pseudo-Color Modes
  On Red Pixel Port
  On Green Pixel Port
  On Blue Pixel Port

15-Bit True Color
  5 Bits Red, 5 Bits Green and 5 Bits Blue
  8 Bits Red and 7 Bits Green

GENERAL DESCRIPTION

The ADV7150/ADV7152 (ADV®) is a complete analog output, Video RAM-DAC on a single CMOS monolithic chip. The part is specifically designed for use in the graphics systems of high performance, color graphics workstations. The ADV7150/ADV7152 integrates a number of graphic functions onto one device allowing 24-bit direct True-Color operation at the maximum screen update rate of 170 MHz. It can also be used in other modes, including 15-bit true color and 8-bit pseudo or indexed color. Either the RED, GREEN or BLUE input pixel ports can be used for pseudo color.

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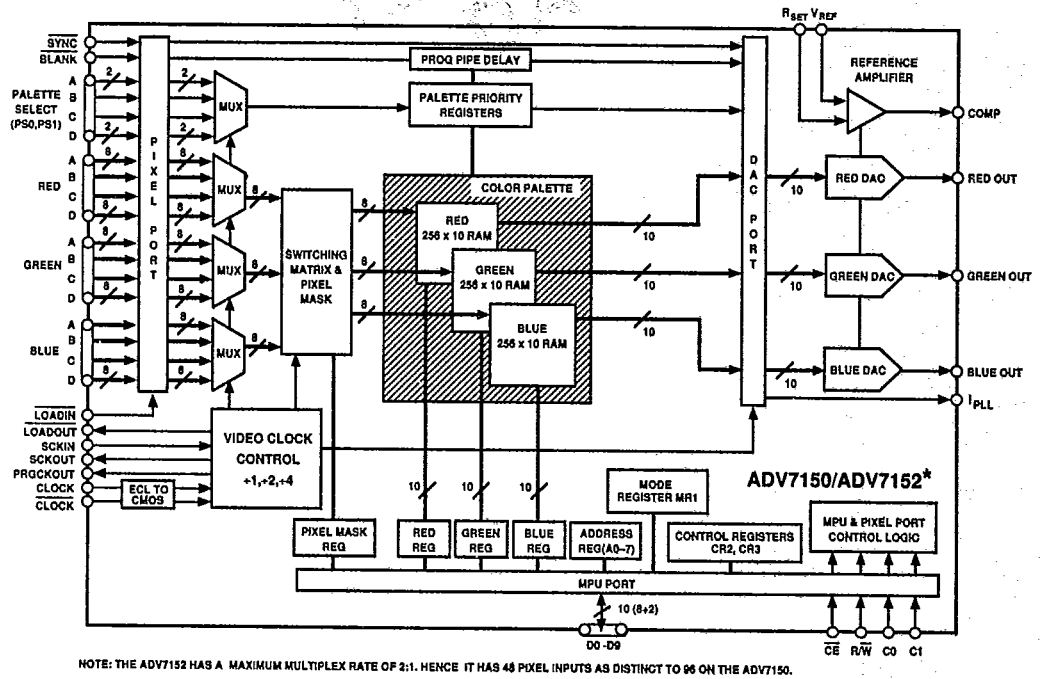
FUNCTIONAL BLOCK DIAGRAM



NOTE: THE ADV7152 HAS A MAXIMUM MULTIPLEX RATE OF 2:1. HENCE IT HAS 48 PIXEL INPUTS AS DISTINCT TO 96 ON THE ADV7150.

ADV7150/ADV7152—SPECIFICATIONS

(V_{AA}[1] = +5 V; V_{REF} = +1.235 V; R_L = 37.5 Ω, C_L = 10 pF; R_{SET} = 280 Ω. All specifications T_{MIN} to T_{MAX}[2] unless otherwise noted.)

T-52-33-43

Parameter	All Versions	Units	Test Conditions/Comments
STATIC PERFORMANCE			
Resolution (Each DAC)	10	Bits	
Accuracy (Each DAC)			
Integral Nonlinearity	±1	LSB max	
Differential Nonlinearity	±1	LSB max	Guaranteed Monotonic
Gray Scale Error	±5	% Gray Scale max	
Coding	Binary		
DIGITAL INPUTS (Excluding CLOCK, $\overline{CLOCK}$)			
Input High Voltage, V_{INH}	2	V min	
Input Low Voltage, V_{INL}	0.8	V max	
Input Current, I_{IN}	±10	μA max	V_{IN} = 0.4 V or 2.4 V
Input Capacitance, C_{IN}	10	pF max	
CLOCK INPUTS (CLOCK, $\overline{CLOCK}$)			
Input High Voltage, V_{INH}	V_{AA} − 1.0	V min	
Input Low Voltage, V_{INL}	V_{AA} − 1.6	V max	
Input Current, I_{IN}	±10	μA max	V_{IN} = 0.4 V or 2.4 V
Input Capacitance, C_{IN}	10	pF max	
DIGITAL OUTPUTS			
Output High Voltage, V_{OH}	2.4	V min	I_{SOURCE} = 400 μA
Output Low Voltage, V_{OL}	0.4	V max	I_{SINK} = 3.2 mA
Floating-State Leakage Current	20	μA max	
Floating-State Output Capacitance	20	pF typ	
ANALOG OUTPUTS			
Gray Scale Current Range	15	mA min	
	22	mA max	
Output Current			
White Level Relative to Blank	17.69	mA min	Typically 19.05 mA
	20.40	mA max	
White Level Relative to Black	16.74	mA min	Typically 17.62 mA
	18.50	mA max	
Black Level Relative to Blank	0.95	mA min	Typically 1.44 mA
	1.90	mA max	
Blank Level on RED OUT, BLUE OUT	0	μA min	Typically 5 μA
	50	μA max	
Blank Level on GREEN OUT	6.29	mA min	Typically 7.62 mA
	8.96	mA max	
Sync Level on GREEN OUT	0	μA min	Typically 5 μA
	50	μA max	
LSB Size	17.22	μA typ	
DAC-to-DAC Matching	5	% max	Typically 2%
Output Compliance, V_{OC}	−1	V min	
	+1.4	V max	
Output Impedance, R_{OUT}	100	kΩ typ	
Output Capacitance, C_{OUT}	30	pF max	I_{OUT} = 0 mA
VOLTAGE REFERENCE			
Voltage Reference Range, V_{REF}	1.14/1.26	V min/V max	V_{REF} = 1.235 V for Specified Performance
Input Current, I_{VREF}	−5	mA typ	
POWER REQUIREMENTS			
V_{AA}	5	V nom	
I_{AA}	500	mA max	170 MHz Parts
Power Supply Rejection Ratio	0.5	%/% max	Typically 0.12%/%: f = 1 kHz, COMP = 0.1 μF
Power Dissipation	2500	mW max	170 MHz Parts: V_{AA} = 5 V
DYNAMIC PERFORMANCE			
Clock and Data Feedthrough[3, 4]	−30	dB typ	
Glitch Impulse	50	pV secs typ	
DAC-to-DAC Crosstalk[5]	−23	dB typ	

NOTES
[1]±5% for all versions.
[2]Temperature range (T_{MIN} to T_{MAX}): 0°C to +70°C.
[3]Clock and data feedthrough is a function of the amount of overshoot and undershoot on the digital inputs. Glitch impulse includes clock and data feedthrough.
[4]TTL input values are 0 to 3 volts, with input rise/fall times ≤3 ns, measured the 10% and 90% points. Timing reference points at 50% for inputs and outputs.
[5]DAC-to-DAC crosstalk is measured by holding one DAC high while the other two are making low to high and high to low transitions.
Specifications subject to change without notice.

TIMING CHARACTERISTICS[1] (V_{AA}[2] = +5 V; V_{REF} = +1.235 V; R_L = 37.5 Ω, C_L = 10 pF; R_{SET} = 280 Ω. All specifications T_{MIN} to T_{MAX}[3] unless otherwise noted.)

T-52-33-43

Parameter	170 MHz Version	135 MHz Version	110 MHz Version	85 MHz Version	Units	Conditions/Comments
f_{MAX}	170	135	110	85	MHz	Clock Rate
LOADOUT						
1:1 MUX Mode						
Frequency	68	68	68	68	MHz	LOADOUT Clocking Rate
Period	14.71	14.71	14.71	14.71	ns max	LOADOUT Period
High Time	6	6	6	6	ns min	LOADOUT High Time
Low Time	6	6	6	6	ns min	LOADOUT Low Time
2:1 MUX Mode						
Frequency	68	68	55	42.5	MHz	LOADOUT Clocking Rate
Period	14.71	14.81	18.18	21.25	ns max	LOADOUT Period
High Time	6	6	8	8.5	ns min	LOADOUT High Time
Low Time	6	6	8	8.5	ns min	LOADOUT Low Time
4:1 MUX Mode						
Frequency	42.5	33.75	27.5	21.25	MHz	LOADOUT Clocking Rate
Period	23.5	30	36.4	47	ns max	LOADOUT Period
High Time	10	12	14.5	18.8	ns min	LOADOUT High Time
Low Time	10	12	14.5	18.8	ns min	LOADOUT Low Time
t_1	15	15	15	15	ns max	Pixel CLOCK to LOADOUT Delay
t_2	15	15	15	15	ns max	Pixel CLOCK to PRGCKOUT Delay
t_3	5	5	5	5	ns min	LOADIN to LOADOUT Setup Time
t_4	0	0	0	0	ns min	Video and Pixel Data Setup Time
t_5	5	5	5	5	ns min	Video and Pixel Data Hold Time
t_6	5	5	5	5	ns max	SCKIN to SCKOUT Delay
t_7	5.88	7.4	9.09	11.77	ns min	Clock Cycle Time
t_8	2.5	3	4	5	ns min	Clock Pulse Width High Time
t_9	2.5	3	4	5	ns min	Clock Pulse Width Low Time
t_{10}	12	12	12	12	ns min	Analog Output Delay
t_{11}	2	2	2	3	ns min	Analog Output Rise/Fall Time
t_{12}[4]	6	8	8	12	ns min	Analog Output Settling Time
t_{13}	0	0	0	0	ns min	R/$\overline{W}$, C0, C1 Setup Time
t_{14}	15	15	15	15	ns min	R/$\overline{W}$, C0, C1 Hold Time
t_{15}	50	50	50	50	ns min	$\overline{CE}$ Low Time
t_{16}	25	25	25	25	ns min	$\overline{CE}$ High Time
t_{17}[5]	5	5	5	5	ns min	$\overline{CE}$ Asserted to Data Bus Driven
t_{18}[5]	50	50	50	50	ns max	$\overline{CE}$ Asserted to Data Valid
t_{19}[6]	15	15	15	15	ns max	$\overline{CE}$ Disabled to Data Bus Three Stated
	5	5	5	5	ns min	
t_{20}	20	20	20	20	ns min	Write Data Setup Time
t_{21}	5	5	5	5	ns min	Write Data Hold Time
t_{SK}	2	2	2	2	ns max	Analog Output Skew
	0	0	0	0	ns typ	
t_{PD}	6	6	6	6	Clocks	Pipeline Delay

NOTES

[1]TTL input values are 0 to 3 volts, with input rise/fall times ≤ 3 ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. Analog output load ≤ 10 pF, D0–D7 output load ≤ 50 pF. See timing notes in Figure 5.

[2]±5% for all versions.

[3]Temperature range (T_{MIN} to T_{MAX}); 0°C to + 70°C.

[4]Settling time does not include clock and data feedthrough.

[5]t_{17} and t_{18} are measured with the load circuit of Figure 1 and are defined as the time required for an output to cross 0.4 V or 2.4 V.

[6]t_{19} is derived from the measured time taken by the data outputs to change by 0.5 V when loaded with the circuit of Figure 1. The measured number is then extrapolated back to remove the effects of charging the 50 pF capacitor. This means that the time, t_{19}, quoted in the timing characteristics is the true value for the device and as such is independent of external bus loading capacitances.

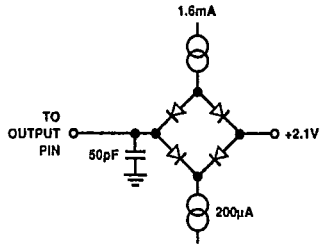


Figure 1. Load Circuit for Bus Access and Relinquish Time

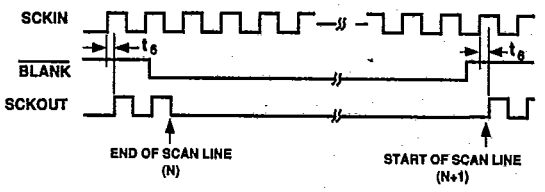


Figure 4. Video Data Serial Clock Input (SCKIN) vs. Serial Clock Output (SCKOUT)

TIMING WAVEFORMS

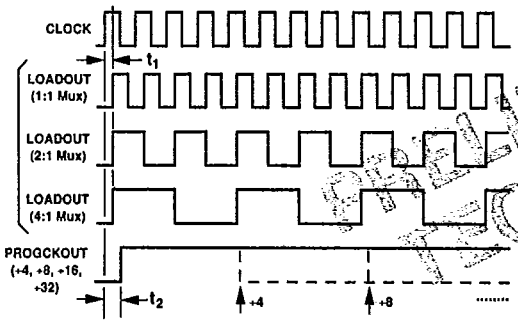


Figure 2. Video Output Clock Controls vs. Pixel Clock Input

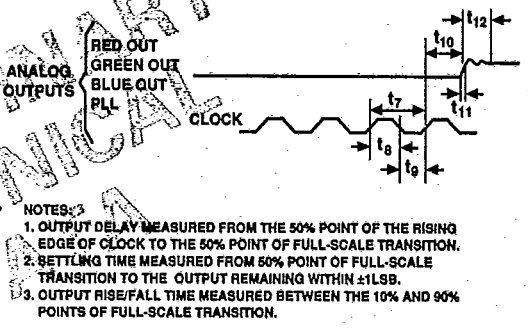


Figure 5. Analog Outputs vs. Pixel Clock

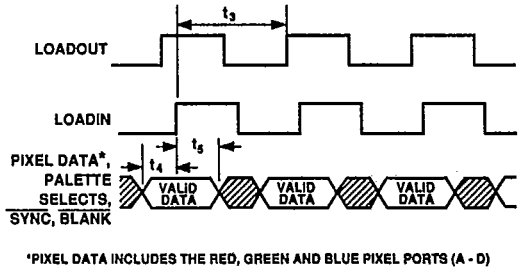


Figure 3. LOADOUT Timing vs. LOADIN and Pixel Data

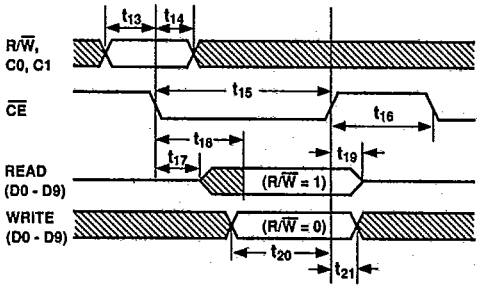


Figure 6. MPU Port Read/Write Timing

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

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RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	V_{AA}	4.75	5.00	5.25	Volts
Ambient Operating Temperature	T_A	0		+70	°C
Reference Voltage	V_{REF}	1.14	1.235	1.26	Volts
Output Load	R_L		37.5		Ω

ABSOLUTE MAXIMUM RATINGS[1]

V_{AA} to GND . . . . . 7 V
Voltage on any Digital Pin . . . . . GND−0.5 V to V_{AA}+0.5 V
Ambient Operating Temperature (T_A) . . . . . −55°C to +125°C
Storage Temperature (T_S) . . . . . −65°C to +150°C
Junction Temperature (T_J) . . . . . +175°C
Lead Temperature (Soldering, 10 secs) . . . . . +300°C
Vapor Phase Soldering (2 minutes) . . . . . +220°C
IOR, IOG, IOB to GND[2] . . . . . −1.5 V to V_{AA}

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Analog output short circuit to any power supply or common can be of an indefinite duration.

ORDERING GUIDE

Model	Speed	Temperature Range	No. of Pins	Package Option*
ADV7150KS170	170 MHz	0°C to +70°C	160	S-160
ADV7150KS135	135 MHz	0°C to +70°C	160	S-160
ADV7150KS110	110 MHz	0°C to +70°C	160	S-160
ADV7150KS85	85 MHz	0°C to +70°C	160	S-160
ADV7152KS170	170 MHz	0°C to +70°C	100	S-100
ADV7152KS135	135 MHz	0°C to +70°C	100	S-100
ADV7152KS110	110 MHz	0°C to +70°C	100	S-100
ADV7152KS85	85 MHz	0°C to +70°C	100	S-100

*S = Plastic Quad Flatpack. For outline information see Package Information section.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.

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The device consists of three, high speed, 10-bit, video D/A converters (RGB), three 256 × 10 (one 256 × 30) color look-up tables, palette priority registers, a pixel input data multiplexer/serializer and a clock generator/divider circuit. The ADV7150 is capable of 1:1, 2:1 and 4:1 multiplexing while the ADV7152 implements 1:1 and 2:1 multiplexing. The on-board palette priority select registers enable multiple palette devices to be connected together for use in multipalette and window applications. The part is controlled (i.e., mode selection and multiplex selection) through the MPU port by the various on-board control/command registers. The part also contains a number of on-board test registers, associated with self diagnostic testing of the device.

The individual red, green and blue pixel input ports allow true-color, image rendition. True-color image rendition, at speeds of up to 170 MHz, is achieved through the use of the on-board data multiplexer/serializer. The pixel input port's flexibility allows for direct interface to most standard frame buffer memory configurations, including general purpose DRAM and VRAM designs.

The 30 bits of resolution, associated with the color look-up table and triple 10-bit DAC, realizes 24-bit true color resolution, while also allowing for the on-board implementation of linearization algorithms, such as gamma correction.

The on-chip video clock controller circuit generates all the internal clocking and some additional external clocking signals. An external ECL oscillator with differential outputs is all that is required to drive the CLOCK and $\overline{\text{CLOCK}}$ inputs of the ADV7150/ADV7152. The part can also be driven by an external clock generator chip circuit.

The ADV7150/ADV7152 is capable of generating RGB video output signals which are compatible with RS-343A and RS-170 video standards, without requiring external buffering.

Test diagnostic circuitry has been included to complement the user's system level debugging.

The ADV7150/ADV7152 is fabricated in a +5 V CMOS process. Its monolithic CMOS construction ensures greater functionality with low power dissipation.

The ADV7150 is packaged in a 160-pin plastic quad flatpack (PQFP). The ADV7152 is packaged in a 100-pin plastic quad flatpack (PQFP).

ADV7150/ADV7152

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ADV7150 PIN ASSIGNMENTS

Pin No.	Mnemonic	Pin No.	Mnemonic	Pin No.	Mnemonic	Pin No.	Mnemonic
1	$G3_A$	41	$PS1_D$	81	NC*	121	$R1_A$
2	$G3_B$	42	$B0_A$	82	D2	122	$R1_B$
3	$G3_C$	43	$B0_B$	83	NC*	123	$R1_C$
4	$G3_D$	44	$B0_C$	84	NC*	124	$R1_D$
5	$G4_A$	45	$B0_D$	85	GND	125	$R2_A$
6	$G4_B$	46	$B1_A$	86	GND	126	$R2_B$
7	$G4_C$	47	$B1_B$	87	D3	127	$R2_C$
8	$G4_D$	48	$B1_C$	88	D4	128	$R2_D$
9	$G5_A$	49	$B1_D$	89	D5	129	$R3_A$
10	$G5_B$	50	$B2_A$	90	V_{AA}	130	$R3_B$
11	$G5_C$	51	$B2_B$	91	D6	131	$R3_C$
12	$G5_D$	52	$B2_C$	92	D7	132	$R3_D$
13	$\overline{CLKIN}$	53	$B2_D$	93	D8	133	$R4_A$
14	CLKIN	54	$B3_A$	94	D9	134	$R4_B$
15	LOADIN	55	$B3_B$	95	GND	135	$R4_C$
16	LOADOUT	56	$B3_C$	96	GND	136	$R4_D$
17	V_{AA}	57	$B3_D$	97	GND	137	$R5_A$
18	V_{AA}	58	$B4_A$	98	$\overline{IOB}$	138	$R5_B$
19	PRGCKOUT	59	$B4_B$	99	$\overline{IOR}$	139	$R5_C$
20	SCKIN	60	$B4_C$	100	$\overline{IOG}$	140	$R5_D$
21	SCKOUT	61	$B4_D$	101	IOB	141	$R6_A$
22	GND	62	$B5_A$	102	IOG	142	$R6_B$
23	GND	63	$B5_B$	103	V_{AA}	143	$R6_C$
24	GND	64	$B5_C$	104	V_{AA}	144	$R6_D$
25	GND	65	$B5_D$	105	V_{AA}	145	$R7_A$
26	$G6_A$	66	$B6_A$	106	IOR	146	$R7_B$
27	$G6_B$	67	$B6_B$	107	COMP	147	$R7_C$
28	$G6_C$	68	$B6_C$	108	V_{REF}	148	$R7_D$
29	$G6_D$	69	$B6_D$	109	R_{SET}	149	$G0_A$
30	$G7_A$	70	$B7_A$	110	I_{PLL}	150	$G0_B$
31	$G7_B$	71	$B7_B$	111	GND	151	$G0_C$
32	$G7_C$	72	$B7_C$	112	V_{AA}	152	$G0_D$
33	$G7_D$	73	$B7_D$	113	V_{AA}	153	$G1_A$
34	$PS0_A$	74	$\overline{CE}$	114	V_{AA}	154	$G1_B$
35	$PS0_B$	75	R/$\overline{W}$	115	$\overline{SYNC}$	155	$G1_C$
36	$PS0_C$	76	C0	116	$\overline{BLANK}$	156	$G1_D$
37	$PS0_D$	77	C1	117	$R0_A$	157	$G2_A$
38	$PS1_A$	78	D0	118	$R0_B$	158	$G2_B$
39	$PS1_B$	79	D1	119	$R0_C$	159	$G2_C$
40	$PS1_C$	80	NC*	120	$R0_D$	160	$G2_D$

*NC = NO CONNECT.

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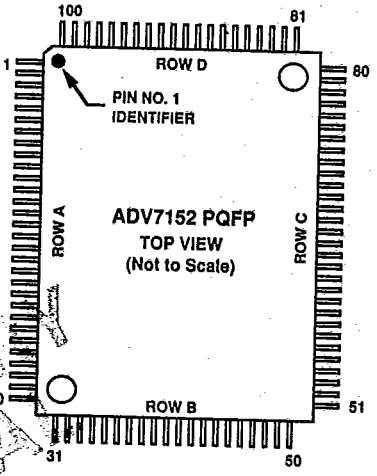
ADV7152 PIN ASSIGNMENTS

Pin No.	Mnemonic	Pin No.	Mnemonic	Pin No.	Mnemonic
1	$\overline{SYNC}$	41	SCKOUT	81	D5
2	$\overline{BLANK}$	42	GND	82	V_{AA}
3	$R0_A$	43	GND	83	D6
4	$R0_B$	44	GND	84	D7
5	GND	45	GND	85	D8
6	$R1_A$	46	GND	86	D9
7	$R1_B$	47	$G6_A$	87	GND
8	$R2_A$	48	$G6_B$	88	GND
9	$R2_B$	49	$G7_A$	89	$\overline{IOB}$
10	$R3_A$	50	$G7_B$	90	$\overline{IOR}$
11	$R3_B$	51	$PS0_A$	91	$\overline{IOG}$
12	$R4_A$	52	$PS0_B$	92	IOB
13	$R4_B$	53	$PS1_A$	93	IOG
14	$R5_A$	54	$PS1_B$	94	V_{AA}
15	$R5_B$	55	$B0_A$	95	I_{PLL}
16	$R6_A$	56	$B0_B$	96	IOR
17	$R6_B$	57	$B1_A$	97	COMP
18	$R7_A$	58	$B1_B$	98	V_{REF}
19	$R7_B$	59	$B2_A$	99	R_{SET}
20	$G0_A$	60	$B2_B$	100	V_{AA}
21	$G0_B$	61	$B3_A$		
22	$G1_A$	62	$B3_B$		
23	$G1_B$	63	$B4_A$		
24	$G2_A$	64	$B4_B$		
25	$G2_B$	65	$B5_A$		
26	NC*	66	$B5_B$		
27	$G3_A$	67	$B6_A$		
28	$G3_B$	68	$B6_B$		
29	$G4_A$	69	$B7_A$		
30	$G4_B$	70	$B7_B$		
31	$G5_A$	71	$\overline{CE}$		
32	$G5_B$	72	$R/\overline{W}$		
33	$\overline{CLOCK}$	73	C1		
34	CLOCK	74	C0		
35	LOADIN	75	D0		
36	LOADOUT	76	D1		
37	V_{AA}	77	D2		
38	V_{AA}	78	GND		
39	PRGCKOUT	79	D3		
40	SCKIN	80	D4		

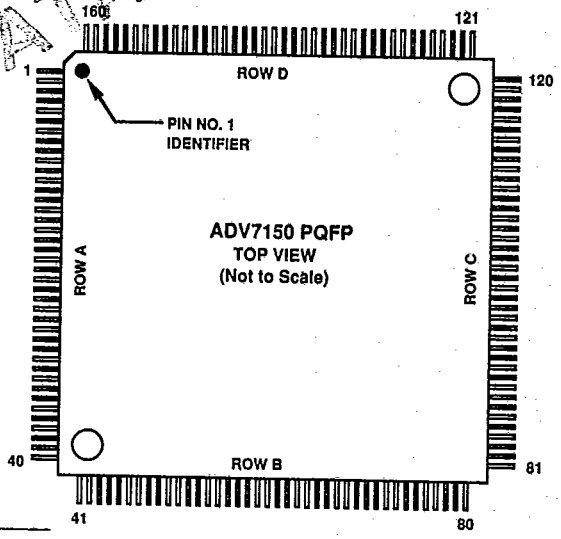
*NC = NO CONNECT.

PIN CONFIGURATIONS

100-Pin PQFP



160-Pin PQFP



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REV. 0

PIN DESCRIPTION

Pin	Function
RED ($R0_A$–$R0_D$/$R7_A$–$R7_D$), GREEN ($G0_A$–$G0_D$/$G7_A$–$G7_D$), BLUE ($B0_A$–$B0_D$/$B7_A$–$B7_D$)	Pixel Port: 96 pixel select inputs, 8 bits for red, green and blue. Each bit is multiplexed (A–D)* 4:1, 2:1 or 1:1. All inputs are TTL compatible.
$PS0_A$–$PS0_D$, $PS1_A$–$PS1_D$	Palette Priority Select Inputs: These inputs allow for switching between multiple palette devices at the pixel rate. The device can be preprogrammed to completely shut off the DAC analog O/Ps. If the values of PS0 and PS1 match the values programmed into bits MR16 and MR17 of the Mode Register, then the device is selected. Each bit is multiplexed (A–D)* 4:1, 2:1 or 1:1. All inputs are TTL compatible.
LOADIN, LOADOUT, PRGCKOUT SCKIN, SCKOUT	Video Data Control Inputs/Outputs: These inputs/outputs are used to load pixel data and, optionally, to control external video frame buffer timing and control synchronization.
CLOCK, $\overline{\text{CLOCK}}$	Clock Inputs: These differential clock inputs are designed to be driven by ECL logic configured for single supply (+5 V) operation. The clock rate is typically the pixel clock rate of the system.
$\overline{\text{BLANK}}$	Composite Blank: Drives the analog outputs to the blanking level.
$\overline{\text{SYNC}}$	Composite Sync Input: Drives the IOG analog output to the sync level. It can only be asserted during the blanking period.
D0–D9	Data Bus: Data is written to and is read from the device over this 10-bit, bidirectional databus. 10-bit data or 8-bit data can be used. The databus can be configured for either 10-bit parallel data or byte data (8+2).
$\overline{\text{CE}}$, R/$\overline{\text{W}}$, CO, C1	Control Inputs: These inputs control the writing to and reading from the address reg, color palette, palette select registers, mode control registers, etc., of the device.
IOR, IOG, IOB ($\overline{\text{IOR}}$, $\overline{\text{IOG}}$, $\overline{\text{IOB}}$)	Analog Video Current Outputs (Differential Outputs): These RGB video outputs are capable of directly driving RS-343A and RS-170 video levels into doubly terminated 75 Ω loads. $\overline{\text{IOR}}$, $\overline{\text{IOG}}$ and $\overline{\text{IOB}}$ can be tied to GND if it is not required to have differential outputs.
V_{REF}	Voltage Reference Input: An external 1.235 V voltage reference is required to drive this input. The use of an AD589 (2-terminal voltage reference) is recommended.
R_{SET}	Output Full-Scale Adjust Control: A resistor connected between this pin and analog ground controls the absolute amplitude of the output video signal. To maintain RS-343A video output levels, R_{SET} = 280 Ω.
COMP	Compensation Pin: A 0.1 μF capacitor should be connected between this pin and V_{AA}.
I_{PLL}	Phase Lock Loop Output Current: This is used to enable multiple ADV7150/ADV7152s along with ADV7151s to be synchronized with pixel resolution.
V_{AA}	Power Supply (+5 V ± 5%): The part contains multiple power supply pins; all should be connected to one common +5 V analog power supply.
GND	Analog Ground: The part contains multiple ground pins; all should be connected to one common analog ground.

*The ADV7152 has only bits A-B (2:1 and 1:1 multiplexing).

COLOR VIDEO MODES (PIXEL PORT)

24-BIT TRUE COLOR

This mode is selected by writing to Command Register 2. In this mode 24-bit true color images can be generated on screen at video rates of up to 170 MHz. A 24-bit pixel word is latched at the pixel clock rate to the RAM and out to the RGB DACs.

15-BIT TRUE COLOR

The ADV7150/ADV7152 can be programmed to run in 15-bit true-color mode. There are two 15-bit true-color modes; the first mode uses the red, green and blue pixel ports while the second mode uses only the red and green pixel ports. Command Register 2 sets the various 15-bit modes. The diagrams show the various pixel port mapping schemes for 15-bit true-color.

15-Bit True Color (Mode 1)

When this mode is set, 15 bits of video data are latched to the device over the upper five bits of each of the RED (R7–R3), GREEN (G7–G3) and BLUE (B7–B3) pixel ports (see Figure 7). The lower 3 bits are ignored. Internally this data is shifted to the lower 5 bits of the LUT decode register, therefore addressing locations 0 to 32 of the look-up table. Each of these 32 addressed locations for the red, green and blue channels can contain an 8- or 10-bit color value, which is latched to each of the three DACs.

15-Bit True Color (Mode 2)

When this mode is set, 15 bits of video data are latched to the device over all 8 bits of the RED (R7–R0) and 7 bits of the

GREEN (G6–G0) pixel ports (see Figure 8). G7 and the data on the BLUE (B7–B0) pixel port is ignored. Internally, this data is shifted to the lower 5 bits of the red, green and blue LUT decode registers, therefore addressing locations 0 to 32 of the look-up table. Each of these 32 addressed locations for the red, green and blue channels can contain an 8- or 10-bit color value which is latched to each of the three DACs.

8-BIT PSEUDO COLOR

This mode is again selected by writing to Command Register 2. In this mode 8-bit pseudo color images can be generated on screen at video rates of up to 170 MHz. 256 colors can be displayed out of a total color palette of 16.7 million addressable colors.

This mode has three further submodes. The pixel input data can be encoded onto either the RED, GREEN or BLUE input pixel stream.

SUBMODE a: 8-bit pseudo color on RED
SUBMODE b: 8-bit pseudo color on GREEN
SUBMODE c: 8-bit pseudo color on BLUE

2

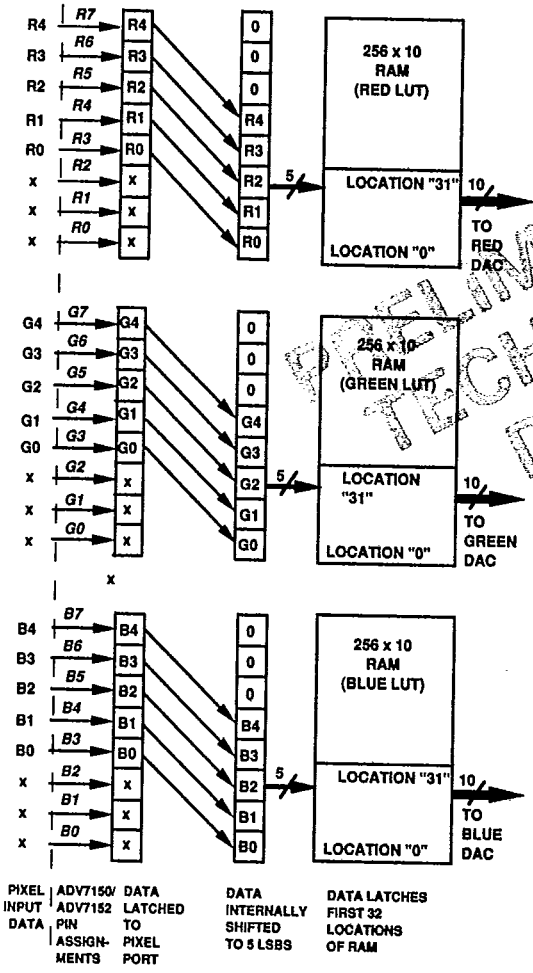

Figure 7. 15-Bit True-Color Mapping Using Red, Green and Blue Pixel Ports (Mode 1)

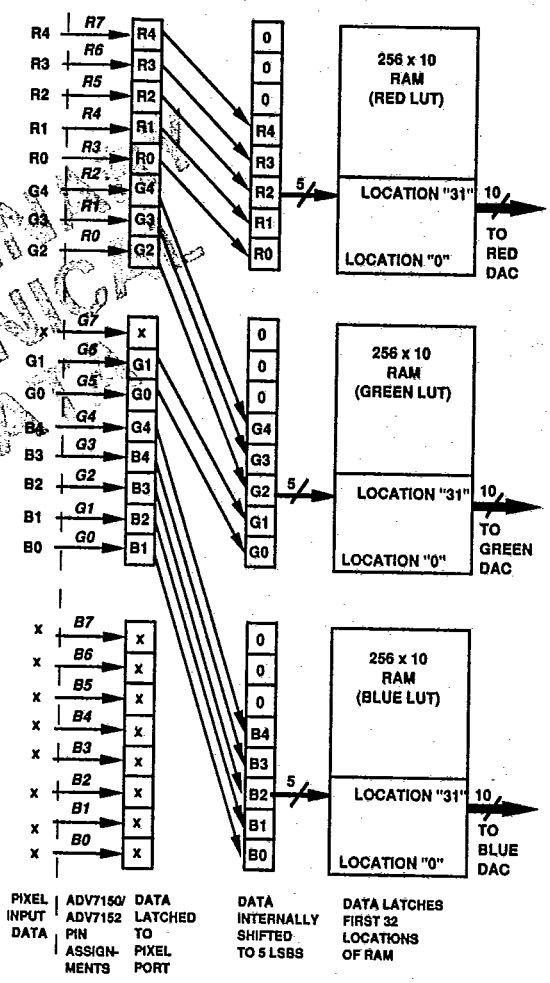

Figure 8. 15-Bit True-Color Mapping Using Red and Green Pixel Ports (Mode 2)

ADV7150/ADV7152

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MPU INTERFACE & CONTROL

The ADV7150/ADV7152 supports a standard MPU Interface. All the functions of the part are controlled via this MPU port. Direct access is gained to the address register, mode register and all the control registers as well as the color palette. The following tables describe the setup for reading and writing to all of the devices registers.

Table I. Interface Truth Table (A)

R/$\overline{W}$	C1	C0	D9–D0	Action[1]
0	0	0	DB7–DB0	Write DB7–DB0 to Address Register (A7–A0)
0	1	1	DB7–DB0	Write DB7–DB0 to Mode Register (MR7–MR0)
0	0	1	DB9–DB0	Write DB9–DB0 to Red RAM Latch
0	0	1	DB9–DB0	Write DB9–DB0 to Green RAM Latch
0	0	1	DB9–DB0	Write DB9–DB0 to Blue RAM Latch & Write RGD Data to RAM Location A7–A0 & Address Register = Address Register + 1
0	1	0	DB7–DB0	Write to Register (A2–A0)[2]
1	0	0	DB7–DB0	Read Address Register (A7–A0)
1	1	1	DB7–DB0	Read Mode Register (MR17–MR10)
1	0	1	DB9—DB0	Read Red RAM Location A7–A0
1	0	1	DB9–DB0	Read Green RAM Location A7–A0
1	0	1	DB9–DB0	Read Blue Ram Location A7–A0 Address Register = Address Register + 1
1	1	0	DB7–DB0	Read Register (A2–A0)[2]

[1]10-bit wide databus, i.e., MR12 = "1" and 10-bit RAM & DACs, i.e., MR11 = "1" or 10-bit wide databus, i.e., MR12 = "1" and 8-Bit RAM & DACs, i.e., MR11 = "0" or 8-bit wide databus, i.e., MR12 = "0" and 8-Bit RAM & DACs, i.e., MR11 = "0."
[2]Refer to Table III.

Table II. Interface Truth Table (B)

R/$\overline{W}$	C1	C0	D7–D0	Action[1]
0	0	0	DB7–DB0	Write DB7–DB0 to Address Register (A7–A0)
0	1	1	DB7–DB0	Write DB7–DB0 to Mode Register (MR7–MR0)
0	0	1	DB9–DB2	Write DB9–DB2 to Red RAM Latch (9–2)
0	0	1	DB1–DB0	Write DB1–DB0 to Red RAM Latch (1–0)
0	0	1	DB9–DB2	Write DB9–DB2 to Green RAM Latch (9–2)
0	0	1	DB1–DB0	Write DB1–DB0 to Green RAM Latch (1–0)
0	0	1	DB9–DB2	Write DB9–DB2 to Blue RAM Latch (9–2)
0	0	1	DB1–DB0	Write DB1–DB0 to Blue RAM Latch (1–0) & Write RGB Data to RAM Location A7–A0 & Address Register = Address Register + 1
0	1	0	DB7–DB0	Write to Register (A2–A0)[2]
1	0	0	DB7–DB0	Read Address Register (A7–A0)
1	1	1	DB7–DB0	Read Mode Register (MR17–MR10)
1	0	1	DB9–DB2	Read Red RAM (9–2) Location A7–A0
1	0	1	DB1–DB0	Read Red RAM (1–0) Location A7–A0
1	0	1	DB9–DB2	Read Green RAM (9–2) Location A7–A0
1	0	1	DB1–DB0	Read Green RAM (1–0) Location A7–A0
1	0	1	DB9–DB2	Read Blue RAM (9–2) Location A7–A0
1	0	1	DB1–DB0	Read Blue RAM (1–0) Location A7–A0 Address Register = Address Register + 1
1	1	0	DB7–DB0	Read Register (A2–A0)[2]

[1]8-bit wide databus, i.e., MR12 = "0" and 10-Bit RAM & DACs, i.e., MR11 = "1."
[2]Refer to Table III.

REGISTER PROGRAMMING

Direct writes and reads can be made to the address register and the mode register. The control registers, seven of which are listed in the table, are indexed addressable. The first write to the control register specifies which particular register is to be accessed.

Address Register (ADDR) A7–A0

As illustrated in the previous tables, the C0 and C1 control inputs, in conjunction with this address register, specify which control/mode register or color palette location is accessed by the MPU port. The address register is 8 bits wide and can be read from as well as written to. When writing to or reading from the color palette on a sequential basis, only the start address needs to be written. After a red, green and blue write sequence, the address register is automatically incremented.

Mode Register 1 (MR1)

The mode register is a 10-bit wide register. However, for programming purposes it may be considered as an 8-bit wide register (MR18 and MR19 are both reserved).

The diagram below shows the various operations under the control of the mode register. This register can be read from as well as written to. In read mode, MR18 and MR19 are both returned as zeros.

MODE REGISTER (MR1) BIT DESCRIPTION

Reset Control (MR10)

This bit is used to reset the pixel port sampling sequence. This ensures that the pixel sequence ABCD starts at A. It is reset by writing a 1 followed by a zero followed by a 1.

RAM-DAC Resolution Control (MR11)

When this is programmed with a 1, the RAM is 30 bits deep (10 bits each for red, green and blue), and each of the three DACs is configured for 10-bit resolution.

When MR11 is programmed with a 0, the RAM is 24 bits deep (8 bits each for red, green and blue), and the DACs are configured for 8-bit resolution. The two LSBs of the 10-bit DACs are pulled down to zero.

MPU Data Bus Width (MR12)

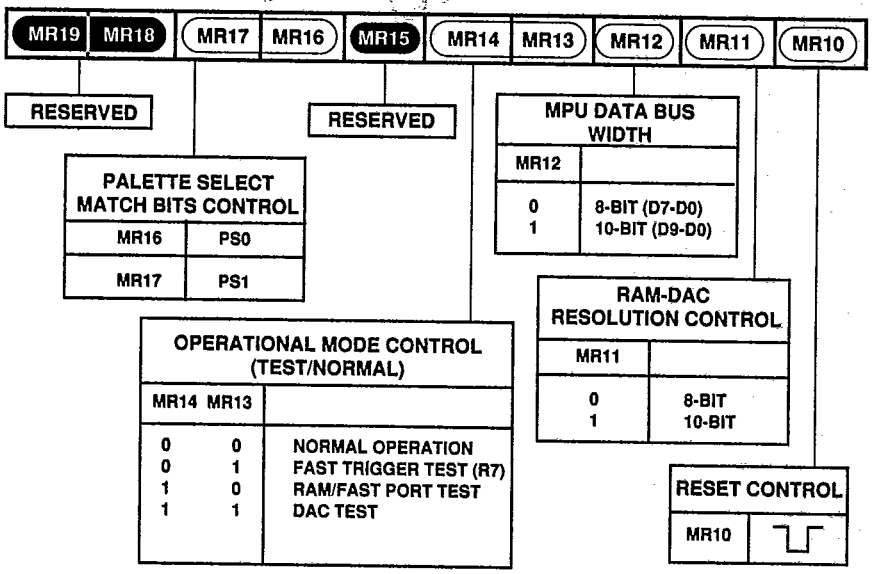
This bit determines the width of the MPU port. It is configured as either a 10-bit wide (D9–D0) or 8-bit wide (D7–D0) bus. 10-bit data can be written to the device when configured 8-bit wide mode. The eight MSBs are first written on D7–D0, then the two LSBs are written over D1–D0. Bits D9–D8 are zeros in 8-bit mode.

Operational Mode Control (Test/Normal) (MR14–MR13)

When these bits are zero, the part operates in normal mode. All other combinations are used in conjunction with the device's various test/diagnostic modes (see Test Diagnostics section).

Palette Select Match Bits Control (MR17–MR16)

These bits allow multiple palette devices to work together. When PS1–PS0 match MR17–MR16, the device is selected (see Palette Priority Select Inputs section).



Mode Register 1 (MR1)

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CONTROL REGISTERS

The ADV7150/ADV7152 has seven control registers. To access each register, two write operations must be performed. The first write to the address register specifies which of the seven registers is to be accessed. The second access determines the value written to that particular control register.

Table III lists the various control registers and their respective addresses.

Table III. Control Registers Descriptions

ADDR Register	Control Registers* (A2–A0)
00H	Pixel Test Register
01H	DAC Test Register
02H	SYNC, BLANK and I_{PLL} Test Register
03H	ID Register (Read Only)
04H	Pixel Mask Register
05H	Reserved
06H	Command Register 2
07H	Command Register 3

*C1 = 1; C0 = 0.

Pixel Test Register
This register is used when the device is in test/diagnostic mode. It is an 8-bit wide read-only register which allows MPU access to the pixel port (see Test Diagnostics section).

DAC Test Register
This register is used when the device is in test/diagnostic mode. It is a 10-bit wide read/write register which allows MPU access to the DAC port (see Test Diagnostics section).

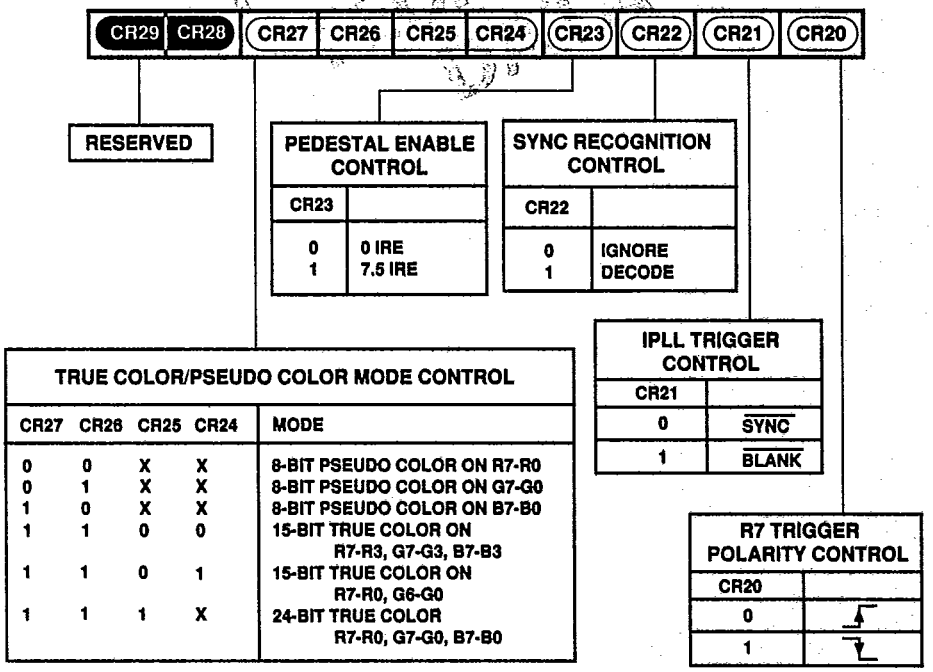
$\overline{SYNC}$, $\overline{BLANK}$ & I_{PLL} Test Register:
This register is used when the device is in test/diagnostic mode. It is a 3-bit wide (3 LSBs) read/write register which allows MPU access to these particular pixel control bits (see Test Diagnostics section).

ID Register
This is an 8-bit wide read-only register. For the ADV7150, it will always return the hexadecimal value 8EH and for the ADV7152, 8CH will be returned.

Pixel Mask Register
The contents of the pixel read mask register are individually bitwise logically ANDed with the red, green and blue pixel input stream of data. It is an 8-bit read/write register with D0 corresponding to R0, G0 and B0.

Command Register 2 (CR2)
This register contains a number of control bits as shown in the diagram. CR2 is a 10-bit wide register. However, for programming purposes, it may be considered as an 8-bit wide register (CR28 and CR29 are both reserved).

The diagram below shows the various operations under the control of CR2. This register can be read from as well written to. In read mode, CR28 and CR29 are both returned as zeros.



Command Register 2 (CR2)

COMMAND REGISTER 2 (CR2) BIT DESCRIPTION

R7 Trigger Polarity Control (CR20)
This bit is used when the device is in test/diagnostic mode. It determines whether the pixel data is latched into the test registers in the rising or falling edge of R7 (see test diagnostics section).

I_{PLL} Trigger Control (CR21)
This bit specifies whether the PLL output is triggered from $\overline{BLANK}$ or $\overline{SYNC}$.

$\overline{SYNC}$ Recognition Control (CR22)
This bit specifies whether the video $\overline{SYNC}$ input is to be encoded onto the IOG analog output or ignored.

Pedestal Enable Control (CR23)
This bit specifies whether a 0 IRE or a 7.5 IRE blanking pedestal is to be generated on the video outputs.

True-Color/Pseudo-Color Mode Control (CR27-CR24)
These 4 bits specify the various color modes. These include a 24-bit true-color mode, two 15-bit true-color modes and three 8-bit pseudo color modes.

Command Register 3 (CR3)
This register contains a number of control bits as shown in the diagram. CR3 is a 10-bit wide register. However, for programming purposes, it may be considered as an 8-bit wide register (CR38 and CR39 are both reserved).

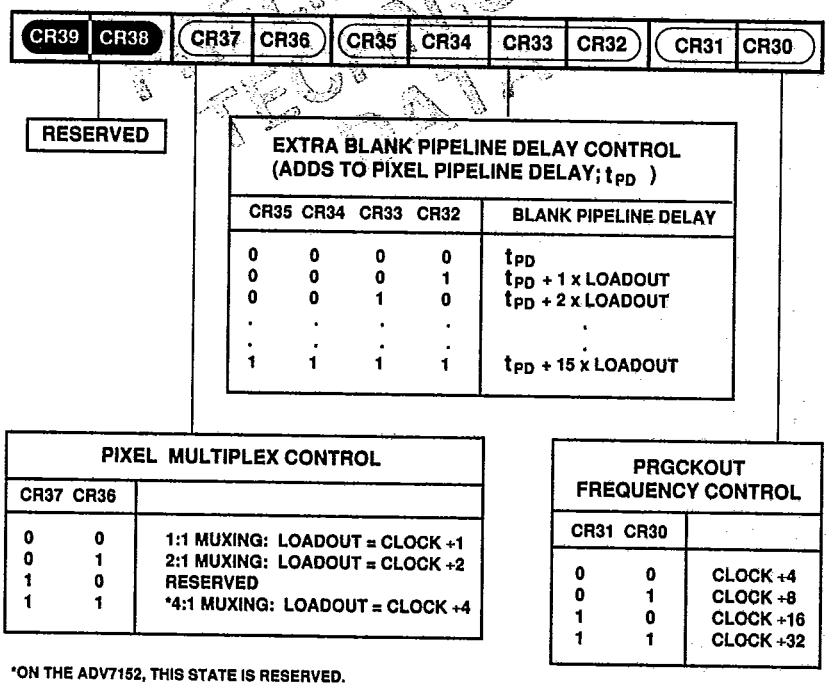
The diagram below shows the various operations under the control of CR3. This register can be read from as well as written to. In read mode, CR38 and CR39 are both returned as zeros.

COMMAND REGISTER 3 (CR3) BIT DESCRIPTION

PRGCKOUT Frequency Control (CR31–CR30)
These bits specify the output frequency of the PRGCKOUT output. PRGCKOUT is a divided down version of the pixel CLOCK.

$\overline{BLANK}$ Pipeline Delay Control (CR35–CR32)
These bits specify the additional pipeline delay that can be added to the $\overline{BLANK}$ function, relative to the overall device pipeline delay (t_{PD}). As the $\overline{BLANK}$ control normally enters the video DAC from a shorter pipeline than the video pixel data, this control is useful in deskewing the pipeline differential.

Pixel Multiplex Control (CR37–CR36)
These bits specify the device's multiplex mode. It, therefore, also determines the frequency of the LOADOUT signal. LOADOUT is a divided down version of the pixel CLOCK.



*ON THE ADV7152, THIS STATE IS RESERVED.

Command Register 3 (CR3)

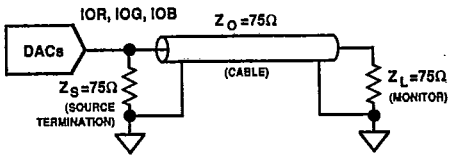


Figure 9. RS-343A Termination

RED, BLUE		GREEN	
mA	V	mA	V
19.05	0.714	26.67	1.000
1.44	0.054	9.05	0.340
0	0	7.62	0.286
		0	0

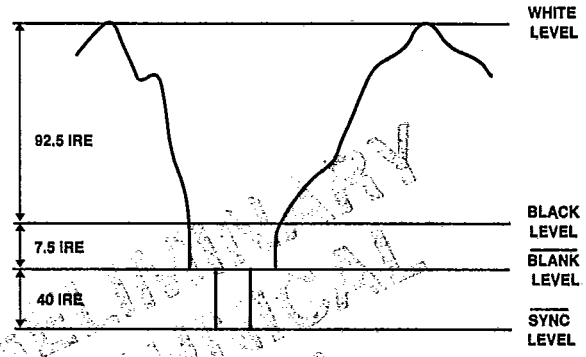


Figure 10. RS-343 Video Waveform

Table IV. Video Output Truth Table

Description	GREEN OUT (mA)	RED OUT, BLUE OUT (mA)	SYNC	BLANK	DAC Input Data
WHITE LEVEL	26.67	19.05	1	1	3FFH
VIDEO	video + 9.05	video + 1.44	1	1	data
VIDEO to BLANK	video + 1.44	video + 1.44	0	1	data
BLACK LEVEL	9.05	1.44	1	1	000H
BLACK to BLANK	1.44	1.44	0	1	000H
BLANK LEVEL	7.62	0	1	0	XXXH
SYNC LEVEL	0	0	0	0	XXXH

CLOCK CONTROLLER CIRCUIT

The ADV7150/ADV7152 has an on-board clock controller circuit. This is driven by an external crystal oscillator which must be capable of generating differential clock inputs to drive CLOCK and CLOCK of the ADV7150/ADV7152.

No additional external clocking devices are necessary. A sophisticated on-board clocking arrangement generates all the required internal clocking signals.

Additional functions are included to ease system design. The PRGCKOUT can be sufficiently divided down and can be used to drive the video clock of the graphics processor.

In its simplest form, the LOADOUT pin can be tied directly to the LOADIN pin, as shown. The pixel data LOADIN rate will be determined by the multiplex rate.

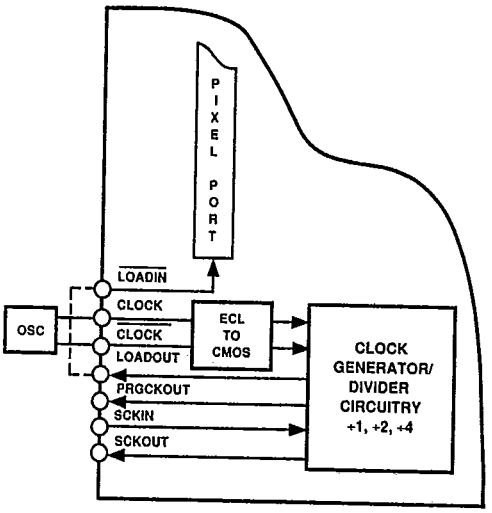


Figure 11. Clock Circuitry

TEST DIAGNOSTICS

Test diagnostic circuitry on the ADV7150/ADV7152 allows the user to debug both the device itself and its interface to other components in the system. Essentially, the video or pixel path through the device can be monitored via the MPU. Monitoring points, in the form of test registers are positioned at the PIXEL PORT, RAM and DAC PORT. Control of the test modes is determined by the Mode Register (MR1) and Command Register 2. Data is latched to the various test registers along the video path by either the pixel CLOCK or by using one bit of pixel data as a trigger bit (R7). This latter case is useful when the pixel CLOCK is connected to a free running source.

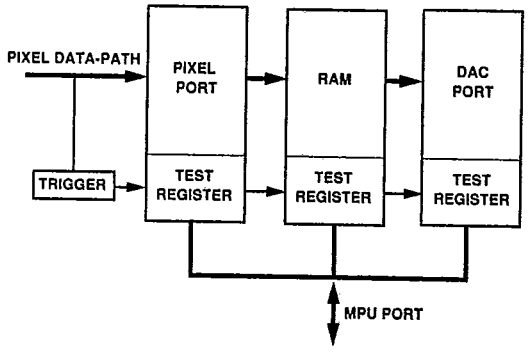


Figure 12.

Mode 0

Normal Chip Operation. In this mode, the test registers are configured as in Figure 13. Both the pixel test register and the DAC test register are triggered every clock cycle. This is transparent to the general user. It becomes useful when there is independent control over the CLOCK. By stopping the clock in the low state, the data in the test registers can be read out and verified.

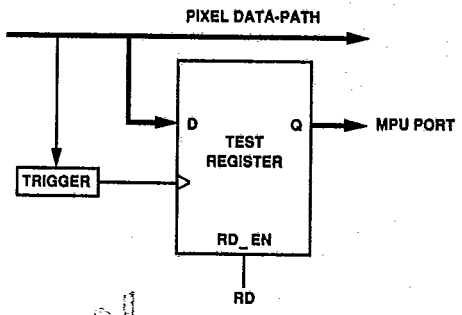


Figure 13.

Mode 1

Pixel Data-Path Trigger. In this mode, the test register trigger is activated by a transition on the R7 bit of the pixel port, Figure 13. Bit 0 of command register 2 controls whether the trigger is activated by a rising edge or a falling edge of R7. The trigger bit is piped through the chip along with the pixel data. This means that each test register captures the pixel with the transition on R7 as it is piped through the chip. Once the data has been captured, it can be read out at any time, even if the pattern is cyclical with the same pixel repeatedly activating the trigger.

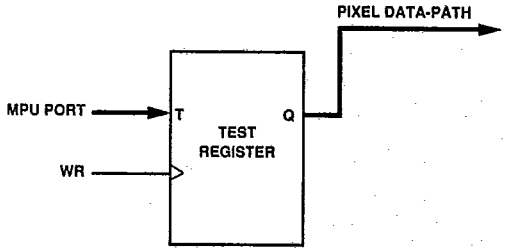


Figure 14.

Mode 2

RAM Fast-Port Test. Is this mode, the pixel test register is configured as in Figure 13, and the DAC test register configured as in Figure 14. The DAC test register is triggered every clock cycle. Data written into the pixel test register enters the fast data path, passes through the palette, and gets captured at the DAC test register.

Mode 3

DAC Test. In this mode, the DAC test register and the $\overline{\text{SYNC}}$, $\overline{\text{BLANK}}$ & PLL test register are configured as in Figure 14. Data written to the DAC test register, and the $\overline{\text{SYNC}}$, $\overline{\text{BLANK}}$ and PLL test register is reflected at the DAC outputs. This allows the DACs to be tested over the microport.

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Palette Priority Select Inputs

The palette priority selection function allows up to 4 palette devices to be used with their analog O/Ps connected together. During initialization, internal registers, which prioritize each device, are programmed. PS0 and PS1 inputs will select one of the preprogrammed devices at any instant. PS0 and PS1 are multiplexed similar to the pixel data, thus allowing for subpixel resolution. This enables the user to have multiple palettes and/or windows.

Note: Only one palette device is selected at any particular instant. The analog O/Ps of the unselected devices should be at 0 mA.

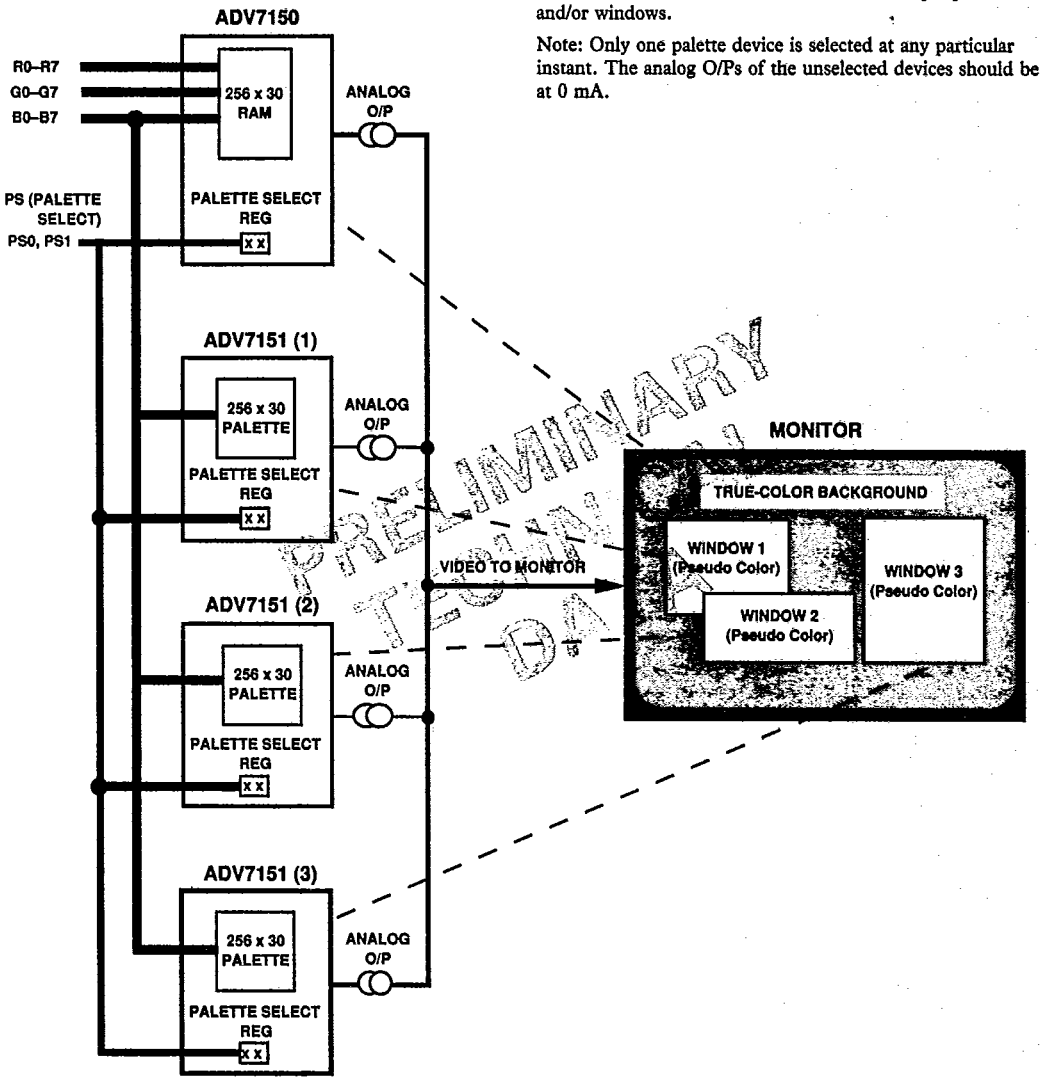

Figure 15.

PC Board Considerations
The layout should be optimized for lowest noise on the ADV7150/ADV7152 power and ground lines by shielding the digital inputs and providing good decoupling. The lead length between groups of V_{AA} and GND pins should by minimized so as to minimize inductive ringing.

Ground Planes
The ground plane should encompass all ADV7150/ADV7152 ground pins, voltage reference circuitry, power supply bypass circuitry for the ADV7150/ADV7152, the analog output traces, and all the digital signal traces leading up to the ADV7150/ ADV7152.

Power Planes
The ADV7150/ADV7152 and any associated analog circuitry should have its own power plane, referred to as the analog power plane. This power plane should be connected to the regular PCB power plane (V_{CC}) at a single point through a ferrite bead. This bead should be located within three inches of the ADV7150/ADV7152.

The PCB power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all ADV7150/ADV7152 power pins and voltage reference circuitry.

Plane-to-plane noise coupling can be reduced by ensuring that portions of the regular PCB power and ground planes do not overlay portions of the analog power plane, unless they can be arranged such that the plane-to-plane noise is common mode.

Supply Decoupling
For optimum performance, bypass capacitors should be installed using the shortest leads possible, consistent with reliable operation, to reduce the lead inductance. Best performance is obtained with a 0.1 μF ceramic capacitor decoupling each of the two groups of V_{AA} pins to GND. These capacitors should be placed as close as possible to the device.

It is important to note that while the ADV7150/ADV7152 contain circuitry to reject power supply noise, this rejection decreases with frequency. If a high frequency switching power supply is used, the designer should pay close attention to reducing power supply noise and should consider using a three terminal voltage regulator for supplying power to the analog power plane.

Digital Signal Interconnect
The digital inputs to the ADV7150/ADV7152 should be isolated as much as possible from the analog outputs and other analog circuitry. Also, these input signals should not overlay the analog power plane.

Due to the high clock rates involved, long clock lines to the ADV7150/ADV7152 should be avoided to reduce noise pickup.

Any active termination resistors for the digital inputs should be connected to the regular PCB power plane (V_{CC}), and not the analog power plane.

2

Analog Signal Interconnect
The ADV7150/ADV7152 should be located as close as possible to the output connectors to minimize noise pickup and reflections due to impedance mismatch.

The video output signals should overlay the ground plane, and not the analog power plane, to maximize the high frequency power supply rejection.

For maximum performance, the analog outputs should each have a 75 ohm load resistor connected to GND. The connection between the current output and GND should be as close as possible to the ADV7150/ADV7152 to minimize reflections.