



PIC16C71 → PIC16C710/711 Migration

DEVICE MIGRATIONS

This document is intended to describe the functional differences and the electrical specification differences that are present when migrating from one device to the next.

Note: This device has been designed to perform to the parameters of its data sheet. It has been tested to an electrical specification designed to determine its conformance with these parameters. Due to process differences in the manufacture of this device, this device may have different performance characteristics than its earlier version. These differences may cause this device to perform differently in your application than the earlier version of this device.

Table 1 shows the considerations that must be taken into account when migrating from the PIC16C71 to the PIC16C710/711.

TABLE 1: PIC16C71 → PIC16C710/711 DIFFERENCES

Functional Differences				
No.	Difference	H/W	S/W	Prog.
1	Programming algorithm change	—	—	✓
2	PIC16C710/711 has BOR circuit	✓	—	✓

Note: The user should verify that the device oscillator starts and performs as expected. Adjusting the loading capacitor values and /or the oscillator mode may be required.

TABLE 2: PROGRAM AND DATA MEMORY DIFFERENCES

	PIC16C71	PIC16C710	PIC16C711
Program Memory	1024	512	1024
Data Memory	36	36	68

TABLE 3: ELECTRICAL SPECIFICATION DIFFERENCES

Parm. No.	Sym.	Characteristic	PIC16C71 Data Sheet			PIC16C710/711 Data Sheet			Units	Conditions
			Min	Typ	Max	Min	Typ	Max		
	VDD	Supply Voltage XT, RC, LP Options XT, RC Opt. Extended	3.0 —	— —	6.0 —	2.5 3.0	— —	6.0 6.0	V V	LC versions LC version
	IDD	Supply Current XT and RC options HS option XT and RC options LP option	— —	1.8 4.8	3.3 10	— —	1.8 4.5	2.4 16	mA mA	PIC16C71/710/711 Note 1 Note 2 PIC16LC71/710/711 Note 3 Note 4
	IPD	Power Down Current Commercial Industrial Extended Commercial Industrial Extended	— — — —	1.0 7 1.0 —	14 28.0 16 —	— — — —	1.5 10.5 1.5 1.5	21 41 24 30	μA μA μA μA	PIC16C71/710/711 VDD = 4.0 WDT Disabled WDT enabled WDT disabled WDT disabled PIC16LC71/710/711 VDD = 3.0 WDT disabled WDT enabled WDT disabled WDT disabled
	VIH	Input High Voltage I/O Ports with Schmitt Trigger buffer MCLR, RB0/INT	0.85VDD 0.85VDD	— —	VDD VDD	0.8VDD 0.8VDD	— —	VDD VDD	V V	For all VDD
	FOSC	Oscillator Frequency	1 1 DC	— — —	4 20 200	4 — 5	— — —	20 — 200	MHz MHz kHz	HS osc mode HS osc mode LP osc mode
	TmLC	MCLR Pulse Width (low)	0.2	—	—	2	—	—	μs	Note 5
	TIOZ	I/O High Impedance from MCLR Low	—	—	0.1	—	—	1.1	μs	
	EABS	Absolute Error (AD converter)	—	—	< ±2	—	—	< ±1	LSb	LC versions
	EIL	Integral linearity error (AD converter)	—	—	< ±2	—	—	< ±1	LSb	LC versions
	EDL	Differential linearity error (AD converter)	—	—	< ±2	—	—	< ±1	LSb	LC versions
	EFS	Full Scale Error (AD converter)	—	—	< ±2	—	—	< ±1	LSb	LC versions
	EOFF	Offset Error (AD converter)	—	—	< ±2	—	—	< ±1	LSb	LC versions

Note 1: FOSC = 4.0MHz, VDD = 5.5V.

2: FOSC = 20MHz, VDD = 5.5V.

3: FOSC = 4MHz, VDD = 3.0V.

4: FOSC = 32kHz, VDD = 3.0V, WDT disabled.

5: For PIC16C71: VDD = 5.0V, -40°C to +85°C; For PIC16C710/711: VDD = 5.0V, -40°C to +125°C.

TABLE 4: ABSOLUTE MAXIMUM SPECIFICATION DIFFERENCES

Description	PIC16C71 Data Sheet	PIC16C710/711 Data Sheet	Units
Total Power Dissipation	0.8	1	W
Maximum Current out of Vss Pin	150	300	mA
Maximum Current into VDD Pin	100	250	mA
Maximum Current Sourced by any I/O Pin	20	25	mA
Maximum Current Sunk by PORTA	80	200	mA
Maximum Current Sourced by PORTA	50	200	mA
Maximum Current Sunk by PORTB	150	200	mA
Maximum Current Sourced by PORTB	100	200	mA

FIGURE 1: CONFIGURATION WORD FOR PIC16C71

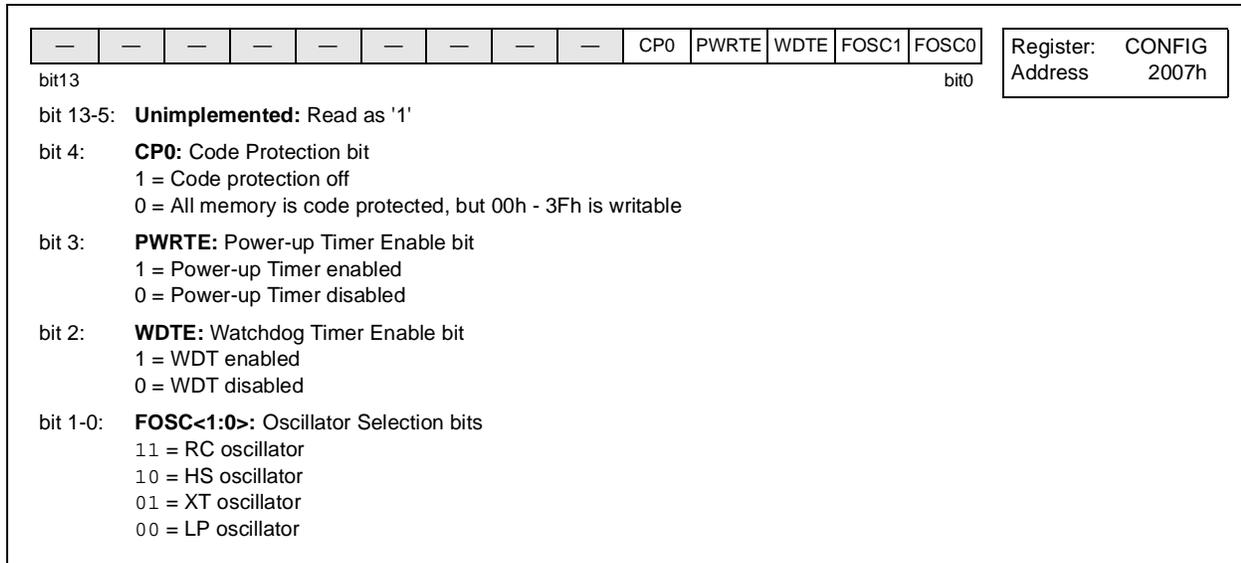
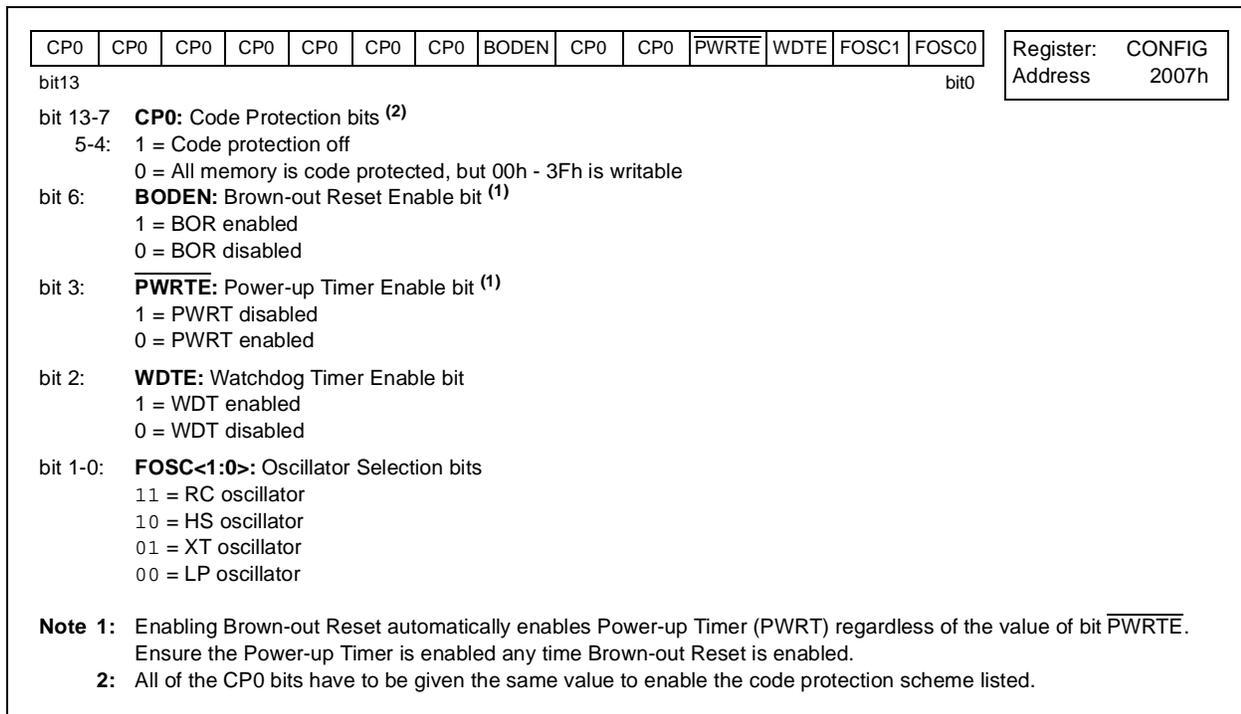


FIGURE 2: CONFIGURATION WORD FOR PIC16C710/711



Note: The Power-up Timer enable bit has a reverse polarity on the PIC16C71 and PIC16C710/711.

TABLE 5: TAD vs. DEVICE OPERATING FREQUENCIES, PIC16C71

AD Clock Source (TAD)		Device Frequency				
Operation	ADCS<1:0>	20 MHz	16 MHz	4 MHz	1 MHz	333.33 kHz
2TOSC	00	100 ns ⁽²⁾	125 ns ⁽²⁾	500 ns ⁽²⁾	2.0 µs	6 µs
8TOSC	01	400 ns ⁽²⁾	500 ns ⁽²⁾	2.0 µs	8.0 µs	24 µs ⁽³⁾
32TOSC	10	1.6 µs ⁽²⁾	2.0 µs	8.0 µs	32.0 µs ⁽³⁾	96 µs ⁽³⁾
RC ⁽⁵⁾	11	2 - 6 µs ^(1,4)	2 - 6 µs ^(1,4)	2 - 6 µs ^(1,4)	2 - 6 µs ⁽¹⁾	2 - 6 µs ⁽¹⁾

Legend: Shaded cells are outside of recommended range.

Note 1: The RC source has a typical TAD time of 4 µs.

2: These values violate the minimum required TAD time.

3: For faster conversion times, the selection of another clock source is recommended.

4: When device frequency is greater than 1 MHz, the RC A/D conversion clock source is recommended for SLEEP operation only.

5: For extended voltage devices (LC), please refer to Electrical Specifications section.

TABLE 6: TAD vs. DEVICE OPERATING FREQUENCIES, PIC16C710/711

AD Clock Source (TAD)		Device Frequency			
Operation	ADCS<1:0>	20 MHz	5 MHz	1.25 MHz	333.33 kHz
2TOSC	00	100 ns ⁽²⁾	400 ns ⁽²⁾	1.6 µs	6 µs
8TOSC	01	400 ns ⁽²⁾	1.6 µs	6.4 µs	24 µs ⁽³⁾
32TOSC	10	1.6 µs	6.4 µs	25.6 µs ⁽³⁾	96 µs ⁽³⁾
RC ⁽⁵⁾	11	2 - 6 µs ^(1,4)	2 - 6 µs ^(1,4)	2 - 6 µs ^(1,4)	2 - 6 µs ⁽¹⁾

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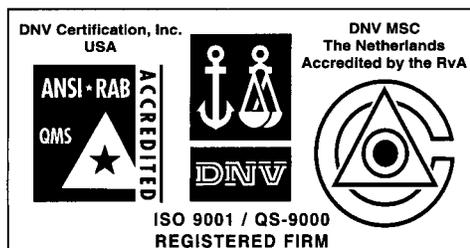
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