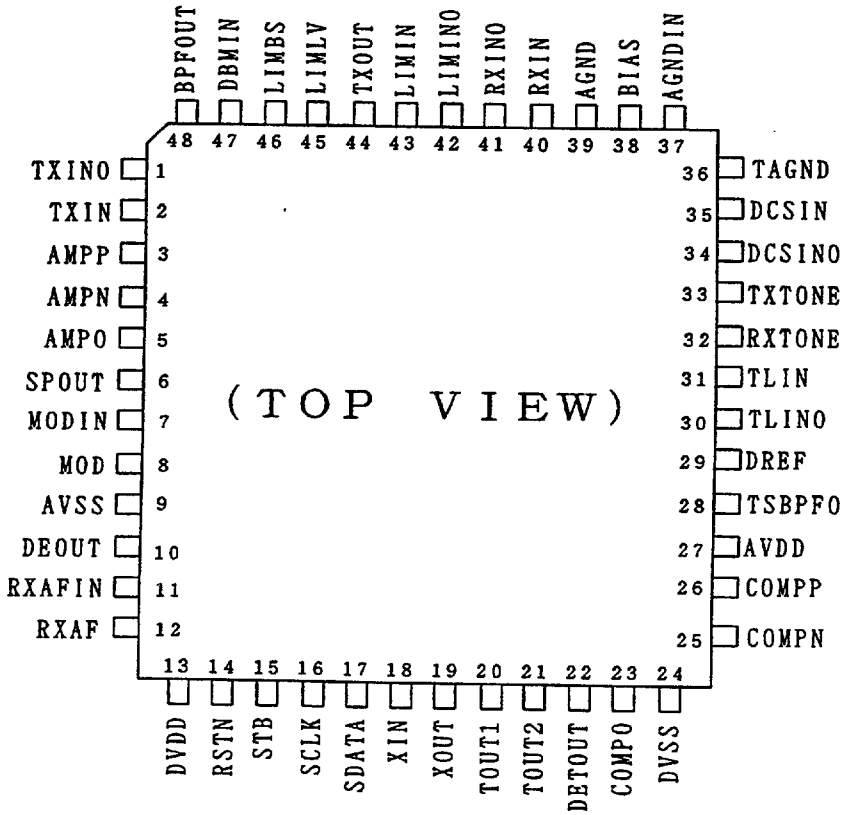
AK2342A

CTCSS Encoder/Decoder (with Scrambler)

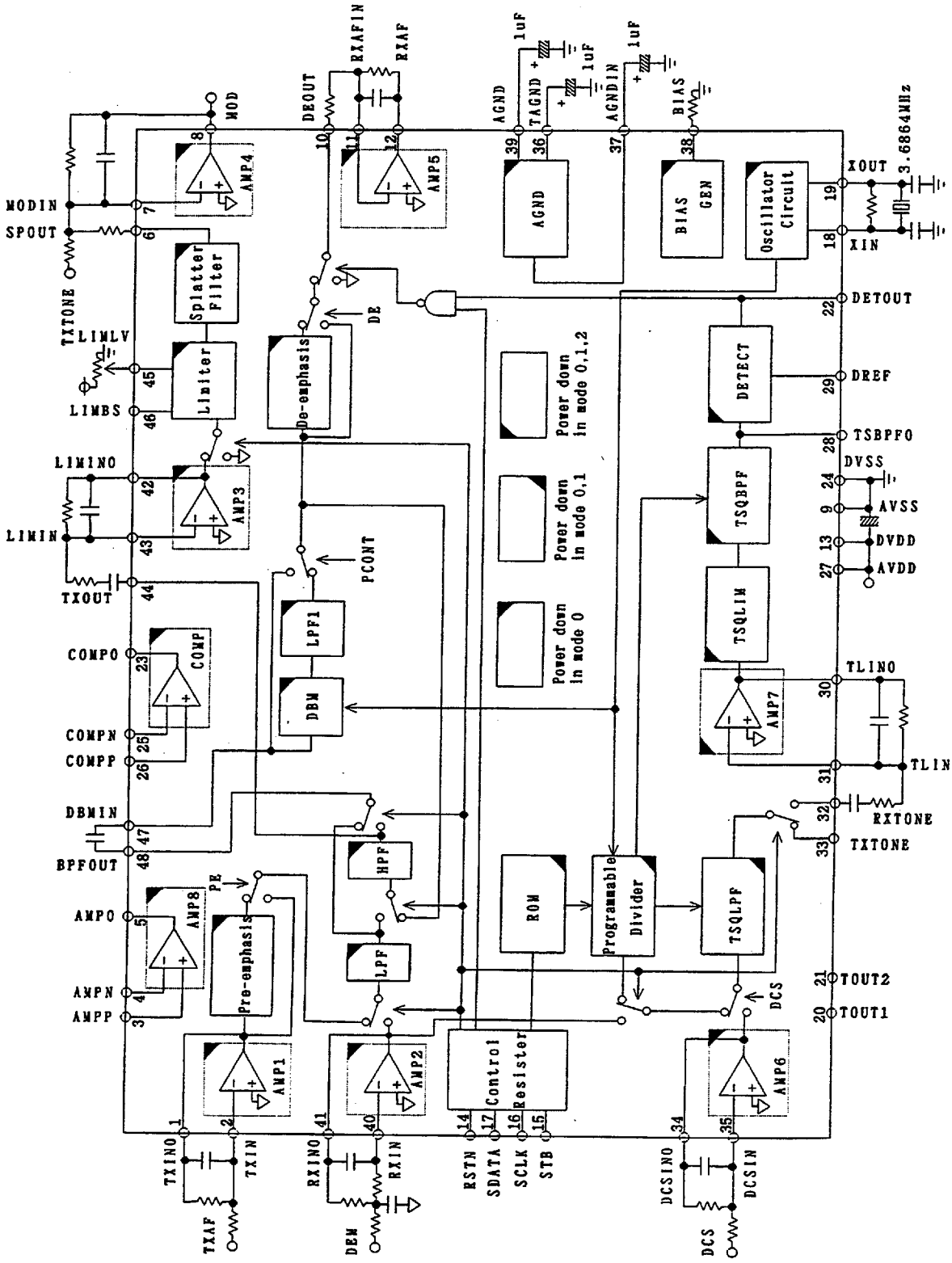
Features

- Encoder/decoder for CTCSS (Continuous Tone Controlled Squelch System).
- Programmable for up to 50 frequencies.
- Integrated voice signal circuits for emphasis, a limiter, splatter filter, etc.
- Integrated scrambler for privacy.
- Integrated tone signal elimination filter.
- Can be linked with a DCS (Digitally Coded Squelch) system.
- Power down function.
- Integrated oscillator circuit (3.6864 MHz) using a crystal oscillator.
- Control register controlled through a serial interface.
- Low voltage operation CMOS (1.8 ~ 5.5 V)
- A compact plastic package 48 Pin SQFP

■ Pin Arrangement



Block Diagram



Description

The AK2342A is an IC which supports CTCSS (Continuous Tone Controlled Squelch System), compatible with the EIA RS-220A standard.
A single tone may be selected from among 50 different frequencies within a range of 67~254 Hz. By sending that tone simultaneously with the voice signal during transmission, and by setting the audio circuit so that it operates only when a tone of that frequency is detected, it is possible to have multiple communications on the same radio frequency.
Voice signal filters, a limiter, op-amp, and other circuits are integrated, making it possible to configure a radio base band unit from a single chip.
A scrambler circuit is also included to keep privacy.

Circuit Configuration

Block	Function
AMP1	Operational amplifier for adjusting the transmitting voice signal gain and preventing SCF aliasing in subsequent stages. Set the gain at 30 dB or lower and the cut-off frequency at about 10 kHz by connecting external resistors and capacitors.
AMP2	Operational amplifier for adjusting the receiving voice signal and tone signal gain, and preventing SCF aliasing in subsequent stages. Set the gain at 30 dB or lower and the cut-off frequency at about 10 kHz by connecting external resistors and capacitors.
Pre-emphasis	Circuit which emphasizes the high frequency component of transmitting voice signals to improve the modulation signal's S/N.
BPF1	SCF circuit which limits the band of input voice signals to 300~3,000 Hz. This prevents voice signals below 300 Hz from having an adverse effect on the tone signals during transmitting. The tone signal is removed during receiving and only the voice signal is output.
DBM	Carrier suppression modulation circuit for scrambler. The carrier frequency is 3.339 kHz.
LPF1	Circuit which removes the high frequency component generated by the DBM and outputs a low frequency component only. Inverting the frequency of the signal input to the DBM.
AMP3	Operational amplifier for adjusting the level of signals input to the limiter, and adding the tone signal and voice signal together.
Limiter	An amplitude limiting circuit for the purpose of inhibiting frequency shift of the modulation signal. The limit level can be adjusted by the DC voltage applied to the LIMLV pin. If the LIMLV pin is made open, the limit level is a predetermined level.
Splatter Filter	A SCF circuit which removes the component above 3 kHz included in the limiter output signal.

Block	Function
AMP4	An operational amplifier for the purpose of configuring a smoothing filter for the transmitting SCF circuit. Set the gain at 0 dB and the cut-off frequency at about 10 kHz by connecting external resistors and capacitors.
De-emphasis	Circuit which restores signals which were given high frequency emphasis by the pre-emphasis circuit to their former level.
Control Register	Circuit which is used to input and store control signals for switching the CTCSS tone frequency, transmit/receive, etc.
ROM	Circuit which creates dividing ratios supplied to the program divider for creating the 50 tone signal frequencies in accordance with control signals stored in the control register.
Programmable Divider	Circuit which generates the clock signals required for generating and detecting the 50 tone signal frequencies.
Oscillator Circuit	By connecting an external crystal oscillator, resistors and capacitors, this circuit can generate a clock frequency of 3.6864 MHz.
AMP6	Operational amplifier used to adjust the gain of signals input to the TSQLPF and in configuring an anti-aliasing filter. If digital signals like those generated by a microcontroller or similar device are input, a signal which has been band limited by the TSQLPF can be output to TXTONE.
TSQLPF	Programmable filter which converts square waves from the programmable divider to sine waves and performs band limitation of signals from AMP6 during transmitting. During receiving, it extracts the tone signal from the received signals.
AMP7	Operational amplifier which amplifies the tone signal from the TSQLFP and applies it to the TSQLIM. The minimum receiving tone detection level is set by connecting external resistors and capacitors.
TSQLIM	Circuit which performs amplitude limiting of the tone signal.
TSQBPF	Narrow band pass filter for identifying the 50 tone signal frequencies. The center frequency is changed by the clock frequency from the programmable divider.
DETECT	Circuit which judges if a tone is present or not from the TSQBPF output signal.
AGND	Circuit for generating a reference voltage for internal analog circuits.
BIAS GEN	Circuit which determines the operating current of the operational amplifiers used internally.
AMP8	Uncomitted CMOS operational amplifier
COMP	Uncomitted CMOS comparator

Pin/Function

Pin No.	Pin Name	I/O	Function
1	TXINO	O	AMP1 output pin. This pin can drive a 30kΩ or greater load.
2	TXIN	I	Transmitting voice input pin. Inverting input of AMP1. A mic amp can be configured by connecting external resistors and capacitors.
3	AMPP	I	AMP8 non-inverting input pin.
4	AMPN	I	AMP8 inverting input pin.
5	AMPO	O	AMP8 output pin. This pin can drive a 10kΩ or greater load.
6	SPOUT	O	Splatter filter output pin.
7	MODIN	I	Transmit modulation signal input pin. This is the inverting input for AMP4. A smoothing filter is configured by connecting external resistors and capacitors.
8	MOD	O	Transmit modulation signal input pin. This pin can drive a 10kΩ or greater load.
9	AVSS	–	Analog negative power supply pin.
10	DEOUT	O	De-emphasis output pin.
11	RXAFIN	I	Receiving voice input pin. Inverseting input for AMP5. A smoothing filter is configured by connecting external resistors and capacitors.
12	RXAF	O	Receiving voice output pin. This pin can drive a 10kΩ or greater load.
13	DVDD	–	Digital positive power supply pin.
14	RSTN	I	Reset signal input pin. By setting this pin to "L", the internal register value, the divider value, etc. are initialized. Reset puts the IC to the standby mode.
15	STB	I	Strobe signal input pin for serial data.
16	SCLK	I	Clock input pin for serial data.
17	SDATA	I	Serial data input pin. 8 bit serial data are input to this pin for setting the operating mode, CTCSS tone frequency, etc.
18 19	XIN XOUT	I O	Crystal oscillator connection pins. By connecting a 3.6864 MHz oscillator across these 2 pins, a reference clock for internal use of the IC is created. If an external clock signal is supplied, XOUT is made open and the clock is connected to XIN.
20 21	TOUT1 TOUT2	O O	Test signal output pin. These pins are used for LSI testing. Do not connect them to anything. During normal operation, no signal is output.

Pin No.	Pin Name	I／O	Function
22	DETOUT	O	Tone detect signal output pin. (Open drain output) In the Receive mode, this pin goes "L" when a tone at the frequency set by serial data is detected. In the Transmit mode, the impedance at this pin is always high.
23	COMPO	O	COMP output pin. (Open drain output) Comparator output pin.
24	DVSS	−	Digital negative power supply pin.
25	COMPN	I	COMP inverting input pin.
26	COMPP	I	COMP non-inverting input pin.
27	AVDD	−	Analog positive power supply pin.
28	TSBPFO	O	Tone squelch band pass filter output pin. TSQBPF output pin. It extracts and outputs the desired tone signal.
29	DREF	I	Tone detect level adjust pin. This pin determines the tone decoder's threshold level when a DC voltage higher than the AGND potential is applied to it. Normally, a voltage of approximately 1.16 V is applied at VDD = 2.0 V.
30	TLINO	O	AMP3 output pin. This pin can drive a 10kΩ or greater load.
31	TLIN	I	Receiving tone signal input pin. AMP3 inverting input pin. The minimum detection level for the receiving tone is set by connecting external resistors and capacitors.
32	RXTONE	O	Receiving tone signal output pin. TSQLPF output pin. In the Receive mode, the tone signal is taken from the receiving signal from DEM.
33	TXTONE	O	Transmit tone signal output pin. In the Transmit mode, a tone set by serial data is output by this pin. In the Receive mode, the AGND potential is output. In standby, the impedance at this pin goes high. This pin can drive a 10kΩ or greater load.
34	DCSINO	O	AMP6 output pin. This pin can drive a 30kΩ or greater load.
35	DCSIN	I	DCS signal input pin. AMP6 inverting input pin. DCS signal level adjustment is accomplished by connecting external resistors and capacitors.
36	TAGND	O	Tone squelch system analog ground pin. A 1/2 VDD voltage is output as a reference voltage for the CTCSS encoder/decoder's analog circuit. Connect a capacitor to stabilize the analog ground.
37	AGNDIN	I	Analog ground input pin. Connect a capacitor to stabilize the analog ground.

Pin No.	Pin Name	I／O	Function
38	BIAS	I	Bias resistor connection pin. Connect a resistor with a value determined by the power supply voltage between this pin and VSS.
39	AGND	O	Voice system analog ground pin. A 1/2 VDD voltage is output as a reference voltage for the analog circuitry of the voice filter, scrambler circuit, etc.
40	RXIN	I	Receiving demodulated signal input pin. This is the AMP2 inverting input pin. Connect external resistors and capacitors to configure a pre-filter.
41	RXINO	O	AMP2 output pin. This pin can drive a 30kΩ or greater load.
42	LIMINO	O	AMP3 output pin.
43	LIMIN	I	Limiter input pin. AMP3 inverting input pin. The transmitting voice signal applied to this pin through external resistors. The transmitting tone signal can also be added.
44	TXOUT	O	Transmitting voice signal output pin.
45	LIMLV	I	Limiter level adjustment pin. The limit level can be adjusted by applying the DC voltage to this pin. If no connections are made, the pre-determined limiter level is set.
46	LIMBS	I	Limiter level fine adjustment pin. By applying a DC voltage to this pin, fine adjustment of the lower limit limiter level can be done and the limiter's symmetry can be adjusted.
47	DBMIN	I	Balanced modulator input pin.
48	BPFOUT	O	Band pass filter output pin. BPF1 output pin. Connected to the DBMIN pin through a capacitor.

Absolute Maximum Ratings

Parameter	Symbol	min	max	Units
Power Supply Voltage : (AVDD, DVDD)	VDD	-0.3	7	V
Ground Level	VSS	0	0	V
Input Current(Except power supply pin)	I_{IN}	-10	+10	mA
Analog Input Voltage	V_{AIN}	-0.3	VDD+0.3	V
Digital Input Voltage	V_{DIN}	-0.3	VDD+0.3	V
	V_{DINO} Note 2)	-0.3	7	
Storage Temperature	Tstg	-55	130	℃

Note: All voltage values are with respect to the VSS pin.
Note 2): Applicable to DETOUT and COMPO.
Caution: If used under conditions which exceed these values, the device may be destroyed and nomal operation cannot be guaranteed under this extremes.

Recommended Operating Conditions

Parameter	Symbol	min	typ	max	Unit
Operating Temperature	Ta	-30		70	℃
Power Supply Voltage: R_{BIAS}= 75kΩ	VDD	1.8	2.0	2.5	V
(AVDD, DVDD) R_{BIAS}=330kΩ		4.5	5.0	5.5	
Analog Reference Voltage	AGND		1/2VDD		V
Current Consumption					
DCS=1, STBY=1 (Mode 0)	Idd0		0.01	0.1	mA
DCS=0, STBY=1 (Mode 1)	Idd1		3.4	7.2	
RX/TX=1, STBY=0 (Mode 3)	Idd2		4.6	10	

Note: All voltage values are with respect to the VSS pin.

Digital Characteristics

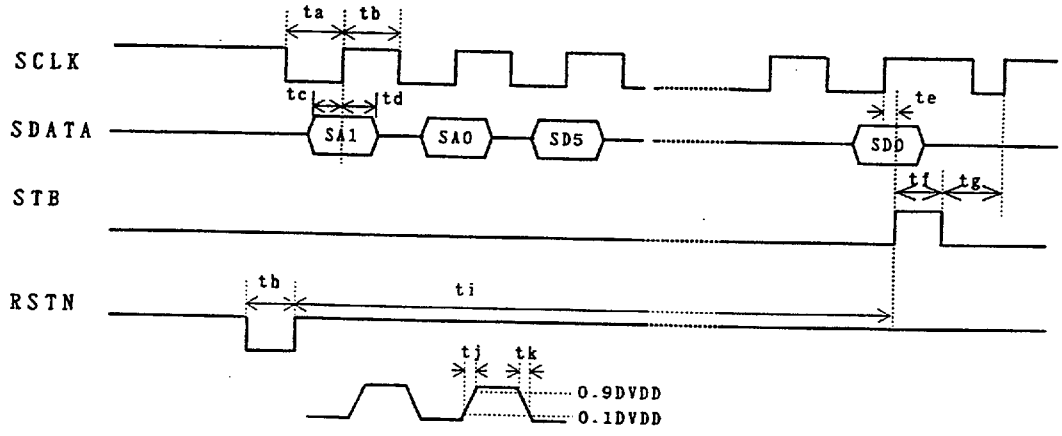
1. DC Characteristics

Parameter	Terminal	Symbol	min	typ	max	Units
High Level Input Voltage	(1)	V_{IH}	70%VD+			V
Low Level Input Voltage	(1)	V_{IL}			30%VD+	V
High Level Input Current V_{IH}=VD+	(1)	I_{IH}			10	μA
Low Level Input Current V_{IL}=0V	(1)	I_{IL}	10			μA
Low Level Output Voltage I_{OL}=0.8mA	(2)	V_{OL}			0.3	V

(1)SDATA, SCLK, STB
(2)DETOUT, COMPO

2. AC Characteristics

Parameter	Symbol	min	typ	max	Units
Master Clock Frequency	fclk		3.6864		MHz
Serial data input timing					
Clock Pulse Width 1	ta	500			ns
Clock Pulse Width 2	tb	500			ns
SDATA Set Up time	tc	100			ns
SDATA Hold time	td	100			ns
STROBE Set up time	te	100			ns
STROBE pulse width	tf	100			ns
STROBE dehold time	tg	100			ns
RESET pulse width	th	1.3			μs
RESET cancel time	ti	500			ns
digital input rising time	tj			250	ns
digital input falling time	tk			250	ns



Serial Data Input

Analog Characteristics

0dBm=0.775Vrms
0dBx=-5dBm at AVDD=2V

1) TX System

Note 6)

Parameter		min	typ	max	Units
Standard Input Level	@TXINO		-10		dBx
Absolute Gain	TXINO→MOD 1kHz Note 1)	-1.5	0	1.5	dB
Maximum Output Level	@LIMINO	0			dBx
Limiter Level	TXINO→MOD 1kHz Note 1) No external R Adjustment range when external R connected	-9	-8	-7 -7	dBx
Noise Level	TXIN→MOD Note 1)			-58	dBm
Transmit Tone Output Level	@TXTONE	-12	-10	-8	dBx
Transmit Tone Frequency Shift	@TXTONE	-0.3		+0.3	%
Transmit Tone Distortion	@TXTONE		-35	-26	dB
DCS Signal Gain	DCSINO→TXTONE	-2	0	+2	dB
Maximum DCS Signal Input Level	@DCSINO	0			dBx

2) RX System

Parameter			min	typ	max	Units
Standard Input Level	@RXINO			-10		dBx
Absolute Gain	RXINO→RXAF 1kHz Note 2)		-1.5	0	1.5	dB
Maximum Output Level	@RXAF		0			dBx
Noise Level	RXINO→RXAF Note 2)				-55	dBm
Receiving Tone Detection Level	Note 3) RXINO→DETOUT		-38			dBx
Receiving Tone Nondetection Level	Note 4) RXINO→DETOUT				-18	dBx
Receiving Tone Detection Time	Note 5) RXINO→DETOUT	@100Hz			250	ms
		@67Hz			370	ms

3) Operational Amplifiers

Parameter			min	typ	max	Units
Gain Error	AMP1~8	60Hz~3.4kHz Gain 0~30dB	-1	0	1	dB

4) Filter Characteristics

Parameter		min	typ	max	Units
Transmitting Overall Characteristic	250Hz			-40	
(See Fig. 1) TXINO → MOD	300Hz	-13.5		-9.5	
Scrambler bypass with	2.5kHz	5	8.1	9	dB
De-emphasis, Relative value	3kHz	5	7.5	10.5	
When gain at 1kHz is set at 0dB	3.6kHz			-36	
Receiving Overall Characteristic	250Hz			-26	
(See Fig. 2) RXINO → RXAF					
Scrambler bypass with	300Hz	7.5	10	11.5	dB
Pre-emphasisz, Relative value	3kHz	-12.5	-10.1	-8.5	
When gain at 1kHz is set at 0dB	3.6kHz			-40	

Note 1) With pre-emphasis. Scrambler bypass. Refer to the external circuit example.
Note 2) With de-emphasis. Scrambler bypass. Refer to the external circuit example.
Note 3) Frequency shift within + 0.5% Refer to the external circuit example.
Note 4) Frequency shift within +3.0% (When the TSQBPF Q value is "H") Refer to the external circuit example.
Note 5) When -20 dBx Refer to the external circuit example.
Compatible with the EIA RS-220A
Note 6) dBx is standardized so that it can correspond to all voltages between 1.9~5.5 V. When the voltage is 2 V, 0 dBx = -5 dBm. If we let the voltage be X [V], then
0 dBx = -5 + 20log(X/2) [dBm].

Scrambler Characteristics

Parameter	min	typ	max	Units
Carrier Frequency		3.339		kHz
Modulated Output Level TXINO→TXOUT Input 1kHz -10dBx Measured Frequency 2.339kHz Note 1)	-12	-10	-8	dBx
High Frequency Rejection Level TXINO→TXOUT Input 1kHz -10dBx Measured Frequency 4.339kHz Note 1)			-50	dBx
Carrier Frequency Leakage Level @TXOUT No Input Measured Frequency 3.339kHz Note 1)			-50	dBx
Original Tone Leakage Level TXINO→TXOUT Input 1kHz -10dBx Measured Frequency 1kHz Note 1)			-50	dBx

Note 1) With Pre-emphasis and scrambler

□Filter Characteristics

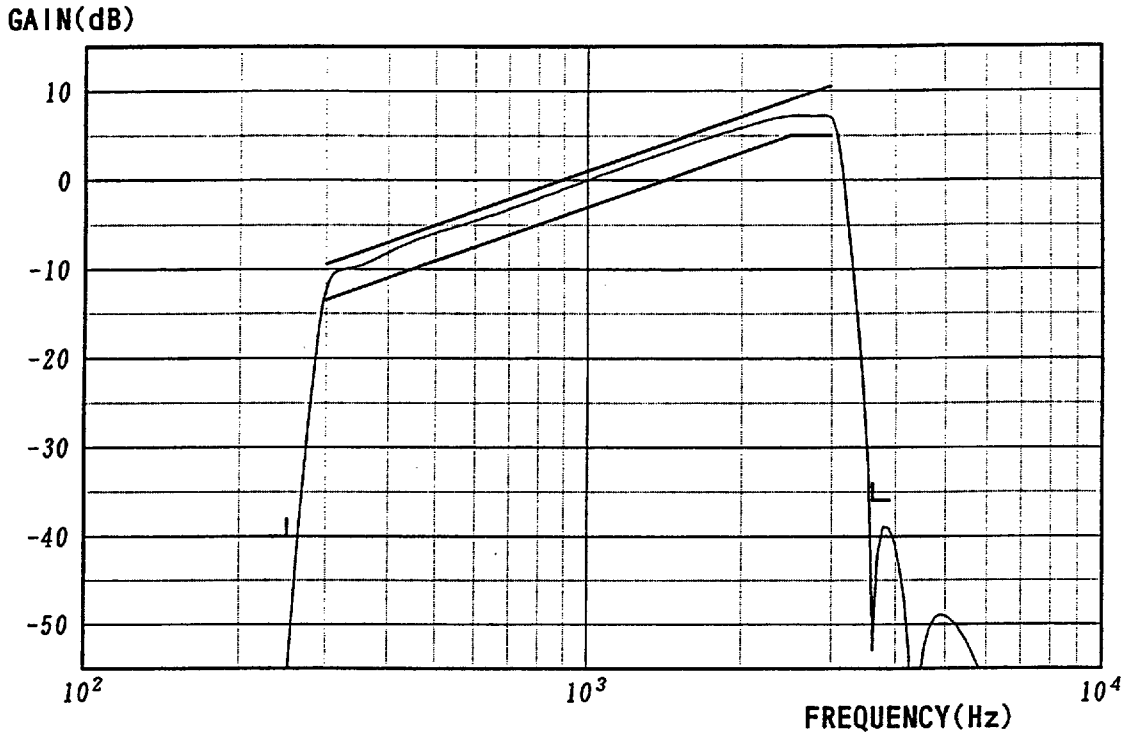


Fig. 1 Transmitting Overall Characteristic

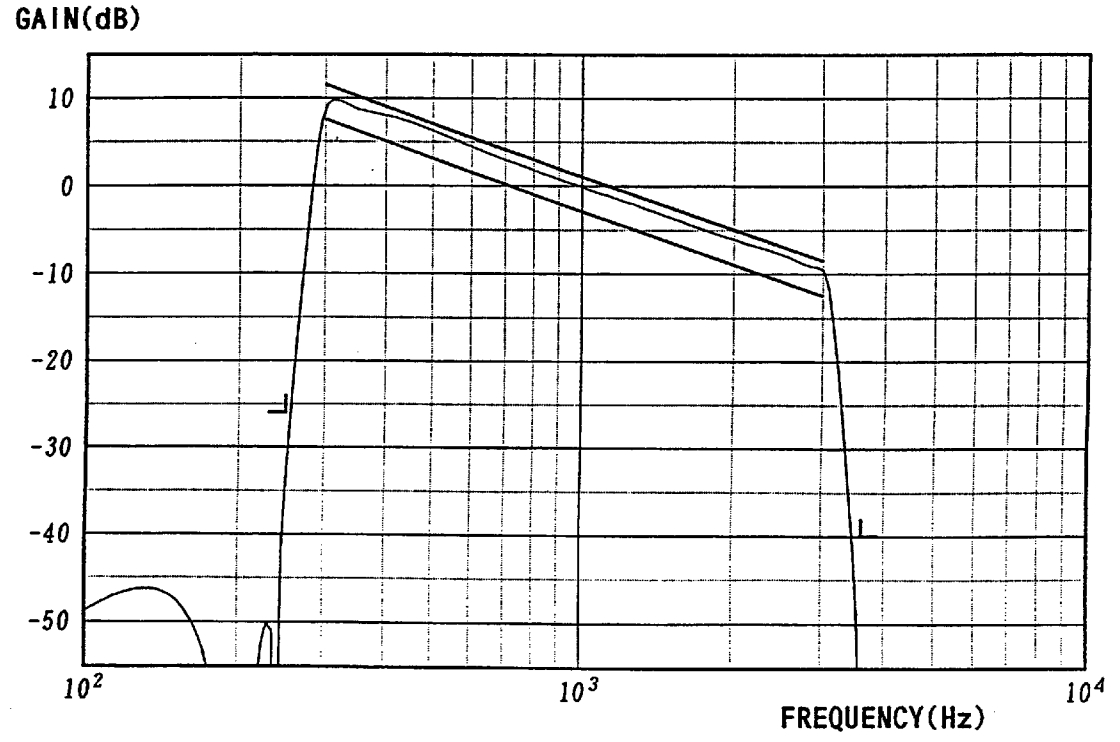


Fig. 2 Receiving Overall Characteristic

Serial Interface Configuration

The various modes and the CTCSS tone frequency of the AK2342A are set by writing data to the control register from the serial interface pints (SDATA, SCLK, STB). Serial data are configured from two address bits and six data bits, for a total of eight bits.

■Register Configuration

Address		Data					
SA1	SA0	SD5	SD4	SD3	SD2	SD1	SD0
0	0	Setting of modes and internal switches					
0	1	Setting of the voice signal path					
1	0	Not used					
1	1	Setting of the tone frequency					

■Register Map

1) Setting of Modes and Internal Switches

Address		Data					
SA1	SA0	SD5	SD4	SD3	SD2	SD1	SD0
0	0	TST	DCS	RVTN	RXON	RX/TX	STBY
At Reset		1	1	1	1	1	1

Data Name	Function	
STBY	Standby mode control.	"1" : Standby Mode "0" : Normal Operation
RX/TX	Selects the Transmit or Receive mode.	"1" : Receive Mode "0" : Transmit Mode
RXON	Receiving voice signal control.	"1" : On or Off according to the presence or absence of a receiving tone. "0" : Normally On.
RVTN	Transmit tone phase control.	"1" : Positive Phase (0°) "0" : Negative Phase (180°)
DCS	Switches between CTCSS and DCS.	"1" : CTCSS Mode "0" : DCS Mode
TST	Test mode control.	"1" : Normal Operation "0" : Test Mode

2) Setting of the Voice Signal Path

Address		Data					
SA1	SA0	SD5	SD4	SD3	SD2	SD1	SD0
0	1	–	–	–	DE	PE	PCONT
At Reset		–	–	–	1	1	1

Data Name	Function	
PCONT	Scrambler control.	"1" Bypass "0" Scrambler operates.
PE	Pre-emphasis circuit control.	"1" Bypass "0" Pre-emphasis circuit operates.
DE	De-emphasis circuit control.	"1" Bypass "0" De-emphasis circuit operates.

3) Setting of the Tone Frequency

Address		Data						Tone Frequency (Hz)	TSQBPF Q Value
SA1	SA0	SD5	SD4	SD3	SD2	SD1	SD0		
1	1	0	0	0	0	0	1	67.0	L
		0	0	0	0	1	0	71.9	L
		0	0	0	0	1	1	77.0	L
		0	0	0	1	0	0	82.5	L
		0	0	0	1	0	1	88.5	L
		0	0	0	1	1	0	94.8	H
		0	0	0	1	1	1	100.0	H
		0	0	1	0	0	0	103.5	H
		0	0	1	0	0	1	107.2	H
		0	0	1	0	1	0	110.9	H
		0	0	1	0	1	1	114.8	H
		0	0	1	1	0	0	118.8	H
		0	0	1	1	0	1	123.0	H
		0	0	1	1	1	0	127.3	H
		0	0	1	1	1	1	131.8	H
		0	1	0	0	0	0	136.5	H
		0	1	0	0	0	1	141.3	H
		0	1	0	0	1	0	146.2	H
		0	1	0	0	1	1	151.4	H
		0	1	0	1	0	0	156.7	H
		0	1	0	1	0	1	162.2	H
		0	1	0	1	1	0	167.9	H
		0	1	0	1	1	1	173.8	H
		0	1	1	0	0	0	179.9	H
		0	1	1	0	0	1	186.2	H
		0	1	1	0	1	0	192.8	H
		0	1	1	0	1	1	203.5	H
		0	1	1	1	0	0	210.7	H
		0	1	1	1	0	1	218.1	H
		0	1	1	1	1	0	225.7	H
		0	1	1	1	1	1	233.6	H
		1	0	0	0	0	0	241.8	H
		1	0	0	0	0	1	250.3	H
		1	0	0	0	1	0	67.0	H
		1	0	0	0	1	1	71.9	H
		1	0	0	1	0	0	74.4	H
		1	0	0	1	0	1	77.0	H
		1	0	0	1	1	0	79.7	H
		1	0	0	1	1	1	82.5	H
		1	0	1	0	0	0	85.4	H
		1	0	1	0	0	1	88.5	H
		1	0	1	0	1	0	91.5	H
		1	0	1	0	1	1	97.4	H
		1	0	1	1	0	0	69.4	H
		1	0	1	1	0	1	159.8	H
		1	0	1	1	1	0	165.5	H
		1	0	1	1	1	1	171.3	H
		1	1	0	0	0	0	177.3	H

Address		Data						Tone Frequency (Hz)	TSQBPF Q Value
SA1	SA0	SD5	SD4	SD3	SD2	SD1	SD0		
1	1	1	1	0	0	0	1	183.5	H
		1	1	0	0	1	0	189.9	H
		1	1	0	0	1	1	196.6	H
		1	1	0	1	0	0	199.5	H
		1	1	0	1	0	1	206.5	H
		1	1	0	1	1	0	229.1	H
		1	1	0	1	1	1	254.1	H
		1	1	1	0	0	0	Note 1)	–
At Reset		1	1	1	1	1	1	OFF	–

Note 1) Valid when in the DCS Transmit mode only. The TSQLPF cut-off frequency is 3.24kHz.
Note 2) If a code other than the above is input, the potential at the TXTONE pin changes to the AGND potential when in the Transmit mode and DETOUT goes "L" when in the Receive mode.

Explanation Operation

1) Mode of Operation

The operation modes of the AK2342A are determined by 4 logical combinations of four bits, STBY, RX/TX, DCS and TST, out of the 6 bits of serial data selected by address "00". (See Table 1.) Further, control of voice signal output or tone signal output can be accomplished through the four bits related to the voice operation mode, Transmit mode and Receive mode, RX/TX, RXON, RVTN and DCS. (See Table 2, Table 3 and Table 4.)

TST	DCS	RVTN	RXON	RX/TX	STBY	Operation Mode	Description of Operation
0	×	×	×	×	×	Test Mode	This mode is used to test the IC at the time it is shipped.
1	1	×	×	×	1	Standby Mode (Mode 0)	In this mode, the oscillator circuit stops and analog output enters the high impedance state, reducing power consumption.
1	0	×	×	×	1	Voice Operation Mode (Mode 1)	The scrambler, voice filter, and other voice signal systems only operate. CTCSS circuit operation is stopped, reducing current consumption.
1	×	×	×	0	0	Transmit Mode (Mode 2)	Voice signals from TXAF pass through BPF1 or another voice filter are output to MOD. A tone signal set according to the tone frequency setting code or a DCS signal is output to TXTONE. The potential at the DEOUT pin becomes the AGND potential and DETOUT goes "H".

TST	DCS	RVTN	RXON	RX/TX	STBY	Operation Mode	Description of Operation
1	×	×	×	1	0	Receive Mode (Mode 3)	If a tone with the frequency set in accordance with the tone frequency setting code is detected from signals input to DEM or DCS, DETOUT goes "L". The tone signal is removed at RXOUT and only the voice signal is output. The potential at the TXOUT pin becomes the AGND potential.

Table 1

Signal Control When in the Voice Operation Mode

Data Name	Function
RX/TX	Switching between Transmit and Receive. "1" : Receiving system operates. "0" : Transmit system operates.

Table 2

Signal Control When in the Transmit Mode

Data Name	Function
RVTN	TXTONE pin Phase control. "1" : Positive Phase (0°) "0" : Negative Phase (180°)
DCS	TXTONE pin signal control. "1" : CTCSS Signal "0" : DCS Signal

Table 3

Signal Control when in the Receive Mode

Data Name	Function
RXON	DEOUT pin control. "1" : Switches On and Off according to the presence or absence of a receiving tone. "0" : Normally On
DCS	TSQLPF input signal control. "1" : AMP2 output signal. "0" : AMP6 output signal.

Table 4

2) Tone Frequencies

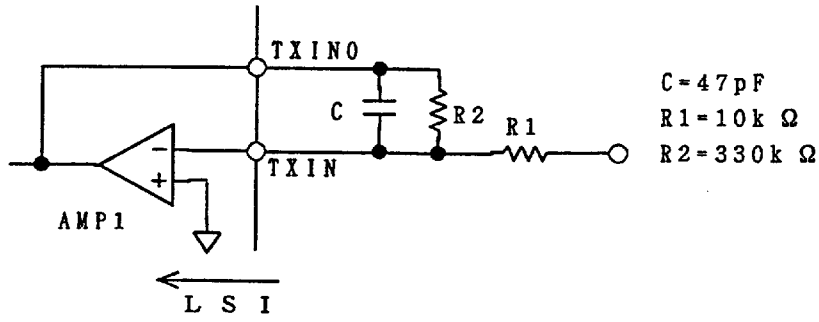
50 tone frequencies can be selected from a frequency range of 67.0 ~ 254.1 Hz. Of these, Q value of "L" or "H" can be selected in case of 67.0, 71.9, 77.0, 82.5, and 88.5 Hz. If "L" is selected, the detection time can be shortened, but it is difficult to distinguish neighboring frequencies (84.5 Hz or 91.5 Hz from 88.5 Hz). The Q value of the other frequencies are "H". In order to stop the transmitting tone signal stopped, set the code for a value other than those shown in the tone frequency setting table. (Example: Set SD0 ~SD5 all at "0".)

Examples of Application Circuit

■ Examples of External Circuit

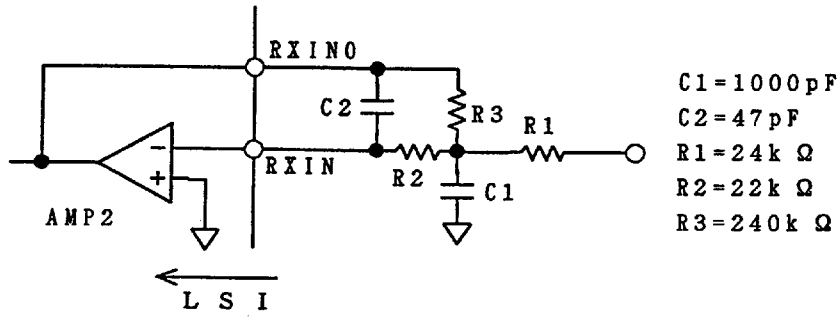
◎ AMP1

This can be used as a transmitting mic amplifier. Set the gain at 30 dB or lower. If there is a possibility of noise from the frequency band below 80 kHz being input, configure an anti-aliasing filter. The following diagram shows a configuration example of a 1st order low pass filter with a gain of 30 dB and a cut-off frequency of 10 kHz.



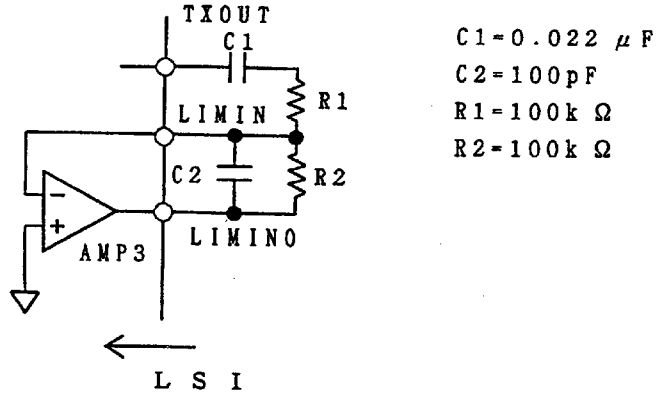
◎ AMP2

This amp can be used to adjust the receiving signal gain and to configure an anti-aliasing filter for cutting off noise above 80 kHz. Set the gain at 30 dB or lower. The following diagram shows an example of a second order low pass filter configuration with a gain of 20 dB and a cut-off frequency of 10 kHz.



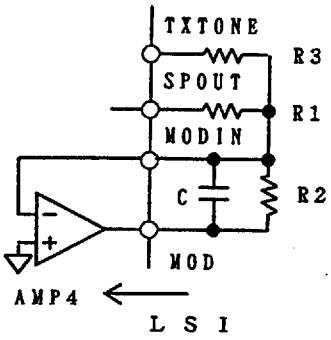
◎ AMP3

By changing the gain of this amplifier, the signal level input to the limiter can be changed. The DC offset of the TXOUT output can be reduced by capacitor coupling. The following diagram shows an example of a 1st order low pass filter configuration with a gai n of 0 dB and a cut-off frequency of 16 kHz.



◎ AMP4

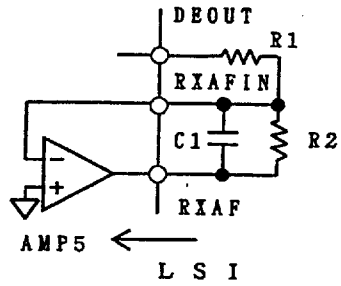
This amplifier is used to adjust the transmitting signal gain and configure a smoothing filter. The smoothing filter is used to cut the 80 kHz clock component included in signals at SPOUT. This amp can also be used to add the voice signal and tone signal. The following diagram shows an example of a 1st order low pass filter configuration with a gai n of 0 dB and a cut-off frequency of 13 kHz.



C=220pF
R1=R2=56k Ω
R3=330k Ω

◎ AMP5

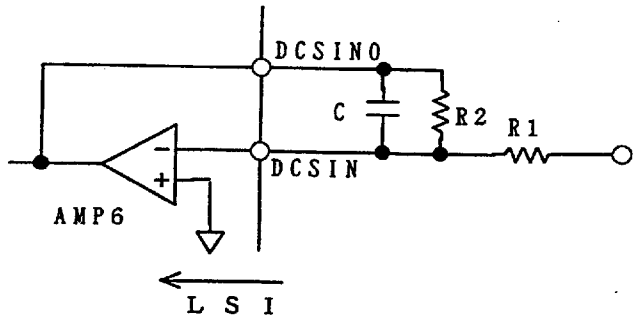
This amplifier is used to adjust the receiving signal gain and configure a smoothing filter. The smoothing filter is used to cut the 80 kHz clock component included in signals at DEOUT. This amp can also be used to add signals from other sources. The following diagram shows an example of a 1st order low pass filter configuration with a gai n of 0 dB and a cut-off frequency of 13 kHz.



C1=220pF
R1=R2=56k Ω

◎ AMP6

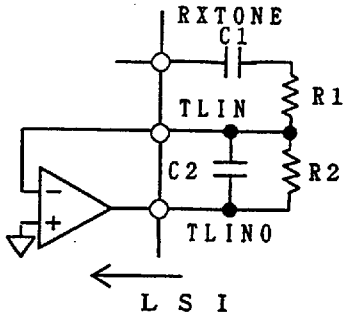
This amp is for the purpose of adjusting the gain of the DCS (Digitally Coded Squelch) signal and configuring an anti-aliasing filter to cut noise above 80 kHz. The following diagram shows an example of a 1st order low pass filter configuration with a gain of -13.7 dB and a cut-off frequency of 13 kHz.



C=220pF
R1=270k Ω
R2=56k Ω

◎ AMP7

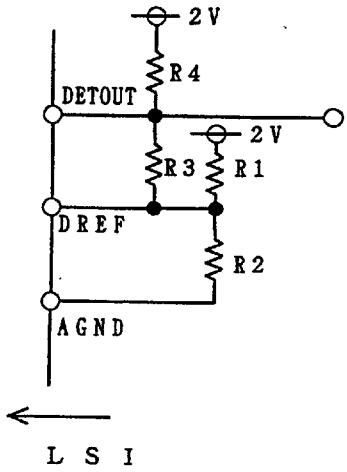
By changing the gain of this amplifier, the minimum detection level of the receiving tone detection circuit can be changed. Configure the constants in the following diagram in order to satisfy the specifications in the data sheet.



C1=4.7 μF
C2=100pF
R1=5.6k Ω
R2=270k Ω

◎ Receiving Tone Detection Circuit Threshold Level

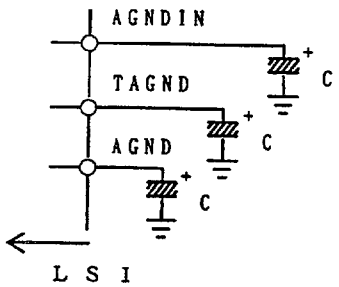
The threshold level of the receiving tone detection circuit is determined by inputting DC signals with a higher potential than the AGND potential to the DREF pin. If V_{DD} = 2.0 V, apply a voltage of approximately 1.16 V. If some hysteresis is desired in the detection sensitivity, feed back DETOUT pin signal. The following diagram shows an example with approximately 3 dB of hysteresis. If the threshold level is changed the tone detection time also changes. If the threshold level is made high, the detection time becomes longer and if it is made low, the detection time becomes shorter.



R1=22k Ω
R2=3.9k Ω
R3=150k Ω
R4=15k Ω

◎ AGND Stabilization Capacity

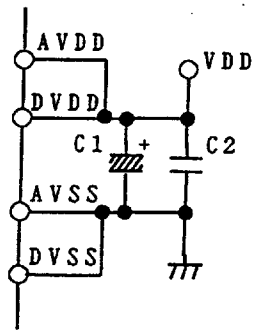
Connect a 0.3 uF or higher capacitor between the AGND pin and VSS to stabilize the AGND level. Also connect a capacitor with the appropriate value between AGNDIN and VSS to eliminate the ripple effect in the power supply. A connection example is shown in the following diagram.



C=1 μF

◎ Power Supply Stabilization Capacity

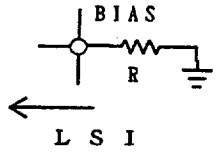
In order to minimize the effect of power supply noise, connect a capacitor between VDD and VSS. Position the capacitor so that it is as close as possible to the power supply pin.



C1=22 μF (electrolytic capacitor)
C2=0.1 μF (ceramic capacitor)

◎ Bias Current Setting Resistor

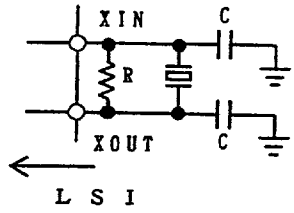
Connect a resistor between BIAS and VSS and set the bias current of the operational amplifiers. When VDD = 2 V, use a 75 kΩ resistor. When VDD = 3 V, use a 160 kΩ resistor. When VDD = 5 V, use a 330 kΩ resistor.



R= 75k Ω (VDD=2V)
R=160k Ω (VDD=3V)
R=330k Ω (VDD=5V)

◎ Crystal Oscillator

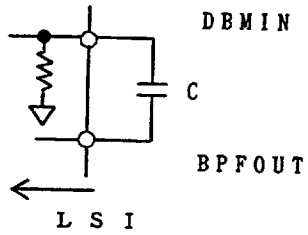
If the internal oscillator circuit is used, connect a crystal oscillator and resistor as shown in the following diagram. If an external clock is used, leave XOUT open and supply the clock signal to XIN. Be careful not to let the clock's amplitude exceed the absolute maximum rating.



Oscillator Frequency : 3.686
R=1M Ω
C=22pF

◎ DC Cut Capacity

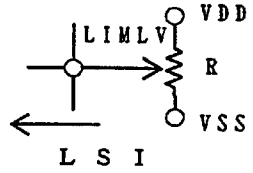
In order to cut the DC offset generated at BPF1, connect a capacitor between BPFOUT and DBMIN.



C=0.022 μF

◎ Limiter Level Setting Resistor

If the limiter level is to be adjusted externally, apply DC voltage to the LIMLV pin as shown in the following diagram. The DC voltage applied should be greater than the TAGND voltage and if we let the voltage between LIMLV and TAGND be a V, the limit level becomes TAGND ± a V. If LIMLV is left open, the limit level becomes the pre-determined limit level. The lower limiter level can be fine tuned and the limiter's non-symmetry corrected by applying DC voltage to the LIMBS pin.



R=50k Ω

Package

■ Markings

(1) Pin No. 1 Indication (The pin at the chamfered corner is pin No. 1.)
(2) Date Code : XXXXX (5 digits)
First 3 digits : Week code
Last 2 digits : In-house control code
(3) Marketing Code : AK2342AV
(4) Country of Manufacture Indication : Japan
(5) Asahi Kasei Logo

■ Package External Dimensions