AKM

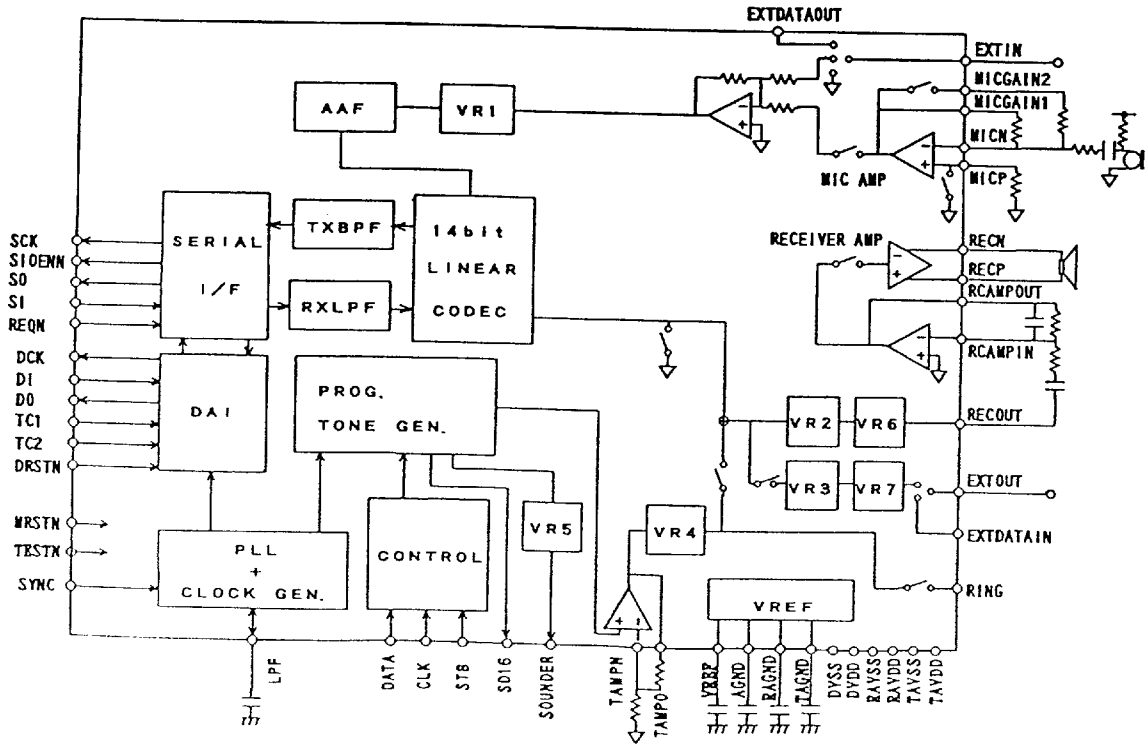
-Preliminary- AK2376A

AUDIO INTERFACE LSI FOR DIGITAL CELLULAR

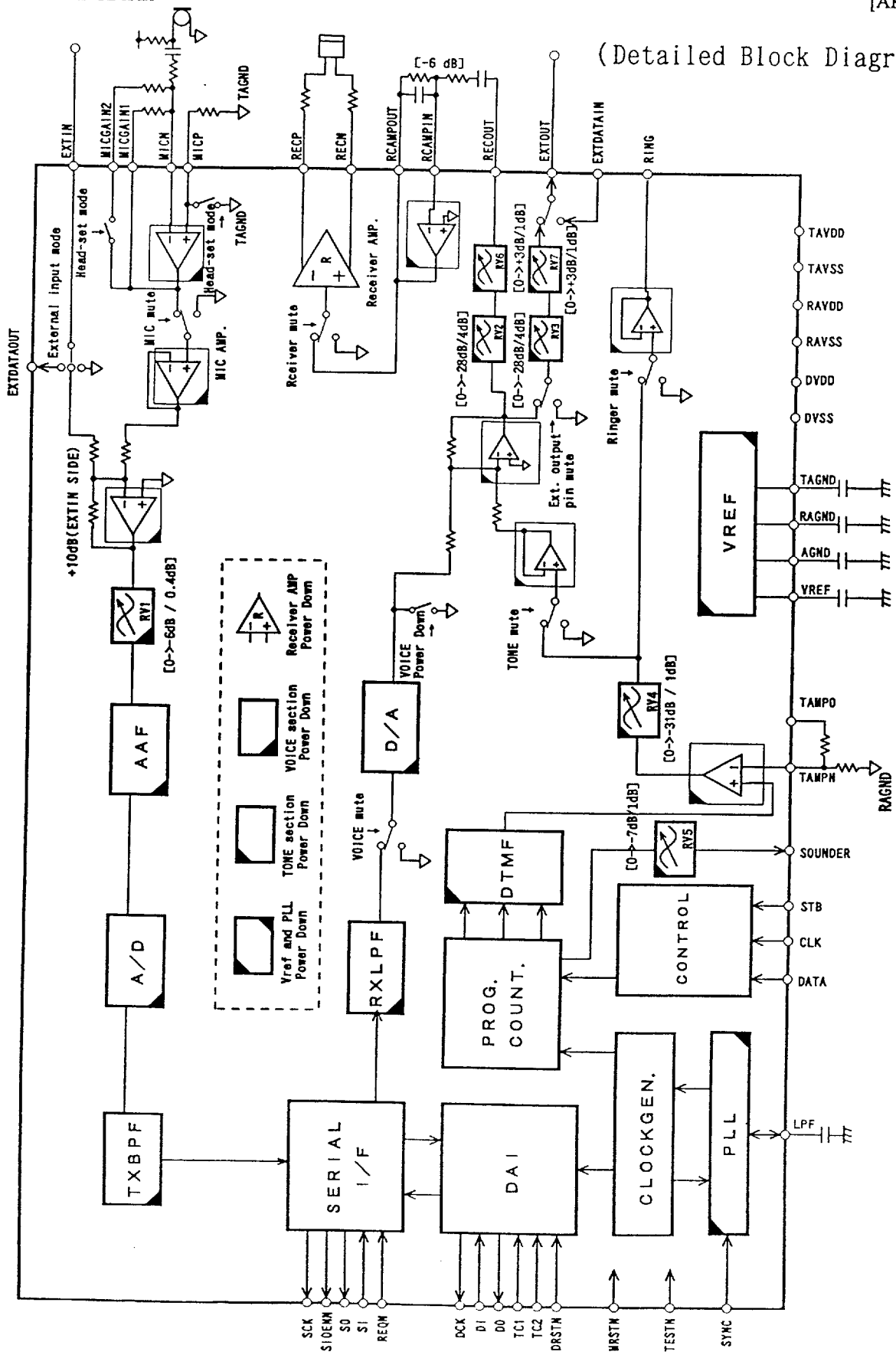
Features

- Suitable for audio interface of digital cellular
- 14bit linear codec
- TX & RX filter, compliant with CCITT recommendation
- Triple tone (including DTMF) generator
- Serial data interface
- Digital audio interface
- Microphone and Ceramic receiver amplifier
- Analog reference voltage
- Clock generator
- Power down mode
- Single 2.7 – 5.5V power supply
- Power consumption 5mA (Typ.)
- 48pin SQFP package

Block Diagram



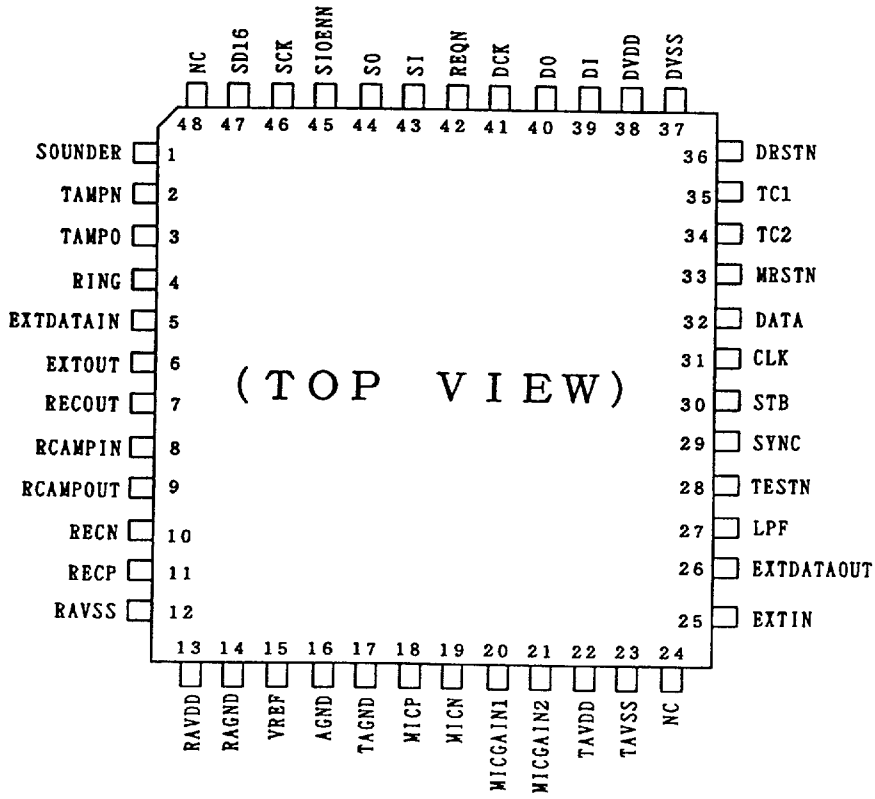
(Detailed Block Diagram)



General Description

The AK2376A is a CMOS LSI that is suitable for audio interface circuit of digital cellular. The AK2376A includes 14bit linear CODEC, TX and RX filters, tone generators, serial data interface, digital audio interface, control registers, clock generators, analog reference voltage ,electrical volumes and others.
The AK2376A can be operated at 3V. The external input (or output) pins of the AK2376A can be connected to the external connector of mobile station directly. When data signal (FAX data etc.) are input from (or output to) external connector, the signal can be output to (or input from) external circuits of mobile station through the external data input (or output) pins of the AK2376A.

■ Pin Assignment



Pin／Function

Pin #	Name	I／O	Function	Remarks
1	SOUNDER	O	Ringer output.	Note-2
2	TAMPN	I	Tone signal gain adjustment amplifier input.	Note-4
3	TAMPO	O	Tone signal gain adjustment amplifier output.	
4	RING	O	Key tone output.	Note-2
5	EXTDATAIN	I	External RX data input.	
6	EXTOUT	O	RX signal external output.	Note-2
7	RECOUT	O	RX signal output for gain adjustment.	Note-1 & 2
8	RCAMPIN	I	RX signal gain adjustment amplifier input.	
9	RCAMPOUT	O	RX signal gain adjustment amplifier output.	Note-1 & 2
10	RECN	O	Inverting output of receiver amplifier.	Connect to Ceramic Rec.
11	RECP	O	Non-inverting output of receiver amplifier.	
12	RAVSS	−	Ground for RX section.	
13	RAVDD	−	Power supply for RX section.	
14	RAGND	−	Analog ground for RX section.	
15	VREF	O	External capacitors connecting pin for adjusting internal operating current.	
16	AGND	−	Analog ground.	
17	TAGND	−	Analog ground for TX section.	
18	MICP	I	Non-inverting input of microphone amplifier.	
19	MICN	I	Inverting input of microphone amplifier.	
20	MICGAIN1	O	Microphone amplifier output for normal mode.	Note-4
21	MICGAIN2	O	Microphone amplifier output for head-set mode.	Note-4
22	TAVDD	−	Power supply for TX section.	
23	TAVSS	−	Ground for TX section.	
24	NC	−	no connection.	
25	EXTIN	I	TX signal external input.	
26	EXTDATAOUT	O	External TX data output.	
27	LPF	I／O	Loop filter connecting pin.	

Note-1 : Connect to external resistors for gain adjustment and capacitors for DC cutting.
Note-2 : This output can drive 50K Ω or larger, or 20pF or smaller.
Note-3 : This output can drive 50pF or smaller.
Note-4 : This output can drive 100K Ω or larger, or 5pF or smaller.
Note-5 : This output can drive 200K Ω or larger.

Pin #	Name	I / O	Function	Remarks
28	TESTN	I	TEST mode input (connect to DVDD)	
29	SYNC	I	8kHz reference clock input.	
30	STB	I	Control register strobe input.	
31	CLK	I	Control register clock input.	
32	DATA	I	Control register data input.	
33	MRSTN	I	Power on reset input. When set "L", this device goes to reset.	
34	TC2	I	DAI control input.	
35	TC1	I	DAI control input.	
36	DRSTN	I	DAI reset signal input. When set "L", the DAI section goes to reset.	
37	DVSS	–	Ground for digital section.	
38	DVDD	–	Power supply for digital section.	
39	DI	I	DAI serial data input.	
40	DO	O	DAI serial data output.	Note-3
41	DCK	O	104KHz DAI serial data clock output.	Note-3
42	REQN	I	Serial data request input.	
43	SI	I	Serial data (D/A data) input.	
44	SO	O	Serial data (A/D data) output.	Note-3
45	SIOENN	O	Serial data I/O enable output.	Note-3
46	SCK	O	208KHz serial data clock output.	Note-3
47	SD16	O	16Hz clock output.	
48	NC	–	no connection.	

Note-1 : Connect to external resistors for gain adjustment and capacitors for DC cutting.
Note-2 : This output can drive 50K Ω or larger, or 20pF or smaller.
Note-3 : This output can drive 50pF or smaller.
Note-4 : This output can drive 100K Ω or larger, or 5pF or smaller.
Note-5 : This output can drive 200K Ω or larger.

Absolute Maximum Ratings

Parameter	Symbol	min	max	Units
Power Supply Voltage (Note-1, 2)				
Digital Power Voltage	DVDD	-0.3	7.0	V
Analog Power Voltage	RAVDD	-0.3	7.0	V
	TAVDD			
Digital Input Voltage	V_{TD}	DVSS-0.3	DVDD+0.3	V
Analog Input Voltage	V_{TA}	RAVSS-0.3	RAVDD+0.3	V
		TAVSS-0.3	TAVDD+0.3	
Input Current	I_{IN}	-10	+10	mA
Storage Temperature	T_{stg}	-55	125	℃

Note-1 : RAVSS,TAVSS,DVSS = 0, all voltage with respect to ground.
Note-2 : When DVDD exceeds RAVDD and TAVDD, the device may be caused permanent damage.
Warning : Exceeding absolute maximum ratings may cause permanent damage.
Normal operation is not guaranteed at these extremes.

Recommended Operating Conditions

Parameter	Symbol	min	typ	max	Units
Power Supply Voltage (Note-1)					
Digital Power Voltage	DVDD	2.7		5.5	V
Analog Power Voltage	RAVDD	2.7		5.5	V
	TAVDD				
Ambient Operating Temperature	T_a	-30		85	℃

Note-1 : RAVSS,TAVSS,DVSS = 0, all voltage with respect to ground.

Electrical Characteristics

■ DC characteristics

Parameter	Symbol	Condition	min	typ	max	Unit
Power Consumption (Note-1)	I_{DD}	Normal operation mode		5		mA
	I_{DD1}	VOICE section power down mode		2.3		mA
	I_{DD2}	VOICE and TONE section power down mode		2.0		mA
	I_{DD3}	VOICE, TONE and Receiver AMP section power down mode		1.2		μA
	I_{DD4}	Full power down mode		200		μA
"H" input level (Note-2)	V_{IH}		0.7DVDD	—	—	V
"L" input level (Note-2)	V_{IL}		—	—	0.3DVDD	V
"H" input leak (Note-2)	I_{IH}	V_{IH}=DVDD	—	—	10	μA
"L" input leak (Note-2)	I_{IL}	V_{IL}=0V	-10	—	—	μA
"H" output level (Note-3)	V_{OH}	I_{OH}=-1mA	DVDD-1	—	—	V
"L" output level (Note-3)	V_{OL}	I_{OL}= 1mA	—	—	0.5	V

Note-1 : Supplying clocks. No load at all output pins. Input pins connect to DVDD or DVSS.
Analog input pins connect to AGND.
Note-2 : Pins are SI,REQN,DI,TC1,TC2,DRSTN,MRSTN,SYNC,DATA,CLK,STB and TESTN.
Note-3 : Pins are SCK,SO,DCK,DO,SIOENN and SD16.

■ Analog Characteristics

VDD = 2.7 ~ 5.5V,Ta = -30 ~ 85 ℃

Attenuation values are 0dB.

Parameter		Conditions		min	typ	max	Unit	Remarks
Signal to Total Distortion (A → D) EXTIN → SO		1020Hz Tone	-45dBm0	24	—	—	d B	With c-Wgt Filter (Note-1)
			-40dBm0	29	—	—		
			0, -30dBm0	35	—	—		
Signal to Total Distortion (D → A) SI → RECOUT		1020Hz Tone	-45dBm0	24	—	—	d B	With c-Wgt Filter (Note-1)
			-40dBm0	29	—	—		
			0, -30dBm0	35	—	—		
Gain Tracking (A → D) EXTIN → SO		1020Hz Tone	-55dBm0	-0.9	—	0.9	d B	Ref. level -10dBm0 (Note-1, 2)
			-50dBm0	-0.6	—	0.6		
			0, -40dBm0	-0.3	—	0.3		
Gain Tracking (D → A) SI → RECOUT		1020Hz Tone	-55dBm0	-0.9	—	0.9	d B	Ref. level -10dBm0 (Note-1, 2)
			-50dBm0	-0.6	—	0.6		
			0, -40dBm0	-0.3	—	0.3		
Idle Channel Noise		A-D	SO, EXTIN = AGND	—	—	20	dBrnc0	(Note-1)
Idle Channel Noise		D-A	RECOUT SI=ALL"0"	—	—	15		
Analog Input Level		1020Hz 0dBm0 Input	MIC→SO	—	0.501	—	Vrms	MICGAIN1 level = 0dB
			EXTIN→SO	—	0.158	—	Vrms	EXTIN level = 0dB
Analog Output Level			SI→EXTOUT		0.501		Vrms	
			SI→ RECP RECN	—	0.501	—	Vrms	RECOUT→ RCAMPOUT -6dB
Tone Output Level	TONE H	2KHz	→RING	-10.4	-8.9	-7.4	dBm	0dBm0 =0.775Vrms (Note-3)
			→EXTOUT	-10.9	-8.9	-6.9	dBm	
	TONE L TONE E		→RING	-12.6	-11.1	-9.6	dBm	
Tone Loss		TONE H 2KHz	→RING	15	—	21	dB	TNLOS=1 (Note-3, 4)
Tone Distortion		TONE H 2KHz	→RING	—	—	-29	dB	(Note-3)

Note-1 : I/O of control register and counters of tone generator section are disable.
Set TNMT=1 and MCMT=1.

Note-2 : Output at reference level (= -10dBm0) input is 0dB.

Note-3 : Measure in the condition that the loss from TAMPO to TAMPN is 0dB and the 3rd order butterworth L.P.F (cut-off frequency:30kHz) is added.

Note-4 : Output at TNLOS=0 is 0dB.

VDD=2.7 ~ 5.5V,Ta=-30 ~ 85 ℃

Attenuation values are 0dB.

Parameter		Conditions		min	typ	max	Unit	Remarks
Volume Gain Error	VR1	1020Hz Input	→SO	–	–	±0.3	dB	(Note-3)
	VR2		→RECOUT	–	–	±2	dB	
	VR3		→EXTOUT					
	VR4	TONE H 2KHz	→RING	–	–	±0.8	dB	(Note-1,2)
	VR5	2KHz	→SOUNDER	–	–	–	dB	(Note-4)
	VR6	1020Hz Input	→REOUT	–	–	±0.8	dB	(Note-3)
	VR7		→EXTOUT					
Head Set SW ON impedance		→MICGAIN2		–	–	1	KΩ	–
PLL set up time				–	–	40	msec	–
Frequency Response (A→D) EXTIN→SO		Relative to 1020Hz 0dBm0	0.06 KHz	24	–	–	d B	–
			0.2KHz	0	–	2.5		
			0.3~ 3.0KHz	-0.3	–	0.3		
			3.4KHz	-0.3	–	0.9		
			3.6KHz	0	–	–		
Frequency Response (D→A) SI→RECOUT		Relative to 1020Hz 0dBm0	0~3.0 KHz	-0.3	–	0.3	d B	–
			3.4KHz	-0.3	–	0.9		
			3.6KHz	0	–	–		

Note-1 : Measure in the condition that the loss from TAMPO to TAMPN is 0dB and the 3rd order butterworth L.P.F (cut-off frequency:30kHz) is added.

Note-2 : When TONE H frequency is 2KHz, output is 0dB.

Note-3 : Output at 1020Hz 0dBm0 input is 0dB.

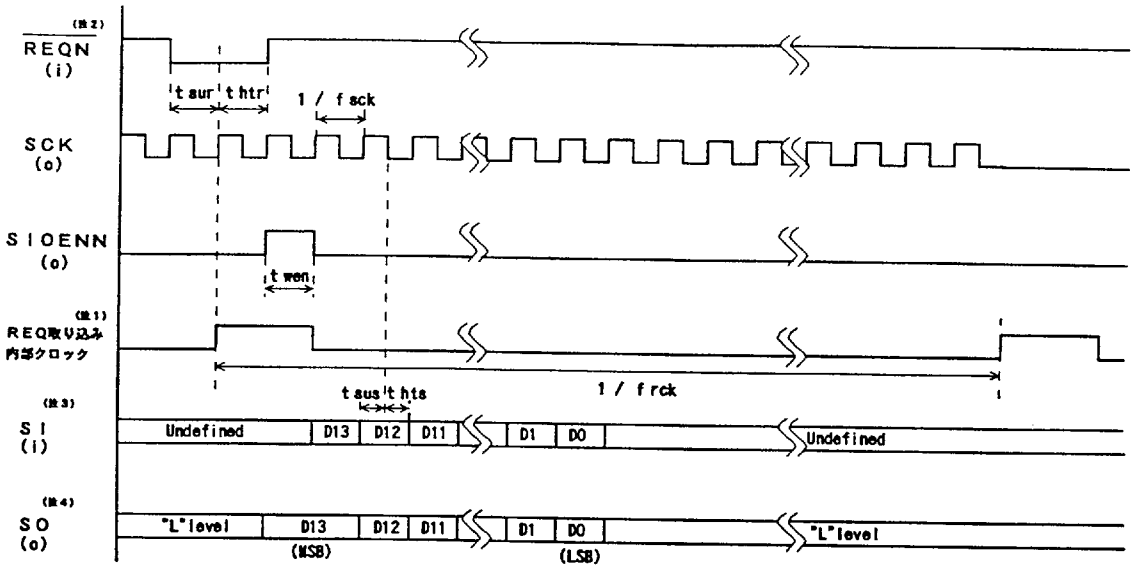
Note-4 : Guarantee only monotony. When VR5 is set to "0", the output is equal to the level of RAVDD.

■ Switching characteristics (Refer to Timing Diagrams)

Parameters	Symbol	min.	typ.	max.	Units
Serial Data Interface Timing					
SCK Frequency	f_{sck}		200		KHz
REQN Setup Time	t_{sur}	5.0	–	–	μs
REQN Holding Time	t_{htr}	5.0	–	–	μs
SI Setup Time	t_{sus}	100	–	–	ns
SI Holding Time	t_{hts}	100	–	–	ns
SIOENN Pulse Width	t_{wen}	5.0	–	–	μs
REQN reading internal clock frequency	f_{rck}		8		KHz
Control Register Interface Timing					
CLK Frequency	f_{clk}	–	–	3	MHz
DATA Setup Time	t_{suda}	100	–	–	ns
DATA Holding Time	t_{htda}	100	–	–	ns
STB Setup Time (CLK↑ to STB↑)	t_{sud}	333	–	–	ns
STB Holding Time (CLK↑ to STB↓)	t_{htd}	1000	–	–	ns
STB Pulse Width	t_{pwd}	667	–	–	ns
DAI Timing					
DCK Frequency	f_{dclk}		104		KHz
DCK Low Pulse Width	t_{wdcl}	3.8	4.8	5.8	μs
DCK High Pulse Width	t_{wdch}	3.8	4.8	5.8	μs
DRSTN Low Pulse Width	t_{wdr}	4	–	–	ms
DI Setup Time	t_{sudi}	100	–	–	ns
DI Holding Time	t_{htdi}	100	–	–	ns

(1) Serial Data Timing Diagram

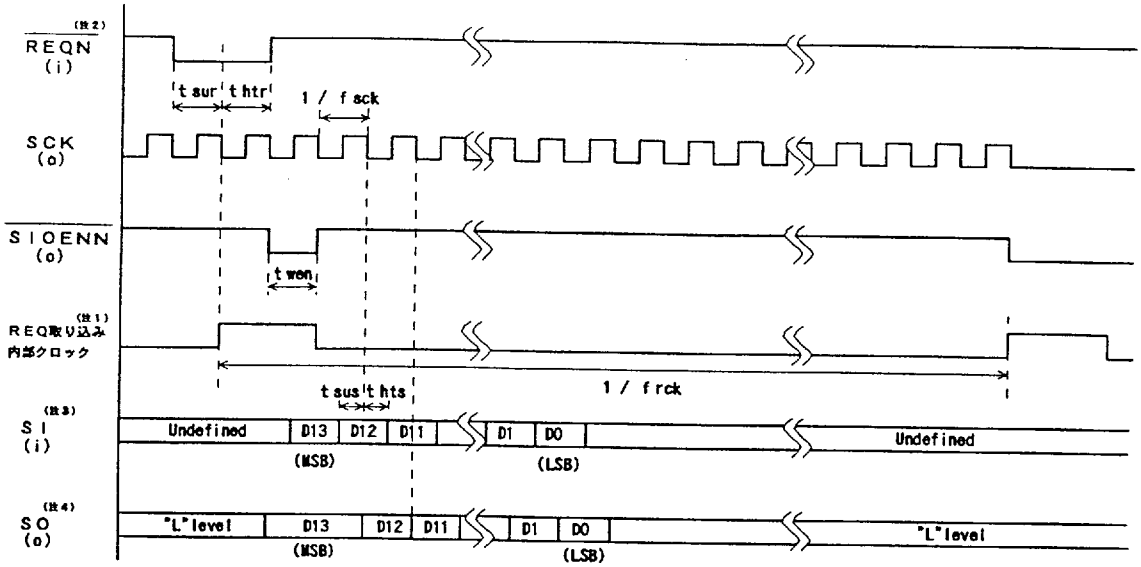
■ Mode 1
(for TI-TMS320C5x/Motorola-DSP56116/Analog Devices-ADSP2101 ／ NEC- μ PD77016)



Note-1) "REQN reading internal clock" is 8KHz internal clock that is used for reading REQN signal.
Note-2) REQN is latched at rising edge of REQN reading internal clock.
Note-3) SI is latched at falling edge of SCK.
MSB first or LSB first can be selected for the data input.
(If LSB first input is selected, the input data are as follows.
" 0 0 LSB ・・・・・・ MSB")
Note-4) SO changes at rising edge of SCK.
MSB first or LSB first can be selected for the data input.
(If LSB first output is selected, the input data are as follows.
" 0 0 LSB ・・・・・・ MSB")
Note-5) If REQN is equal to "H" at the rising edge of REQN reading internal clock,
SCK, SIOENN and SO are fixed to Low.

* REQN reading internal clock is 8KHz internal clock. If REQN is low at rising edge of REQN reading internal clock, serial data SI is latched and SO changes.

■ Mode 2 (for AT&T-DSP1616)



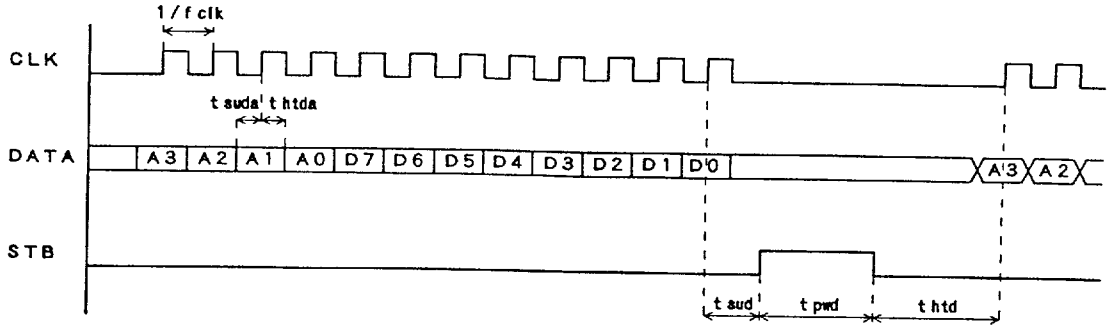
Note-1) "REQN reading internal clock" is 8KHz internal clock that is used for reading REQN signal.
Note-2) REQN is latched at rising edge of REQN reading internal clock.
Note-3) SI is latched at falling edge of SCK.
MSB first or LSB first can be selected for the data input.
(If LSB first input is selected, the input data are as follows.
" 0 0 LSB • • • • • • MSB")
Note-4) SO changes at rising edge of SCK.
MSB first or LSB first can be selected for the data input.
(If LSB first output is selected, the input data are as follows.
" 0 0 LSB • • • • • • MSB")
Note-5) If REQN is equal to "H" at the rising edge of REQN reading internal clock, SCK, SIOENN and SO are fixed to Low.

* REQN reading internal clock is 8KHz internal clock. If REQN is low at rising edge of REQN reading internal clock, serial data SI is latched and SO changes.

■ Mode 3 (for other DSPs)

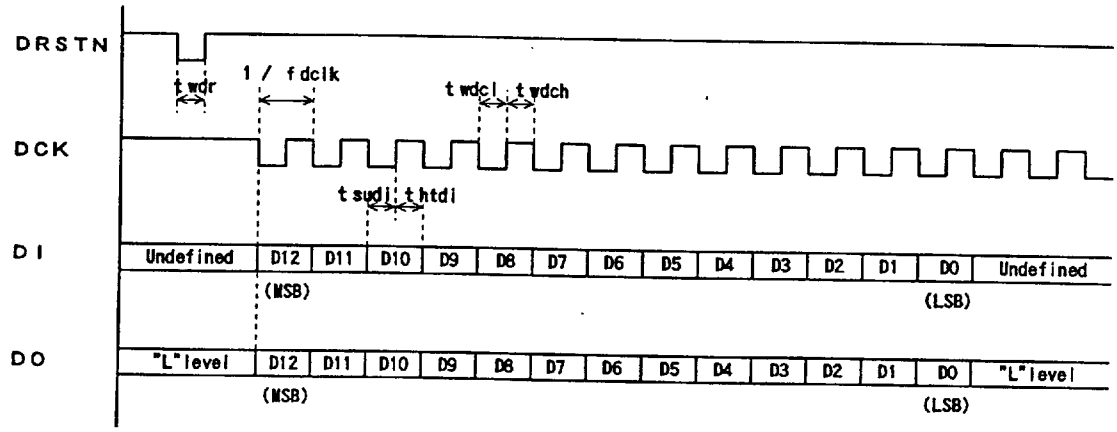
This mode is equal to the mode 2 except that SIOENN is inverted.

(2) Control Register Interface Timing Diagram



Note) DATA is latched at falling edge of CLK.

(3) DAI Timing Diagram



Note-1) DI is latched at rising edge of DCK.
Note-2) DO changes at falling edge of DCK.

Function of blocks

I. TX Section

The TX section includes microphone amplifier, VR1, AAF, TXBPF ,A/D converter and externalinput pin.

(1) Microphone amplifier

Differential amplifier. This amplifier can adjust gain of input signal from microphone with external resistors. The principal specifications are as follows.

Minimum load impedance	: 100 K Ω
Maximum load capacitance	: 5 pF
Maximum gain	: 40 dB
Maximum input amplitude	: 12.5 mVrms

There are two pins to adjust the gain (i.e. MICGAIN1 and MICGAIN2). When head-set is used,the gain can be adjusted by using MICGAIN2, and when hand-set is used, the gain can be adjusted by using MICGAIN1. Mute switch for MICGAIN2 is controlled by control register "HJ". Control method of the HJ register is referred to "Control Register".

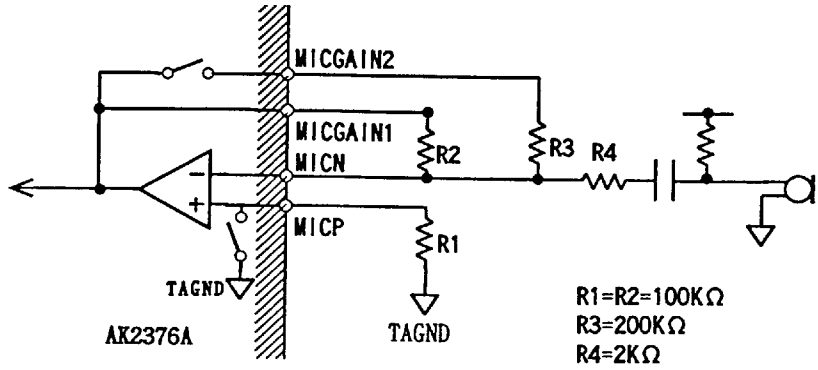


Fig.1: External circuit of microphone amplifier block

(2)VR1

TX attenuator. The attenuation value can be adjusted from 0 to -6 dB by 0.4dB/step. The attenuation value can is set to the control registers.

(3)AAF

Anti-aliasing filter.

(4)TXBPF

TX band-pass filter, compliant with CCITT rec.G.714.

(5)A/D converter

14bit linear A/D converter. Sampling rate is 8KHz. Data format is 2's compliment and MSB first or LSB first can be selected.

(6) External input pin

This pin is connected to external connector of mobile station. Processing methods of input signal can be selected by control registers.

The RX section includes D/A converter, RXLPF, VR2, VR3, VR6, VR7 receiver amplifier and external output pin.

(1)D/A converter
14bit linear D/A converter. Sampling rate is 8KHz. Data format is 2's compliment and MSB first or LSB first can be selected.

(2)RXLPF
RX low-pass filter, compliant with CCITT rec.G.714.

(3)VR2、VR3
RX attenuators. VR2 attenuates receiver output (RECOUT output), and VR3 attenuates external output (EXTOUT output). The attenuation value of each attenuators can be adjustedfrom 0 to −28 dB by 4dB/step. The attenuation values are set to the control registers.

(4)Receiver amplifier
Receiver amplifier includes gain adjustment and differential output buffer. Differential output (RECP and RECP) are connected to ceramic receiver. If filter is needed, form active filter with gain adjustment amplifire to cut noise off.

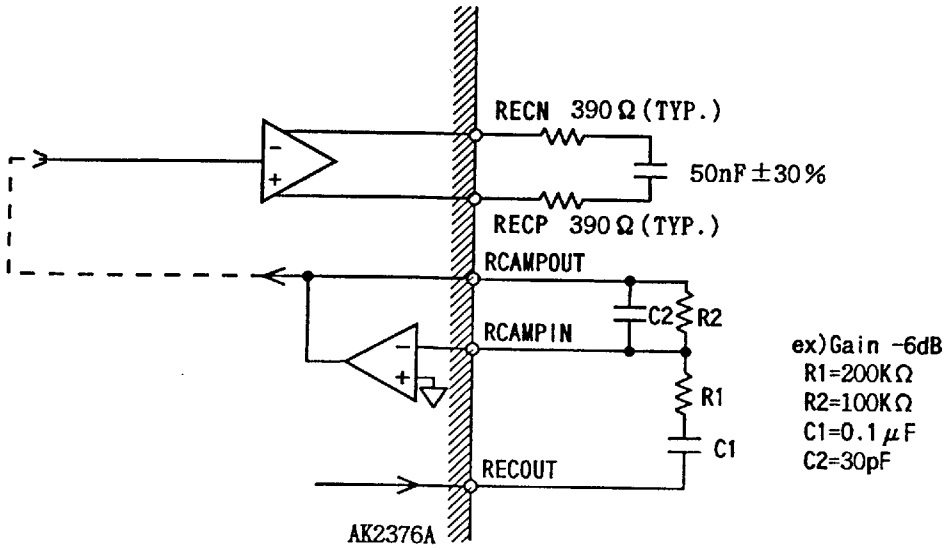


Fig.3: External circuit of receiver amplifier block

(5) external output pin
This pin is connected to external connector of mobile station. Output signal can be selected by control registers.

(6) VR6, VR7
RX attenuators. VR6 attenuates receiver output (RECOUT output), and VR7 attenuates external output (EXTOUT output). The attenuation value of each attenuators can be adjustedfrom 0 to +3 dB by 1dB/step. The attenuation values are set to the control registers.

Ⅲ. Tone generator section

The tone generator section includes TONE GEN., Tone amplifier, VR4 and VR5.

(1)TONE GEN.

Triple tone (including DTMF tones) generator. Tone whose frequency are set to programmable counters is generated. Tones generated by this block are as follows.

① TONE H(High Tone) ··· The high frequency tone of DTMF.
② TONE L(Low Tone) ··· The low frequency tone of DTMF.
③ TONE E(Ext Tone) ··· The tone for ringer tone.

Start and stop of each tones can be controlled independently.
Output level of tones are selected as follows.

① a normal level tone.
② a mute level. (−18dB)

For ringer tone, TONE E can be selected as follows.

① a continuous tone.
② a intermittent tone. (Intermitting frequency is 16Hz.)

For SOUNDER output, the rectangle signal whose frequency equals to TONE E frequency can be output.
In this case, if TONE E are selected to intermittent tone, SOUNDER output is intermitted at 16Hz.
Furthermore, in this case, 16Hz clock that is synchronized to intermitted frequency can be output.(SD16 pin)

[1] Output Frequency

Output frequency of the TONE H, TONE L and TONE E can be set independently. To set frequency, set data X that is found by the equation as follows to control registers.

$$\text{Data } X = \frac{162500/3}{\text{Output frequency } F(\text{Hz})} - 1$$

[2] DTMF Tone

Frequencies of TONE H and TONE L for standard DTMF frequencies are as follows.

	Standard Frequency	TONE H / TONE L Frequency	Error
Low Tones	697Hz	694.6Hz	−0.34%
	770Hz	773.8Hz	+0.49%
	852Hz	859.8Hz	+0.92%
	941Hz	950.3Hz	+0.99%
High Tones	1209Hz	1203.8Hz	−0.43%
	1336Hz	1321.0Hz	−1.12%
	1477Hz	1464.0Hz	−0.88%
	1633Hz	1641.5Hz	+0.52%

(2) Tone amplifier.

Amplifier for tone signal gain adjustment. This amplifier can be used as a noninverting amplifier by connecting external resistors. When this amplifier isn't used, connect TAMPN to TAMPO.

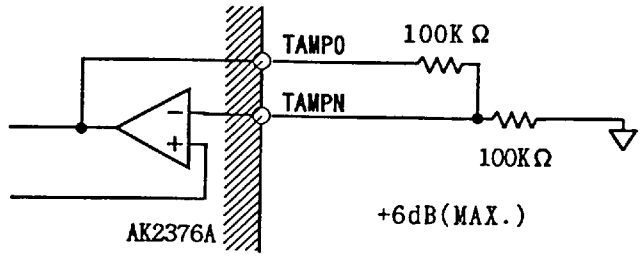


Fig.4: External circuit of tone amplifier block

(3)VR4

Tone signal attenuator. VR4 attenuates tone amplifier output. The attenuation value of VR4 can be adjusted from 0 to −31 dB by 1dB/step. The attenuation value is set to the control registers.

(4)VR5

SOUNDER signal attenuator. VR5 attenuates SOUNDER output. The attenuation value of VR5 can be adjusted from 0 to −7 dB by 1dB/step. The attenuation value is set to the control registers.

The TX section includes microphone amplifier, serial I/F, CLOCK GEN., VREF and CONTROL.

(1)Serial I/F

Serial data interface for A/D and D/A data. The data format is 2's compliment and MSB first or LSB first can be selected.
The triple serial I/F modes are prepared for connected DSPs.

mode	Connected DSPs
1	TMS320C5x(TI), DSP56116(Motorola), ADSP2101(Analog Devices), μPD77017(NEC)
2	DSP1616(AT&T)
3	other DSPs

(2)DAI

Digital audio interface for test mode which is compliant with GSM rec.11.10.

(3)CLOCK GEN.

Internal clocks generator. Internal clocks (2.6MHz main clock etc.) are generated from 8KHz reference clock by a internal PLL circuit. 8Khz clock is not needed as a 50% duty clock.
0.1 μ F capacitor is connected to LPF pin for a loop filter of PLL circuit.

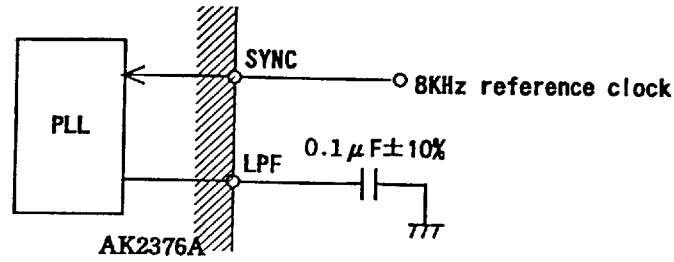


Fig.5: The external circuits of CLOCK GEN.

(4)VREF

Analog reference voltage circuit. Reference voltage is 1/2VDD typicaly.
To stabilize analog ground, connect capacitors analog ground pins.

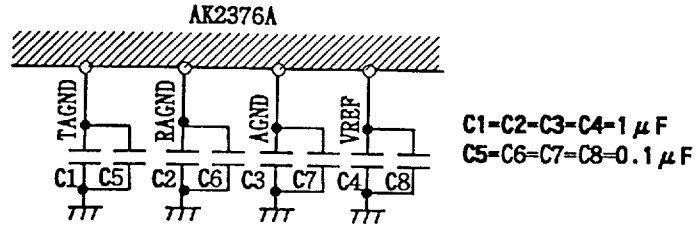


Fig.6: External circuit of VREF.

(5)CONTROL

Control registers for internal state setting. Data format and functions of the control registers are as follows.

[1] Register map

Address	Name	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
0	VR1+VR2	×	VR2 VAL			VR1 VAL			
1	VR3+VR4	VR3 VAL			VR4 VAL				
2	TONE H	TH FREQ							
3	TONE L	TL FREQ							
4	TONE E	TE FREQ							
5	PATH CNTRL	LPON	HJ	MCMT	VCMT	TNMT	EXMT	RCMT	RGMT
6	COUNT CNTRL	×	C16ON	TNLOS	T16ON	SNDON	XTCON	LTCON	HTCON
7	MISC	RCON	TNON	VCON	VPON	INTTC	RTC2	RTC1	×
8	VR5	×	×	×	×	×	VR5 VAL		
9	DSP MODE	×	×	×	×	×	MLSEL	DSP2	DSP1
A	EXT I/O MODE	×	×	×	×	×	EOUT	EIN2	EIN1
B	VR6+VR7	×	×	×	×	VR7 VAL		VR6 VAL	

Note) Address is shown in hexadecimal.
"X" is reserved. Always set zero.

[2] Control data format

Address				Data							
A 3	A 2	A 1	A 0	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0

[3] Function of control registers

(1)VR1+VR2 [R0]

This register sets attenuation values of TX attenuator VR1 and RX attenuator VR2.

1. TX attenuator VR1 attenuation value (D0 ~ D3)
   The attenuation value can be adjusted from 0 to -6 dB by 0.4dB/step.
   Initial value is -3.2dB.

2. RX attenuator VR2 attenuation value (D4 ~ D6)
   The attenuation value can be adjusted from 0 to -28 dB by 4dB/step.
   Initial value is -8dB.

Data format and initial value of VR1+VR2 register:

Bit	7	6	5	4	3	2	1	0
Field	-	VR22	VR21	VR20	VR13	VR12	VR11	VR10
Initial value	-	0	1	0	1	0	0	0

VR1 attenuation value:

VR13	VR12	VR11	VR10	dB
0	0	0	0	0.0
0	0	0	1	-0.4
0	0	1	0	-0.8
0	0	1	1	-1.2
0	1	0	0	-1.6
0	1	0	1	-2.0
0	1	1	0	-2.4
0	1	1	1	-2.8
1	0	0	0	-3.2
1	0	0	1	-3.6
1	0	1	0	-4.0
1	0	1	1	-4.4
1	1	0	0	-4.8
1	1	0	1	-5.2
1	1	1	0	-5.6
1	1	1	1	-6.0

VR2 attenuation value:

VR22	VR21	VR20	dB
0	0	0	0.0
0	0	1	-4.0
0	1	0	-8.0
0	1	1	-12.0
1	0	0	-16.0
1	0	1	-20.0
1	1	0	-24.0
1	1	1	-28.0

(2)VR3+VR4 [R1]

This register sets attenuation values of tone attenuator VR4 and RX attenuator VR3.

1. Tone attenuator VR4 attenuation value (D0 ~ D4)
   The attenuation value can be adjusted from 0 to -31 dB by 1dB/step.
   Initial value is -24dB.

2. RX attenuator VR3 attenuation value (D5 ~ D7)
   The attenuation value can be adjusted from 0 to -28 dB by 4dB/step.
   Initial value is -8dB.

Data format and initial value of VR1+VR2 register:

Bits	7	6	5	4	3	2	1	0
Field	VR32	VR31	VR30	VR44	VR43	VR42	VR41	VR40
Initial value	0	1	0	1	1	0	0	0

VR4 attenuation value:

VR44	VR43	VR42	VR41	VR40	d B
0	0	0	0	0	0
0	0	0	0	1	-1
0	0	0	1	0	-2
0	0	0	1	1	-3
0	0	1	0	0	-4
0	0	1	0	1	-5
0	0	1	1	0	-6
0	0	1	1	1	-7
0	1	0	0	0	-8
0	1	0	0	1	-9
0	1	0	1	0	-10
0	1	0	1	1	-11
0	1	1	0	0	-12
0	1	1	0	1	-13
0	1	1	1	0	-14
0	1	1	1	1	-15

VR44	VR43	VR42	VR41	VR40	d B
1	0	0	0	0	-16
1	0	0	0	1	-17
1	0	0	1	0	-18
1	0	0	1	1	-19
1	0	1	0	0	-20
1	0	1	0	1	-21
1	0	1	1	0	-22
1	0	1	1	1	-23
1	1	0	0	0	-24
1	1	0	0	1	-25
1	1	0	1	0	-26
1	1	0	1	1	-27
1	1	1	0	0	-28
1	1	1	0	1	-29
1	1	1	1	0	-30
1	1	1	1	1	-31

VR3 attenuation value:

VR32	VR31	VR30	d B
0	0	0	0
0	0	1	− 4
0	1	0	− 8
0	1	1	− 1 2
1	0	0	− 1 6
1	0	1	− 2 0
1	1	0	− 2 4
1	1	1	− 2 8

(3)TONE H、TONE L、TONE E [R2 ~ R4]

These registers set frequencies of triple tone(TONE H, TONE L and TONE E).
The data X is specified by binary format.
The equation that specifies data is as follows

Data X = (162500/3) / Output frequency F(Hz) - 1

D7 bit is MSB of data X in binary format.

The data for the standard frequency of DTMF tones are as follows.

	Standard Frequency	Output Frequency	Data
Low Tones	697Hz	694.6Hz	4D
	770Hz	773.8Hz	45
	852Hz	859.8Hz	3E
	941Hz	950.3Hz	38
High Tones	1209Hz	1203.8Hz	2C
	1336Hz	1321.0Hz	28
	1477Hz	1464.0Hz	24
	1633Hz	1641.5Hz	20

Note : Data are shown in hexadecimal.

Data format and initial values of TONE H registers:

Bit	7	6	5	4	3	2	1	0
Field	TH7	TH6	TH5	TH4	TH3	TH2	TH1	TH0
Initial value	0	0	1	0	0	0	0	0

(Initial data is 1633Hz)

Data format and initial values of TONE L registers:

Bit	7	6	5	4	3	2	1	0
Field	TL7	TL6	TL5	TL4	TL3	TL2	TL1	TL0
Initial value	0	0	1	1	1	0	0	0

(Initial data is 941Hz)

Data format and initial values of TONE E registers:

Bit	7	6	5	4	3	2	1	0
Field	TE7	TE6	TE5	TE4	TE3	TE2	TE1	TE0
Initial value	0	1	1	1	1	1	1	0

(Initial data is 425Hz)

(4)Path CNTRL [R5]

This registers control A/D to D/A loopback mode, head-set mode and mute mode.

Data format and initial values of PATH CNTRL register:

Bit	7	6	5	4	3	2	1	0
Field	LPON	HJ	MCMT	VCMT	TNMT	EXMT	RCMT	RGMT
Initial value	0	0	1	1	1	1	1	1

The function of each field is as follows.

1. A/D to D/A loopback mode (D7)
   LPON 0 : Normal mode
   1 : Loopback mode

2. Head-set mode (D6)
   HJ 0 : Normal mode (Hand-set mode)
   1 : Head-set mode

3. MIC mute mode (D5)
   MCMT 0 : Normal operation mode
   1 : mute mode

4. VOICE mute mode (D4)
   VCMT 0 : Normal operation mode
   1 : mute mode

5. TONE mute mode (D3)
   TNMT 0 : Normal operation mode
   1 : mute mode

6. EXTOUT pin mute mode (D2)
   EXMT 0 : Normal operation mode
   1 : mute mode

7. Receiver mute mode (D1)
   RCMT 0 : Normal operation mode
   1 : mute mode

8. RINGER mute mode (D0)
   RGMT 0 : Normal operation mode
   1 : mute mode

Note : The muting position is shown on "Detailed Block Diagram"(page 2).

(5)COUNT CNTRL [R6]

This registers control start and stop of counters and output tone mode.

Data format and initial values of COUNT CNTRL register:

Bit	7	6	5	4	3	2	1	0
Field	–	C16ON	TNLOS	T16ON	SNDON	XTCON	LTCON	HTCON
Initial value	–	0	0	0	0	0	0	0

The function of each field is as follows.

1. 16Hz clock output (D6)
   C16ON 0 : 16Hz clock output stop
   1 : 16Hz clock output start

2. Tone output level (D5)
   TNLOS 0 : Normal tone level output
   1 : Tone mute (–18dB output)

3. 16Hz intermitted output (D4)
   T16ON 0 : 16Hz intermitted output STOP
   1 : 16Hz intermitted output START

4. SOUNDER tone output (D3)
   SNDON 0 : SOUNDER tone output STOP
   1 : SOUNDER tone output START
   ("SOUNDER tone" is rectangle signal from SOUNDER pin whose frequency is equal to TONE E)

5. External tone (TONE E) counter (D2)
   XTCON 0 : External tone (TONE E) counter STOP
   1 : External tone (TONE E) counter START

6. Low tone (TONE L) counter (D1)
   LTCON 0 : Low tone (TONE L) counter STOP
   1 : Low tone (TONE L) counter START

7. High tone (TONE H) counter (D0)
   HTCON 0 : High tone (TONE H) counter STOP
   1 : High tone (TONE H) counter START

(6) MISC [R7]

This registers control power down mode and test mode.

Data format and initial values of MISC register:

Bit	7	6	5	4	3	2	1	0
Field	RCON	TNON	VCON	VPON	INTTC	RTC2	RTC1	–
Initial value	0	0	0	1	0	0	0	–

The function of each field is as follows.

1. Receiver AMP power down mode (D7)
   RCON 0 : Power down
   1 : Power on

2. TONE section power down mode (D6)
   TNON 0 : Power down
   1 : Power on

3. VOICE section power down mode (D5)
   VCON 0 : Power down
   1 : Power on

4. Vref and PLL section power down mode (D4)
   VPON 0 : Power down
   1 : Power on

5. Test mode control method selection (D3)
   INTTC 0 : By external control pins TC1 and TC2
   1 : By internal control registers RTC1 and RTC2

6. Test mode control (D2 ~ D1)

RTC2	RTC1	Test mode
0	0	Normal Operation
0	1	Speech encoder test mode
1	0	Speech decoder test mode
1	1	Acoustic device test mode

(7) VR5 [R8]

This register sets attenuation values of sounder output attenuator VR5.

Data format and initial values of VR5 register:

Bit	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	VR52	VR51	VR50
Initial value	–	–	–	–	–	0	0	0

SOUNDER output attenuator VR5 attenuation value (D0 ~ D2)

Attenuation values are as follows.

VR5 attenuation value:

VR52	VR51	VR50	d B
0	0	0	0
0	0	1	− 1
0	1	0	− 2
0	1	1	− 3
1	0	0	− 4
1	0	1	− 5
1	1	0	− 6
1	1	1	− 7

Note) Guarantee only monotony. When VR5 is set to "0", the output is equal to the level of RAVDD.

(8) DSP MODE [R9]

This registers control serial data I/F mode.

Data format and initial values of DSP MODE register:

Bit	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	MLSEL	DSP2	DSP1
Initial value	–	–	–	–	–	0	0	0

The function of each field is as follows.

1. MSB/LSB first select (D2)

These bits decide the turn of the SI/SO data for the serial I/F.

MLSEL	MSB/LSB first
0	MSB first (Both SI and SO)
1	LSB first (Both SI and SO) (0 0 LSB・・・・・・MSB)

2. DSP mode select (D0 ~ D1)

DSP2	DSP1	mode	DSPs
0	0	1	TMS320C5x, DSP56116, ADSP2101, μPD77017
0	1	2	DSP1616
1	0	3	other DSPs (This mode is equal to the mode 2 except that SIOENN is inverted.)
1	1		

(9) EXT I/O MODE [RA]

This registers control external input/output pin mode.

Data format and initial values of EXT I/O MODE register:

Bit	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	EOUT	EIN2	EIN1
Initial value	–	–	–	–	–	1	0	1

The function of each field is as follows.

1. External input mode (D0 ~ D1)

Select signal that is input from external input pin (EXTIN pin).

EIN2	EIN1	Input signal	Processing method
0	0	Speech signal	process by AK2376A
0	1	Data signal	output to external circuit (output of EXTDATAOUT pin)
1	0	Nothing	short to analog ground *1
1	1	Nothing	High - Z

*1: Warning! If this mode is selected when this IC is connected with the external circuit, the too-much current flows in this IC and it may cause the latch-up. Be separate from the external circuit when this mode is selected.

2. External output mode (D2)

Select signal that is output to external output pin (EXTOUT pin).

EOUT 0 : Speech signal output (output RX speech signal)
1 : Data signal output (output RX data signal from EXTDATAIN pin)

(10)VR6+VR7 [RB]

This register sets attenuation values of Tone attenuator VR7 and RX attenuator VR6.

1. Tone attenuator VR7 attenuation value (D2, D3)
   The attenuation value can be adjusted from 0 to +3 dB by 1dB/step.
   Initial value is 2dB.

2. RX attenuator VR6 attenuation value (D0, D1)
   The attenuation value can be adjusted from 0 to +3 dB by 1dB/step.
   Initial value is 2dB.

Data format and initial value of VR6+VR7 register:

Bit	7	6	5	4	3	2	1	0
Field	–	–	–	–	VR71	VR70	VR61	VR60
Initial value	–	–	–	–	1	0	1	0

VR6 attenuation value:

VR11	VR10	d B
0	0	0
0	1	+ 1
1	0	+ 2
1	1	+ 3

VR7 attenuation value:

VR21	VR20	d B
0	0	0
0	1	+ 1
1	0	+ 2
1	1	+ 3

V. Power Supply

Pins for analog power supply and digital power supply are different. When different powersources are supplied to each pins, DVDD may not exceed AVDD.
Capacitors are connected between each power supply pin and each ground pin, to reduce an influence of noise from power source.

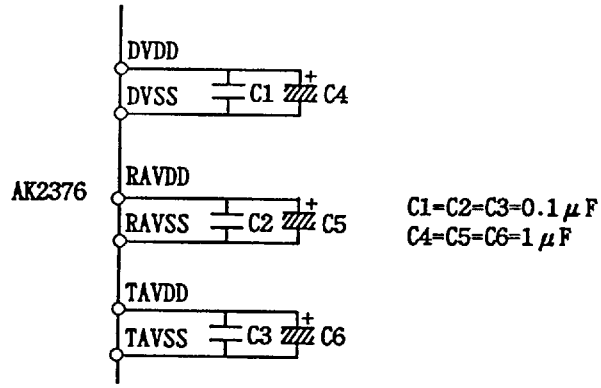


Fig.7: External circuit of power supply

Power Down Mode

The four power down modes are prepared as the standard power down mode, and each power down sections are selected independently to power down.

	Power down mode	Register Setting			
		RCON	TNON	VCON	VPON
1	VOICE section power down	1	1	0	1
2	VOICE and TONE sections power down	1	0	0	1
3	VOICE, TONE and RECEIVER AMP sections power down	0	0	0	1
4	Full power down	0	0	0	0

Note : Serial I/F, DAI, control registers, and programmable counters are not in power down, when full power down mode.

Test Mode

AK2376 have the test mode by DAI that compliant with GSM rec.11.10 and loopback mode.
The test mode can be selected by LPON and RTC1/RTC2(internal registers) or TC1/TC2 (external input pins). INTTC register changes control method (RTC1/RTC2 or TC1/TC2).

LPON	INTTC	TC2	TC1	RTC2	RTC1	Test mode	Signal Path	Timing Chart
0	0	0	0	–	–	Normal operation mode	Fig. 8	Fig. 13
0	0	0	1	–	–	Speech encoder test mode	Fig. 9	Fig. 14
0	0	1	0	–	–	Speech decoder test mode	Fig. 10	Fig. 15
0	0	1	1	–	–	Acoustic device test mode	Fig. 11	Fig. 16
0	1	–	–	0	0	Normal operation mode	Fig. 8	Fig. 13
0	1	–	–	0	1	Speech encoder test mode	Fig. 9	Fig. 14
0	1	–	–	1	0	Speech decoder test mode	Fig. 10	Fig. 15
0	1	–	–	1	1	Acoustic device test mode	Fig. 11	Fig. 16
1	–	–	–	–	–	Loopback mode	Fig. 12	

Note) "–" is don't care.

■ The signal path of each test mode.

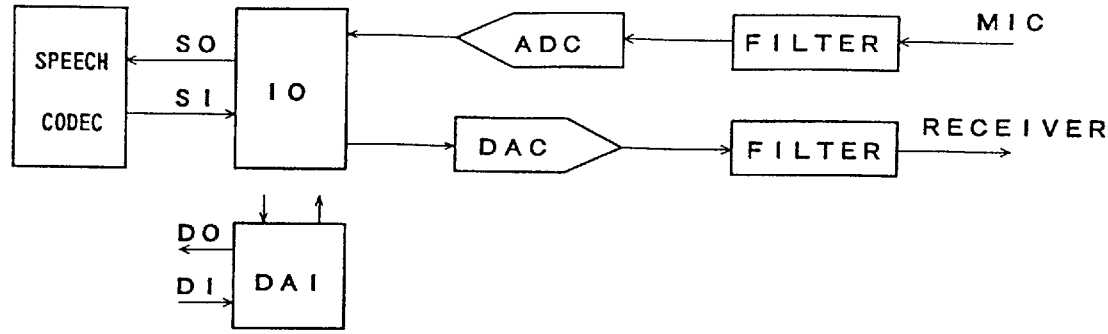


Fig.8: Normal operation mode

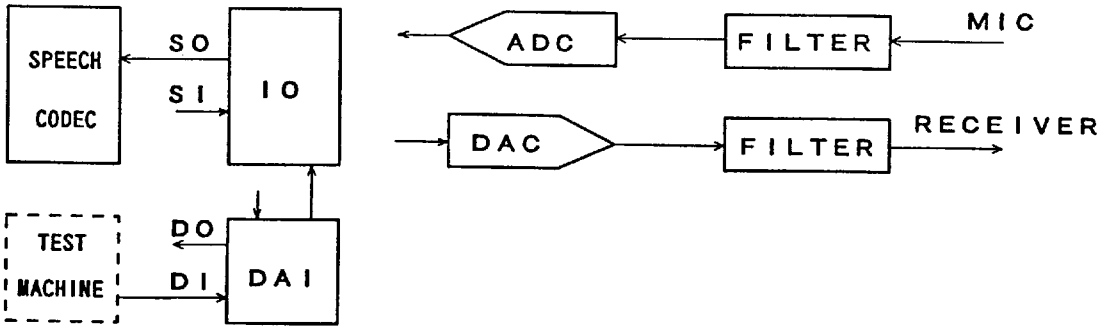


Fig.9: Speech encoder test mode

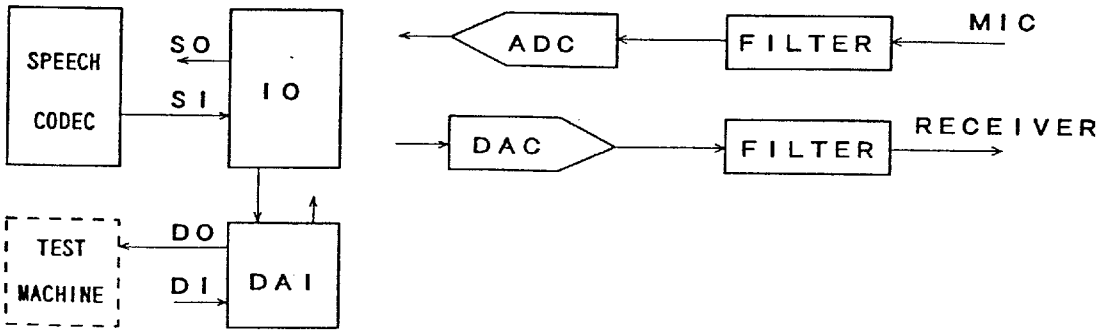


Fig.10: Speech decoder test mode

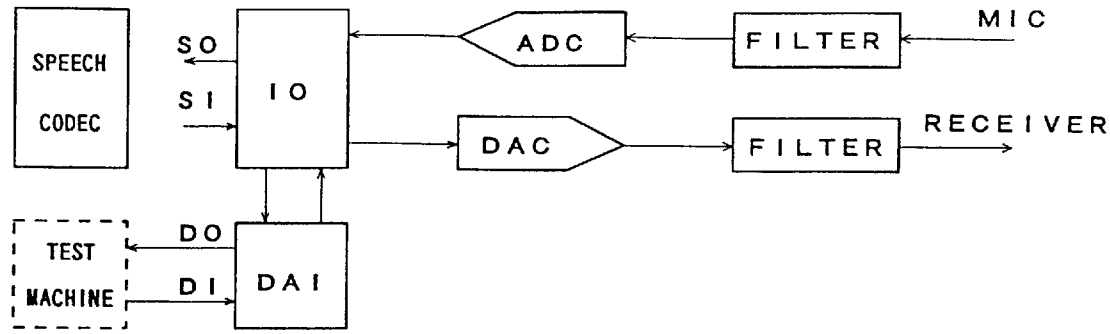


Fig.11: Acoustic device test mode

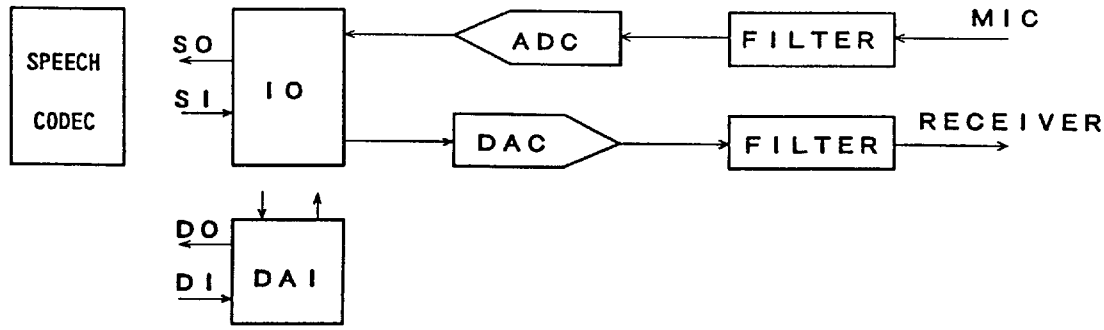


Fig.12: Loopback mode

■ The timing chart of each test mode. (for mode 2)

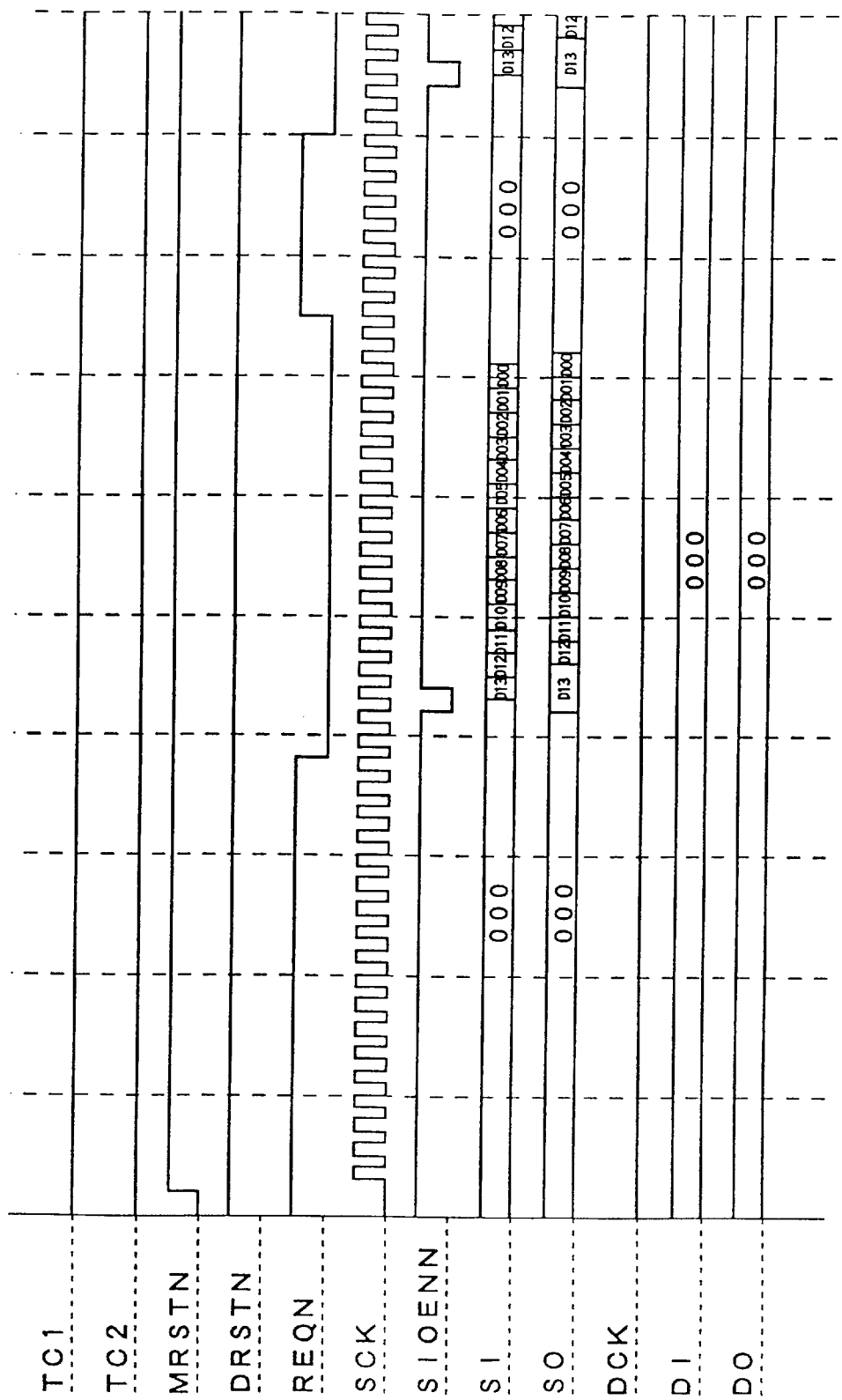


Fig.13: Normal operation mode (TC1=0, TC2=0)

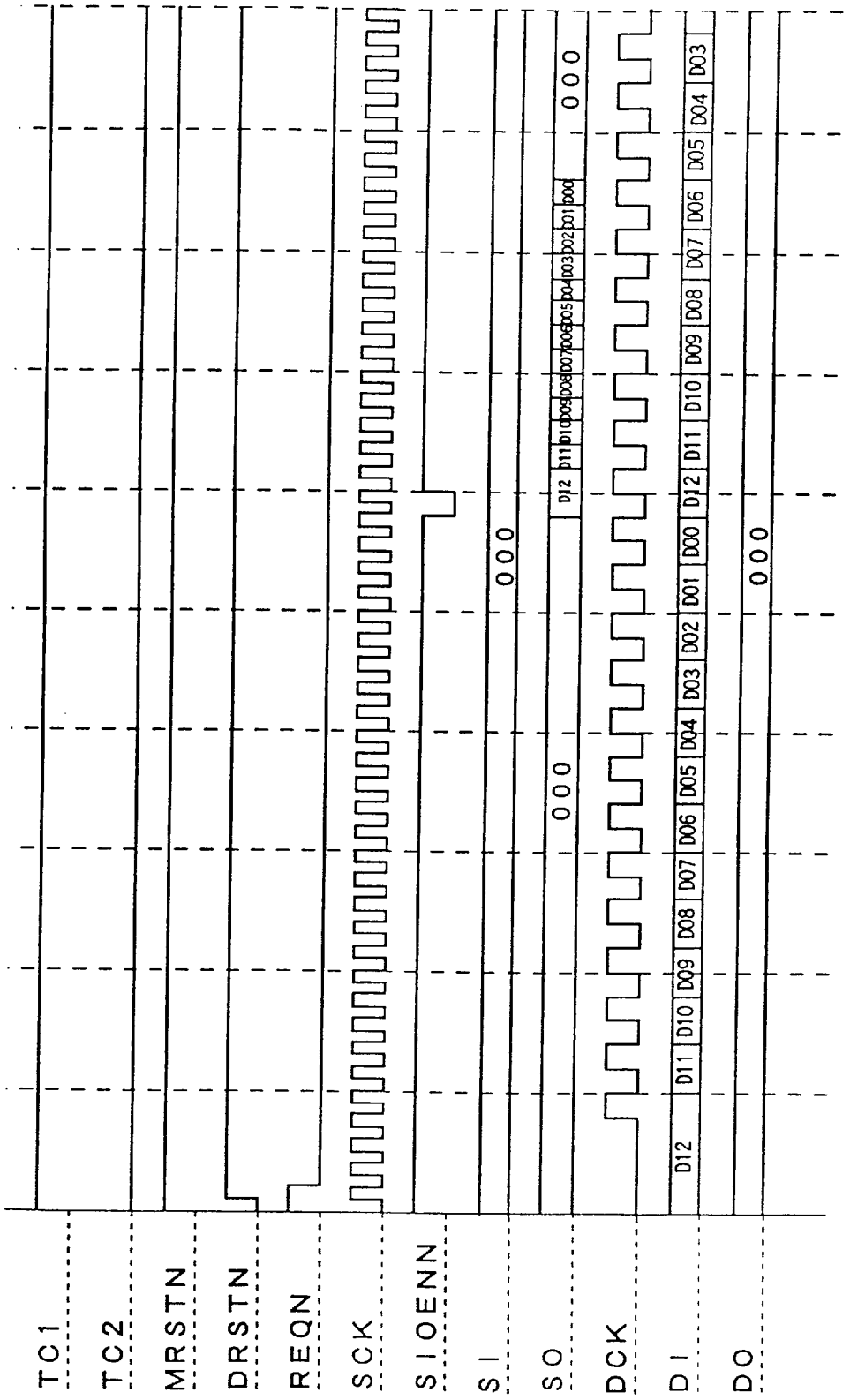


Fig.14: Speech encoder test mode (TC1=1, TC2=0)

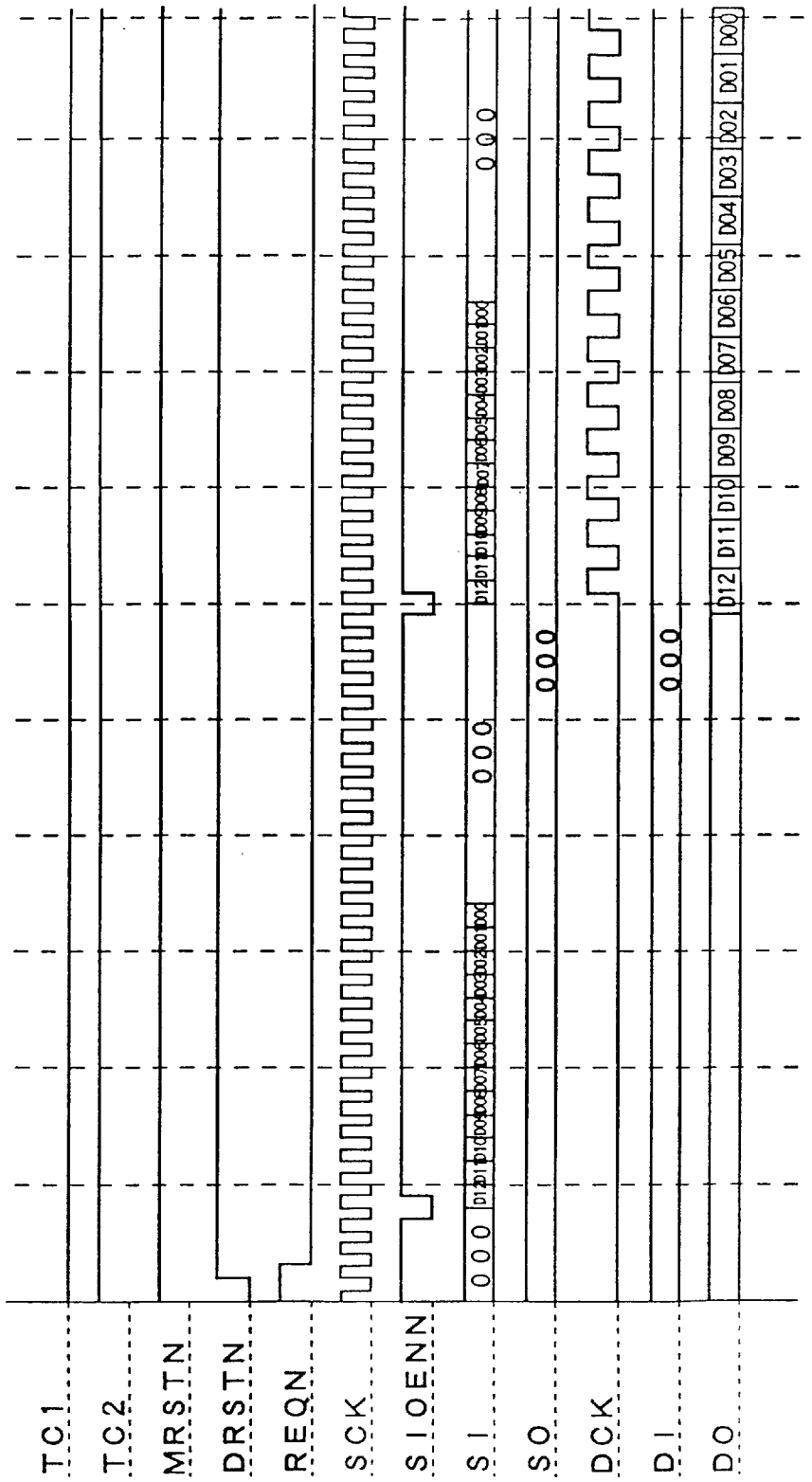


Fig.15: Speech decoder test mode (TC1=0, TC2=1)

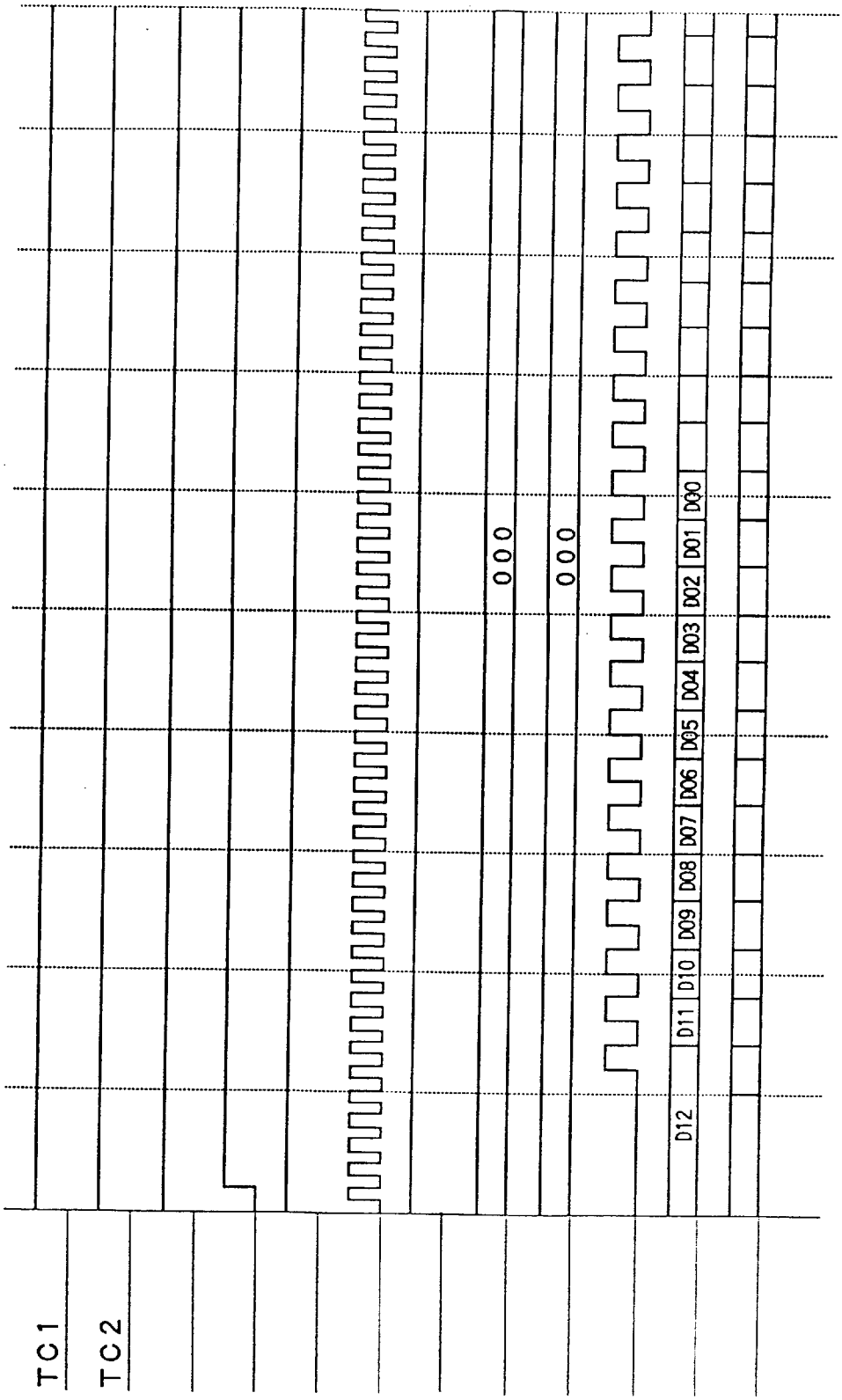


Fig.16: Acoustic device test mode (TC1=1, TC2=1)

Packaging Information

Marking

(1) Pin #1 indication (The chamfered corner indicates pin number 1.)
(2) Date Code: 5 Digits
(3) Marketing Code: AK2376A
(4) Country of Origin: JAPAN
(5) Asahi Kasei Logo

Outline Dimensions