AK4319

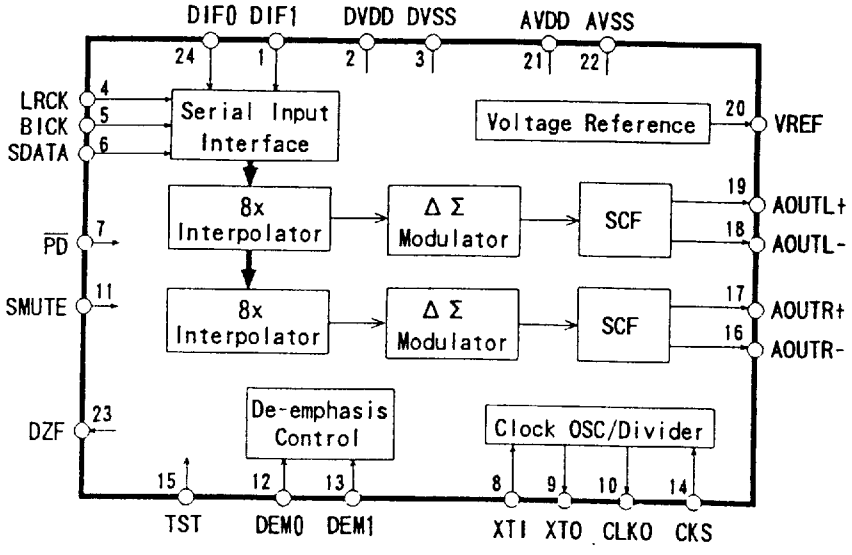
18BIT Δ Σ STEREO DAC

GENERAL DESCRIPTION

The AK4319 is a high performance 1bit stereo DAC for digital audio systems. A 1bit DAC can achieve monotonicity and low distortion with no adjustment. On chip SCF filter makes the device less affected to the clock jitter and also suppresses the undesirable radio emission noise. The device equips differentially configurated output pins, but either of the pins can be used as single-end. The AK4319 achieves lower Out-band noise characteristic (than AK4318) and it is suitable for BS/CS tuner and other digital audio applications.

FEATURES

- ☐ High Performance Stereo 1bit DAC
  - · On chip 8 × Interpolation Filter
  - · 4th Order Δ Σ DAC
  - · On chip Analog Post Filter(SCF)
  - · Differential outputs(Single-end use is available)
  - · 256/384fs Master Clock available
  - · Digital de-emphasis
    for 32, 44.1, 48kHz sampling
  - · Soft mute
  - · High Tolerance to Clock Jitterr
  - · Low Out-band Noise
- ☐ THD+N: -90dB
- ☐ DR: 96dB
- ☐ 24pin SSOP Package



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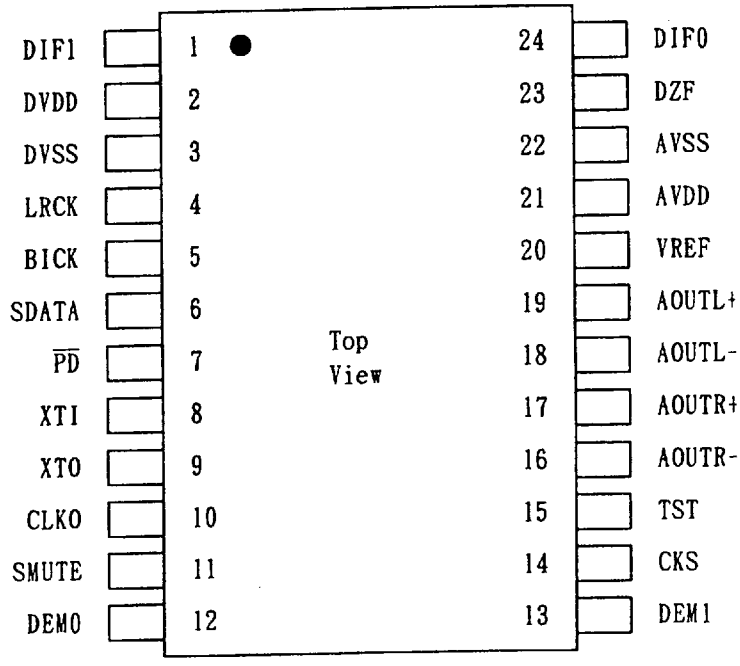
■ Ordering Guide

AK4319-VM	-10 ~ 70 ℃	24pin SSOP
AKD4319	Evaluation Board	

■ Pin Layout



PIN/FUNCTION

No.	Pin Name	I/O	Function
24 1	DIF0 DIF1	I	Digital Input Format Pins (Pull-down pin) These pins select one of four input modes.
2	DVDD	–	Digital Power Supply Pin, +5V
3	DVSS	–	Digital Ground Pin
4	LRCK	I	L/R Clock Pin This input determines which channel is being input.
5	BICK	I	Serial Data Clock Pin This clock is used to latch SDATA.
6	SDATA	I	Serial Data Input Pin 2's complement, MSB-first configuration.
7	$\overline{PD}$	I	Power-down Pin Bringing $\overline{PD}$ Pin Low puts the device into power-down mode Upon returning High, the device initiates internal reset. This input must be brought to Low once to reset after applying power to the device.
8	XTI	I	Master Clock Input Pin A crystal can be connected between this pin and XTO, or an external clock can be input on XTI directly. The frequency of 256fs or 384fs is selected by CKS Pin
9	XTO	O	Crystal Oscillator Output Pin When an external clock is input to XTI, this pin should be left open.
10	CLKO	O	Clock Output pin The inverted XTI clock is output.
11	SMUTE	I	Soft Mute Pin (Pull-down pin) "H" initiates the mute cycle and "L" releases it.
12 13	DEM0 DEM1	I	De-emphasis Mode Pins Major sampling rates(32k, 44.1k, 48k) are supported.
14	CKS	I	Master Clock Select Pin (Pull-down pin) "L": CLK=256fs, "H": CLK=384fs
15	TST	I	Test Pin (Pull-down pin)
			Left open or tied to GND.
16	AOUTR–	O	Rch analog negative output pin
17	AOUTR+	O	Rch analog positive output pin
18	AOUTL–	O	Lch analog negative output pin
19	AOUTL+	O	Lch analog positive output pin
20	VREF	O	Voltage Reference Output pin 2.95V (respects to GND) Must be connected to GND through a 0.1uF ceramic cap. along with a 10uF electrolytic capacitor.
21	AVDD	–	Analog Power Supply Pin, +5V
22	AVSS	–	Analog Ground Pin
23	DZF	O	Zero Input Detect Pin After 8192 LRCK cycles of sequential zero data are input on both L/R channels, this pin goes to "H".

ABSOLUTE MAXIMUM RATINGS

(AVSS,DVSS=0V; Note 1)

Parameter	Symbol	min	max	Units
Power Supplies: Analog	AVDD	-0.3	6.0	V
Digital	DVDD	-0.3	AVDD	V
Input Current, Any Pin Except Supplies	IIN	-	±10	mA
Input Voltage	VIND	-0.3	AVDD+0.3	V
Ambient Operating Temperature	Ta	-10	70	°C
Storage Temperature	Tstg	-65	150	°C

Note: 1. All voltages with respect to ground.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(AVSS,DVSS=0V; Note 1)

Parameter	Symbol	min	typ	max	Units
Power Supplies: Analog	AVDD	4.5	5.0	5.5	V
Digital	DVDD	4.5	5.0	AVDD	V

Notes:1. All voltages with respect to ground.

* Specifications are subject to change without notice.

* AKM assumes no responsibility for the usage beyond the conditions in this data sheet.

ANALOG CHARACTERISTICS

(Ta=25 °C ; AVDD,DVDD=5.0V; fs=48kHz; Signal Frequency=1kHz; 18bit Input Data; Differential Outputs; Measurement Bandwidth=10Hz ~ 20kHz; unless otherwise specified)

Parameter		min	typ	max	Units
Dynamic Characteristics					
THD+N (0dB Output)	(Note 2)		-90	-84	dB
Dynamic Range (-60dB Output)	(Note 3)	88	96		dB
S/N	(Note 4)	88	96		dB
Interchannel Isolation		90	100		dB
Interchannel Gain Mismatch			0.1	0.3	dB
DC Accuracy					
Gain Drift			100		ppm/°C
Output Voltage Range	(Note 5)	±2.55	±2.76	±2.97	V
Power Supplies					
Power Supply Current					
Normal Operation ($\overline{PD}$="H")	AVDD		12	18	mA
	DVDD		7	11	mA
Power-Down-Mode ($\overline{PD}$="L") (All input pins = "L")	AVDD+DVDD		10	50	uA
Power Dissipation (AVDD+DVDD)					
Normal Operation			95	145	mW
Power-Down-Mode			0.1		mW
Power Supply Rejection			40		dB

Notes:2. Inverse of S/(N+D).

3. A-weighted. (IEC publ.651)

4. A-weighted. Digital input all zeros.

5. Summation of the differential outputs, (AOUT+)-(AOUT-). $R_L \geqq 5k\ \Omega$

FILTER CHARACTERISTICS

(Ta=25 °C ; AVDD,DVDD=5.0V ± 10%; fs=48kHz; DEM0="1",DEM1="0")

Parameter		Symbol	min	typ	max	Units
Digital Filter						
Passband ±0.06dB	(Note 6)	PB	0		21.8	kHz
-6.0dB			0		24.0	kHz
Stopband	(Note 6)	SB	26.2			kHz
Passband Ripple		PR			±0.06	dB
Stopband Attenuation		SA	43			dB
Group Delay	(Note 7)	GD		14.7		1/fs
2nd Order SCF						
Frequency Response 20kHz				-0.04		dB
24kHz				-0.32		dB
48kHz				-6.0		dB

Note: 6.The passband and stopband frequencies scale with fs.
For example, PB=0.4535*fs(@-0.06dB), SB=0.546*fs.

7.The processing delay time which is consumed in digital filter. This time is measured from setting the 18bit data on the input register to the output of the corresponding analog signal.

DIGITAL CHARACTERISTICS

(Ta=25 ℃ ; AVDD,DVDD=5.0V ± 10%)

Parameter	Symbol	min	typ	max	Units
High-Level Input Voltage	V_{IH}	2.4	-	-	V
Low-Level Input Voltage	V_{IL}	-	-	0.6	V
XTI input Voltage when it is AC coupled(Note8)	V_{AC}	1			Vp-p
High-Level Output Voltage Iout=-100uA	V_{OH}	DVDD-0.5	-	-	V
Low-Level Output Voltage Iout=100uA (Note 9)	V_{OL}	-	-	0.5	V
Input Leakage Current (Note 10)	Iin	-	-	±10	uA

Note:8.When Not AC coupled, XTI input Voltage is CMOS level.(VIH:70%DVDD,VIL:30%DVDD)

9.Excludes XTO pin.

10.Excludes right listed pins. TST,ZMUTE,SMUTE,DIF0,DIF1,CKS pins are pulled-down internaly. (Typ. 90k Ω)

SWITCHING CHARACTERISTICS

(Ta=25 ℃ ; AVDD,DVDD=5.0V ± 10%; C_L = 20pF)

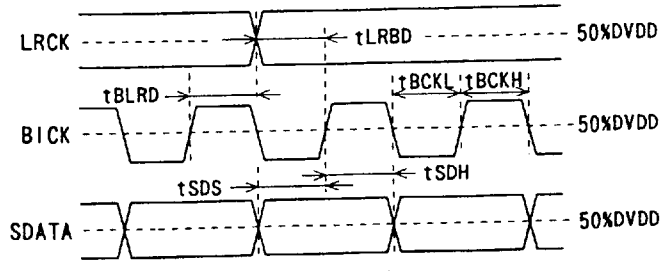
Parameter	Symbol	min	typ	max	Unit
Control Clock Frequency					
Crystal Resonator 256fs:	fCLK	7.10	12.288	13.9	MHz
384fs:	fCLK	10.70	18.432	20.7	MHz
External Clock 256fs:	fCLK	2.56	12.288	13.9	MHz
Pulse Width Low	tCLKL	28			ns
Pulse Width High	tCLKH	28			ns
384fs:	fCLK	3.84	18.432	20.7	MHz
Pulse Width Low	tCLKL	20			ns
Pulse Width High	tCLKH	20			ns
LRCK Frequency	fs	10	48	54	kHz
Serial Interface Timing (Note 11)					
BICK Period	tBCK	290			ns
BICK Pulse Width Low	tBCKL	100			ns
Pulse Width High	tBCKH	100			ns
BICK rising to LRCK edge (Note 12)	tBLRD	40			ns
LRCK Edge to BICK rising (Note 12)	tLRBD	40			ns
SDATA Hold Time	tSDH	40			ns
SDATA Setup Time	tSDS	40			ns
Reset Timing					
$\overline{PD}$ Pulse Width (Note 13)	tRST	100			ns

Notes:11. Refer to the operating overview section "Serial Data Interface".

12. Specified L/R edges not to coincide with the rising edges of BICK.

13. $\overline{PD}$ could be left "L" upon power up.

■ Timing Diagram



Data Input Timing

Reset Timing

OPERATION OVERVIEW

■ System Clock Input

The external clocks of XTI(256fs/384fs), LRCK(fs), BICK(32fs ~) are required to operate the AK4319. The master clock(XTI) should be synchronized with LRCK but there is no need to adjust their phases each other. The XTI is used in the digital interpolation filter and the delta-sigma modulator. The master clock could be generated connecting a crystal oscillator between XTI and XTO, or could be fed to XTI externally with XTO pin left open. XT Icould accept not only CMOS compatible clock but also DC isolated 1Vp-p sinusoidal wave. Internal clock is output via CLKO pin.

The frequency of XTI is determined by the sampling rate fs(LRCK) and the settingof the Clock Select, CKS pin. Setting CKS "L" selects an XTI frequency of 256fs while setting CKS "H" selects 384fs. When the 384fs is selected, the internal masterclock becomes 256fs(=384fs*2/3). Table 1. shows the XTI clock frequency which corresponds to typical audio sampling rate.

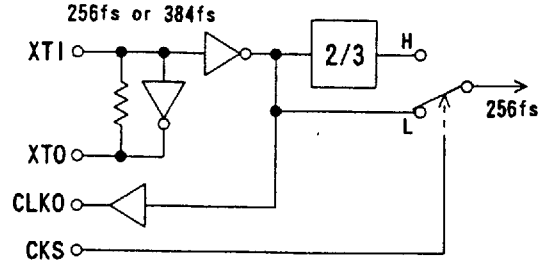


Figure 1. Internal Clock Circuit

LRCK (fs) (kHz)	CKS	XTI (MHz)
32.0	L	8.1920
	H	12.2880
44.1	L	11.2896
	H	16.9344
48.0	L	12.2880
	H	18.4320

Table 1. Example of System Clock

As the AK4319 equipses the phase error detection circuit, the AK4319 is reset by itself automatically when the synchronization between internal timing and external LRCK is missedin case of changing the clock frequencies.Therefore, the reset is not required except onlyupon power-up. Please refer to the "System Reset" section.

When the device is working ($\overline{PD}$="H") , master clock (CLK) should be presented on the device. The missing of the clock may cause to over currents in the dynamic logic in the device. The device should be put into power-down, before stopping the master clock(CLK).

■ Serial Data Interface

The AK4319 interfaces with external systemby using SDATA, BICK and LRCK pins. Four types of data format(Table 2.) are avail- able and one of them is selected by setting DIF0 and DIF1. Format 0 is compatible with existing 16-bit DACs and digital filters. Format1 is an 18-bit version of format0. Format2 is similar to AKM ADCs (AK5339/40/45/89/90) and many DSP serial ports. Format3 is compatible with the I 2 S serial data protocol. In formats 2 and 3, 16-bit data followed by two zeros also could be input. In all modes, the serial data is MSB-first and 2's complement format.

DIF1	DIF0	Mode	Fig
0	0	0: LSB Justified, 16bit	2
0	1	1: LSB Justified, 18bit	2
1	0	2: MSB Justified, 16-18bit	3
1	1	3: I²S Compatible	4

Table 2. Digital Input Formats

*Mode 0 or 3 should be selected for the 32fs BICK.

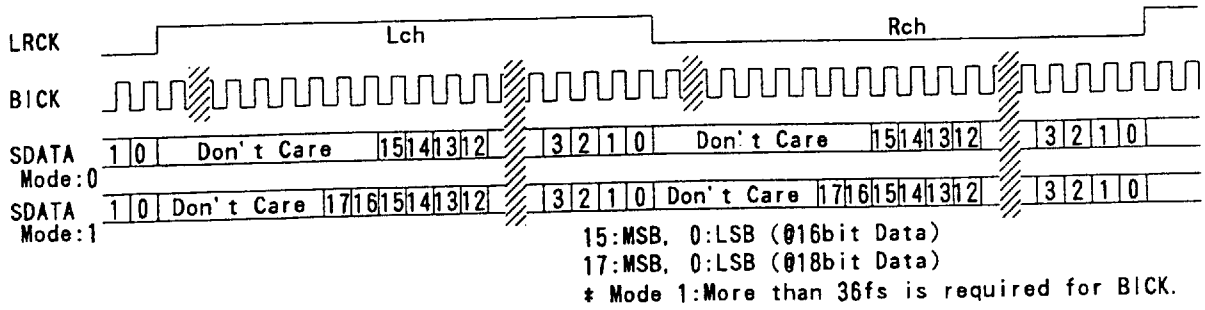


Figure 2. Digital Input Formats 0 & 1

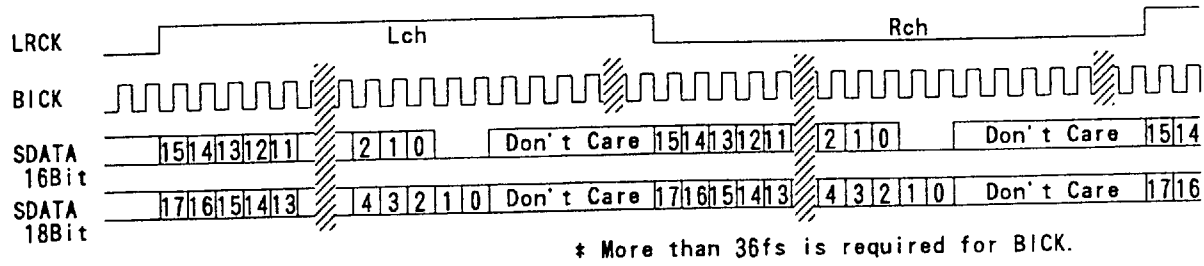


Figure 3. Digital Input Formats 2

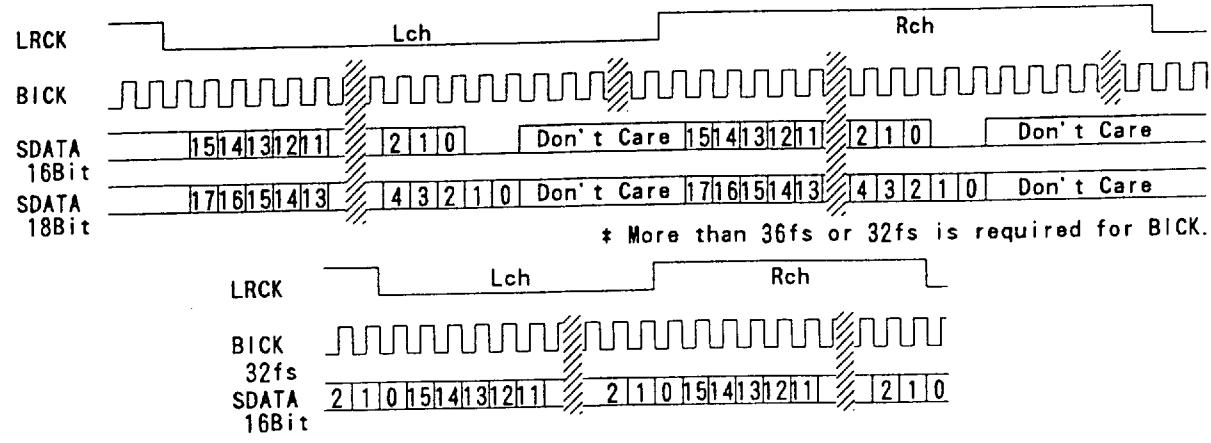


Figure 4. Digital Input Formats 3

■ De-emphasis filter

The AK4319 includes the digital de-emphasis filter (tc=50/15us) based on IIR. The filter is applied to three sampling frequencies (32kHz, 44.1kHz, 48kHz).

The de-emphasis filter selected by DEM0 and DEM1 is enabled for a corresponding input audiodata. The de-emphasis is disabled at DEM0="1" and DEM1="0".

DEM1	DEM0	Mode
0	0	44.1kHz
0	1	OFF
1	0	48kHz
1	1	32kHz

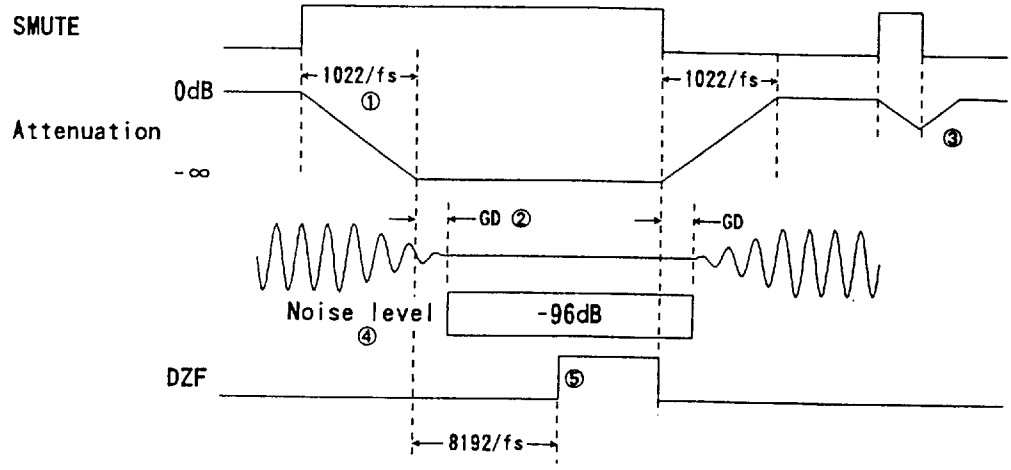
Table 1. De-emphasis filter control

■ Zero detection & Zero mute operation

After the input data at both channels are continuously zeros for 8192 LRCK cycles or when the muting period exceeds 8192+1022 LRCK cycles, DZF goes to "H". DZF goes "L" immediately after non zero data is input or soft mute is released.

■ Soft mute operation

When SMUTE goes "H", the output signal is attenuated into $-\infty$ during 1022 LRCK cycles. SMUTE is returned to "L", the mute condition is released and the output attenuation gradually changes to 0dB during 1022 LRCK cycles. If the soft mute is released within 1022LRCK cycles, the attenuation is recoverd to 0dB with same gradient and cycles.
The soft mute function is effective when changing the signal source without stopping the signal transmission.



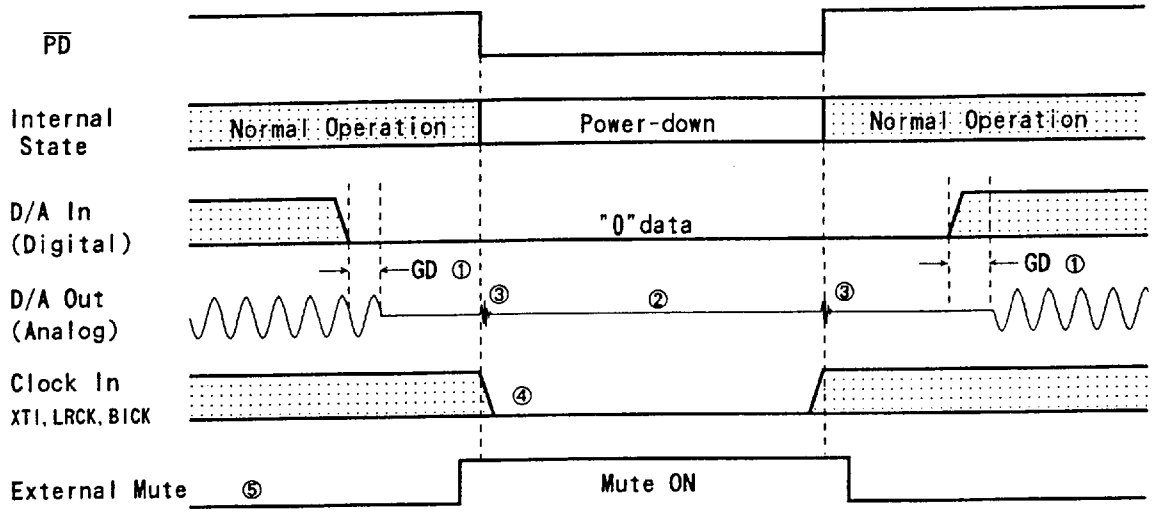
Notes:

① The output signal is attenuated into $-\infty$ during 1022 LRCK cycles(1022/fs).
② Analog output corresponding to digital input have the group delay(GD).
③ If the soft mute is released within 1022 LRCK cycles, the attenuation is recoverd to 0dB.
④ The noise energy of the 20kHz bandwidth on analog outputs is -96dB when muted.
⑤ When the input data at both channels are continuously zeros for 8192 LRCK cycles, DZF goes to "H". DZF goes "L" immediately after non-zero data is input.

Figure 5. Soft mute and zero detection

■ Power-Down

The AK4319 is put in the power-down mode by bringing $\overline{PD}$ pin "L" and the analog outputs are set to floating(Hi-Z) condition. Figure 6 shows an example of the system timing at thepower-down and power-up.



① Analog output has the group delay(GD).
② When power-down is initiated, analog outputs are set into Hi-Z. Outputs noise level is about -110dB.
③ Some -50dB of click noise occurs at the transition (" ↓ ↑ ") of PD pin.
④ When the master clock is stopped, the AK4319 should have been in the power-down mode.
⑤ If the click noise (③) is a problem, an external mute circuit which generates above timing (⑤) is needed. Please refer to Figure 7.

Figure 6. Power-down/up timing

■ System Reset

The AK4319 should be reset once by bringing $\overline{PD}$ "L" upon power-up. The internal timing starts clocking after the first " ↑ " of LRCK upon exiting reset.

■ External mute circuit

Some click noise may occur at the transition(" ↑ ↓ ") of $\overline{PD}$ signal. The click noise of $\overline{PD}$ signal can be avoided by controlling the external mute circuit using the signal like ⑤ in Figure 6. The S/N of -110dB could be achieved by muting the analog outputs using DZF signal. The external mute circuit example is shown in Figure 7.

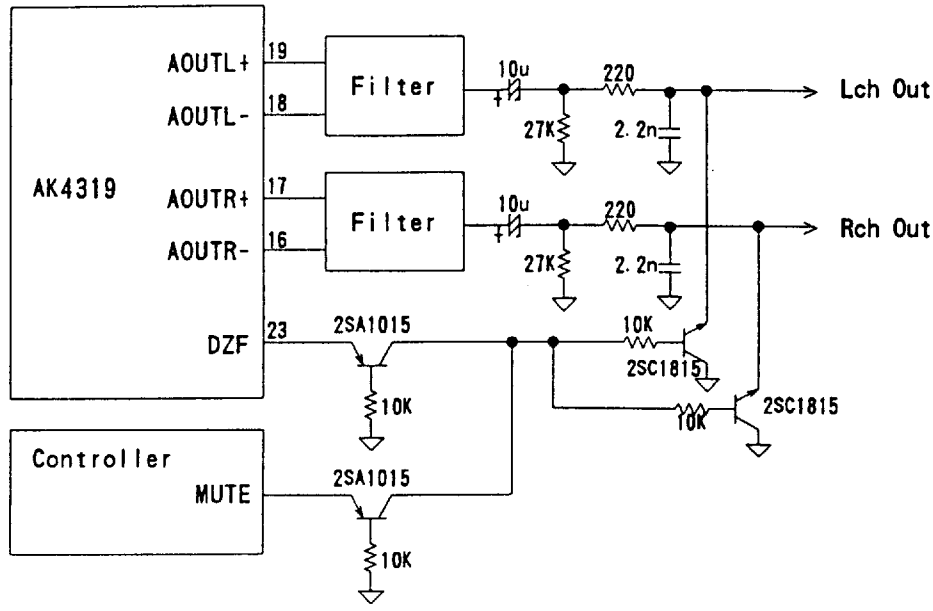


Figure 7. External mute circuit example

SYSTEM DESIGN

Figure 8 shows the system connection diagram. An example of external analog filter is shown in Figure 9. An evaluation board[AKD4318] is available in order to allow an easy study on the layout of a surrounding circuit.

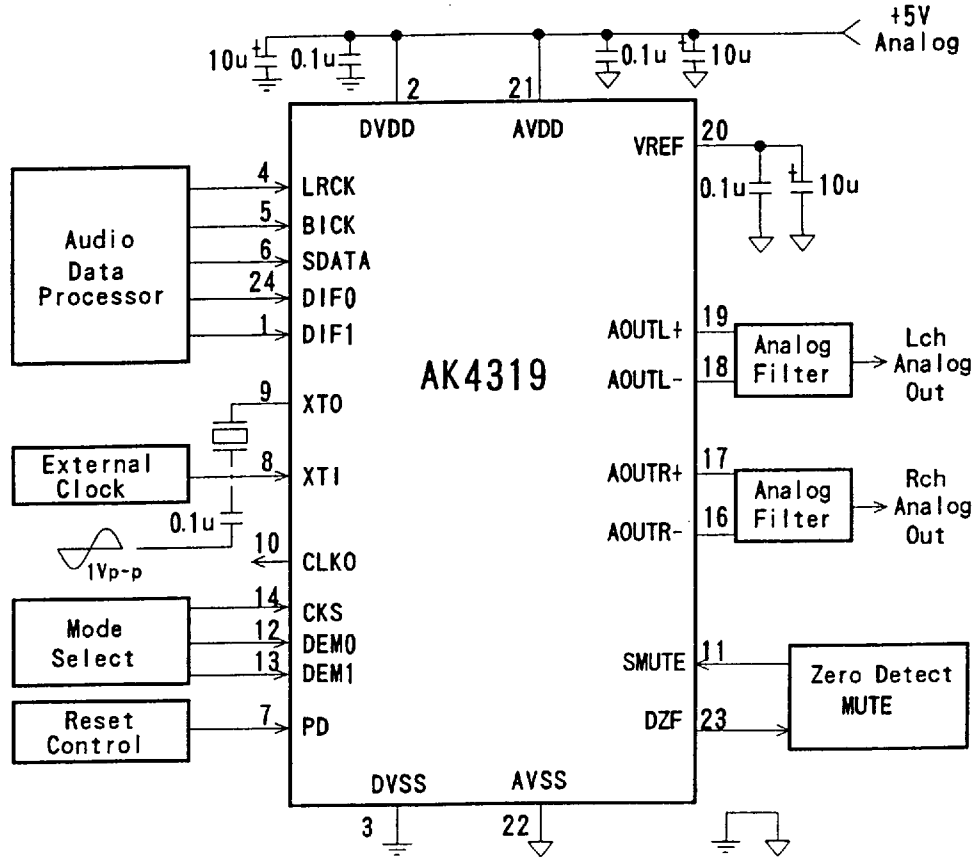


Figure 8. Typical System Connection

■ System design consideration

1. Grounding and Power Supply Decoupling

To minimize the coupling of the digital originated noise, decoupling capacitors should be connected to AVDD and DVDD pins, respectively. Decoupling capacitors should be placed as near to the AK4319 device as possible.

2. On-chip voltage reference

The on-chip voltage reference is output on the VREF pin. An electrolytic capacitor smaller than 10uF in parallel with a 0.1uF ceramic capacitor attached to this pin eliminates the effects of high frequency noise. Especially, the ceramic capacitor should be connected to VREF pin within a few mm as near as possible. No load current may be taken from the VREF output pin. All signals, especially clocks, should be kept away from the VREF pin in order to avoid unwanted coupling into the AK4319.

3. Output analog filter circuit

The analog signals are output from the differential output pins of each channel, thereforethey are summed externally. The analog outputs are the differential voltage, Δ VAOUT=(AOUT+)-(AOUT-) between AOUT+ and AOUT-. The bias voltage(Vop/2) for this summing circuit is supplied externally. The output signal range is ± 1.38V(0.975Vrms,typ) centered at an internal common voltage(AVDD/2). If the summing gain is 1, the output range is ± 2.76V (1.95Vrms,typ). The input data format is 2's complement. The output voltage(Δ VAOUT) is a positive full scale for 7FFFH(@16bit) and a negative full scale for 8000H(@16bit). The ideal Δ VAOUT is 0V for 0000H(@16bit). DC offsets on analog outputs are eliminated by AC coupling the signals since DAC outputs have a few mV offsets. The noise generated by the delta-sigma modulator beyond the audio passband is sufficently attenuated by the high speed over-sampling and by the on-chip SCF filter. However, as the outband noise moves into the audible band at low sampling rate, careful attention is required. On figure 9, the differential outputs of AK4319 are summed by the 1st-order LPF and the 1.95Vrms output signal range is acquired.

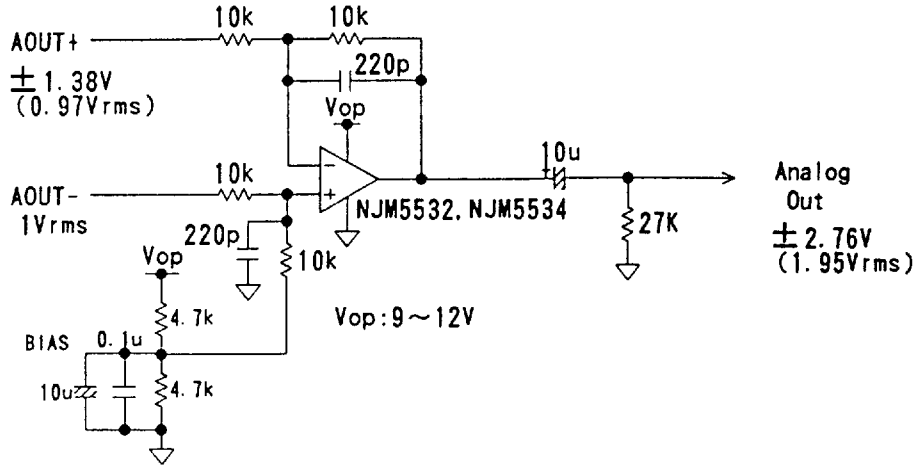


Figure 9. Differential 1st-order LPF example

4. Single-end usage

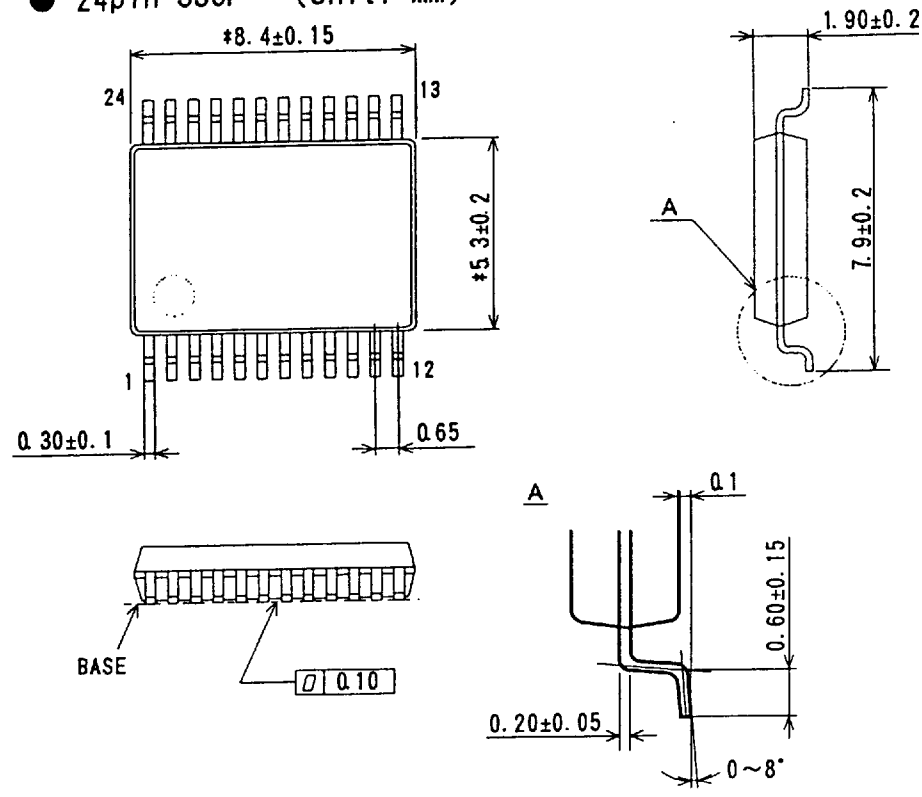
The load impedance for the output pin should be higher than 10k Ω , and the capacitive load should be less than 20pF. Hence the output pin can not drive such as line out directly. The output pin which is not used could be left open. When the device is used as a single-end cofiguration, the analog characteristics (such as THD+N, DR, S/N) may degrade by 1.5 ~ 2dB. (Experienced on our evaluation board, AKD4319)

For single-end operation, The circuit example of Fig.9 sould be modified as follw: DC isolation capacitance is added between AOUT+ and 10k Ω . Then the 10k Ω resistor which is connected to AOUT- is removed. In this case, the output level becomes 0.97Vrms.

With a single-end configuration, the device interfaces directly to external circuit such as volume AMP, which simplifes the circuit.

PACKAGE

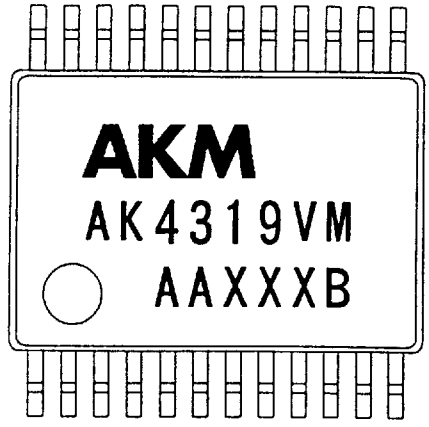
● 24pin SSOP (Unit: mm)



■ Package & Lead frame material

Package molding compound : Epoxy(Black)
Lead frame material : Cu
Lead frame surface treatment: Solder plate

MARKING



Contents of A A X X X B

A A : Lot# (alphabet)

X X X B : Date Code (X : numbers, B : alphabet)