



# AK632128W/AK632128Z 128K x 32 SRAM MODULE

## DESCRIPTION

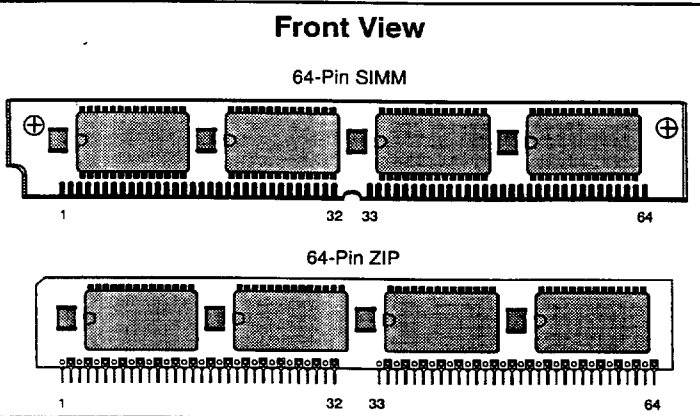
The Accuthek AK632128 SRAM Module consists of fast high performance SRAMs mounted on a low height, 64 pin SIM or ZIP Board. The module utilizes four 32 pin 128K x 8 SRAMs in 400 mil SOJ packages and four decoupling capacitors mounted on the front side of a printed circuit board. A seated height of less than 0.500 inch can be achieved with available 300 mil SOJ parts.

The SRAMs used have common I/O functions and single output enable functions. Also, four separate chip select (CE) connections are used to independently enable the four bytes. The modules can be supplied in a variety of access time values from 15 nSEC to 35 nSEC in CMOS or BiCMOS technology.

The Accuthek module is designed to have a maximum seated height of 0.620 inch SIM or 0.540 inch ZIP to provide for the lowest height off the board. Each conforms to JEDEC-standard sizes and pin-out configurations. Using two pins for module memory density identification, PD<sub>0</sub> and PD<sub>1</sub>, minimizes interchangeability and design considerations when changing from one module size to the other in customer applications.

## FEATURES

- 131,072 x 32 bit organization
- JEDEC Standard 64 pin SIM or ZIP format
- Common I/O, single OE functions with four separate chip selects (CE)
- Low height, 0.620 inch SIM or 0.540 inch ZIP maximum
- Presence Detect, PD<sub>0</sub> and PD<sub>1</sub> for identifying module density



- Downward compatible with 64K x 32 (AK63264)
- Upward compatible with 256K x 32 (AK632256 and 1 Meg x 32 (AK6321024) designs
- Fast access times from 15 nSEC
- TTL-compatible inputs and outputs
- Single +5 Volt (±10%) power supply
- Operating free air temperature 0° to 70°C

## ELECTRICAL SPECIFICATIONS

Timing diagrams and basic electrical characteristics are those of the standard 128K x 8 SRAMs used to construct these modules. Accuthek's module design allows the flexibility of selecting industry-compatible 128K x 8 SRAMs from several semiconductor manufacturers.

## PIN NOMENCLATURE

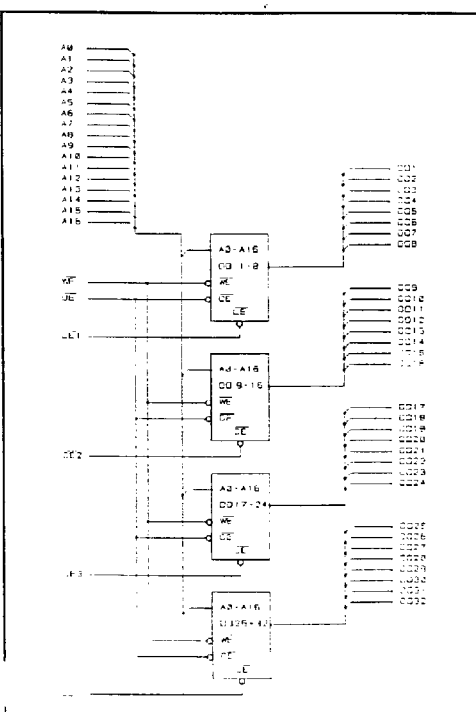
A <sub>0</sub> - A <sub>16</sub>	Address Inputs
CE <sub>1</sub> - CE <sub>4</sub>	Chip Enable
DQ <sub>1</sub> - DQ <sub>32</sub>	Data In/Data Out
OE	Output Enable
PD <sub>0</sub> - PD <sub>1</sub>	Presence Detect
Vcc	5v Supply
Vss	Ground
WE	Write Enable

## PIN ASSIGNMENT

PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL
1	Vss	17	A <sub>2</sub>	33	CE <sub>4</sub>	49	A <sub>4</sub>
2	PD <sub>0</sub>	18	A <sub>9</sub>	34	CE <sub>3</sub>	50	A <sub>11</sub>
3	PD <sub>1</sub>	19	DQ <sub>13</sub>	35	NC	51	A <sub>5</sub>
4	DQ <sub>1</sub>	20	DQ <sub>5</sub>	36	A <sub>16</sub>	52	A <sub>12</sub>
5	DQ <sub>9</sub>	21	DQ <sub>14</sub>	37	OE	53	Vcc
6	DQ <sub>2</sub>	22	DQ <sub>6</sub>	38	Vss	54	A <sub>13</sub>
7	DQ <sub>10</sub>	23	DQ <sub>15</sub>	39	DQ <sub>25</sub>	55	A <sub>6</sub>
8	DQ <sub>3</sub>	24	DQ <sub>7</sub>	40	DQ <sub>17</sub>	56	DQ <sub>21</sub>
9	DQ <sub>11</sub>	25	DQ <sub>16</sub>	41	DQ <sub>26</sub>	57	DQ <sub>29</sub>
10	DQ <sub>4</sub>	26	DQ <sub>8</sub>	42	DQ <sub>18</sub>	58	DQ <sub>22</sub>
11	DQ <sub>12</sub>	27	Vss	43	DQ <sub>27</sub>	59	DQ <sub>30</sub>
12	Vcc	28	WE	44	DQ <sub>19</sub>	60	DQ <sub>23</sub>
13	A <sub>0</sub>	29	A <sub>15</sub>	45	DQ <sub>28</sub>	61	DQ <sub>31</sub>
14	A <sub>7</sub>	30	A <sub>14</sub>	46	DQ <sub>20</sub>	62	DQ <sub>24</sub>
15	A <sub>1</sub>	31	CE <sub>2</sub>	47	A <sub>3</sub>	63	DQ <sub>32</sub>
16	A <sub>8</sub>	32	CE <sub>1</sub>	48	A <sub>10</sub>	64	Vss

PD<sub>0</sub> = Open  
PD<sub>1</sub> = Open

## FUNCTIONAL DIAGRAM



0107647 0000075 75T

## ORDER INFORMATION

## PART NUMBER CODING INTERPRETATION

Position 1 2 3 4 5 6 7 8

### 1 Product

AK = Accuthek Memory

### 2 Type

4 = Dynamic RAM  
5 = CMOS Dynamic RAM  
6 = Static RAM

### 3 Organization/Word Width

1 = by 1 16 = by 16  
4 = by 4 32 = by 32  
8 = by 8 36 = by 36  
9 = by 9

### 4 Size/Bits Depth

64 = 64K 4096 = 4 MEG  
256 = 256K 8192 = 8 MEG  
1024 = 1 MEG 16384 = 16 MEG

### 5 Package Type

G = Single In-Line Package (SIP)  
S = Single In-Line Module (SIM)  
D = Dual In-Line Package (DIP)  
W = .050 inch Pitch Edge Connect  
Z = Zig-Zag In-Line Package (ZIP)

### 6 Special Designation

P = Page Mode  
N = Nibble Mode  
K = Static Column Mode  
W = Write Per Bit Mode  
V = Video Ram

### 7 Separator

- = Commercial 0°C to +70°C  
M = Military Equivalent Screened (-55°C to +125°C)  
I = Industrial Temperature Tested (-45°C to +85°C)  
X = Burned In

### 8 Speed (first two significant digits)

DRAMs		SRAMs	
60	= 60 nS	12	= 12 nS
70	= 70 nS	20	= 20 nS
80	= 80 nS	25	= 25 nS
10	= 100 nS	35	= 35 nS

The numbers and coding on this page do not include all variations available but are shown as examples of the most widely used variations. Contact Accuthek if other information is required.

## EXAMPLES

AK632128W-15

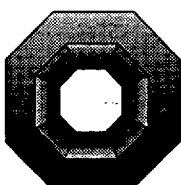
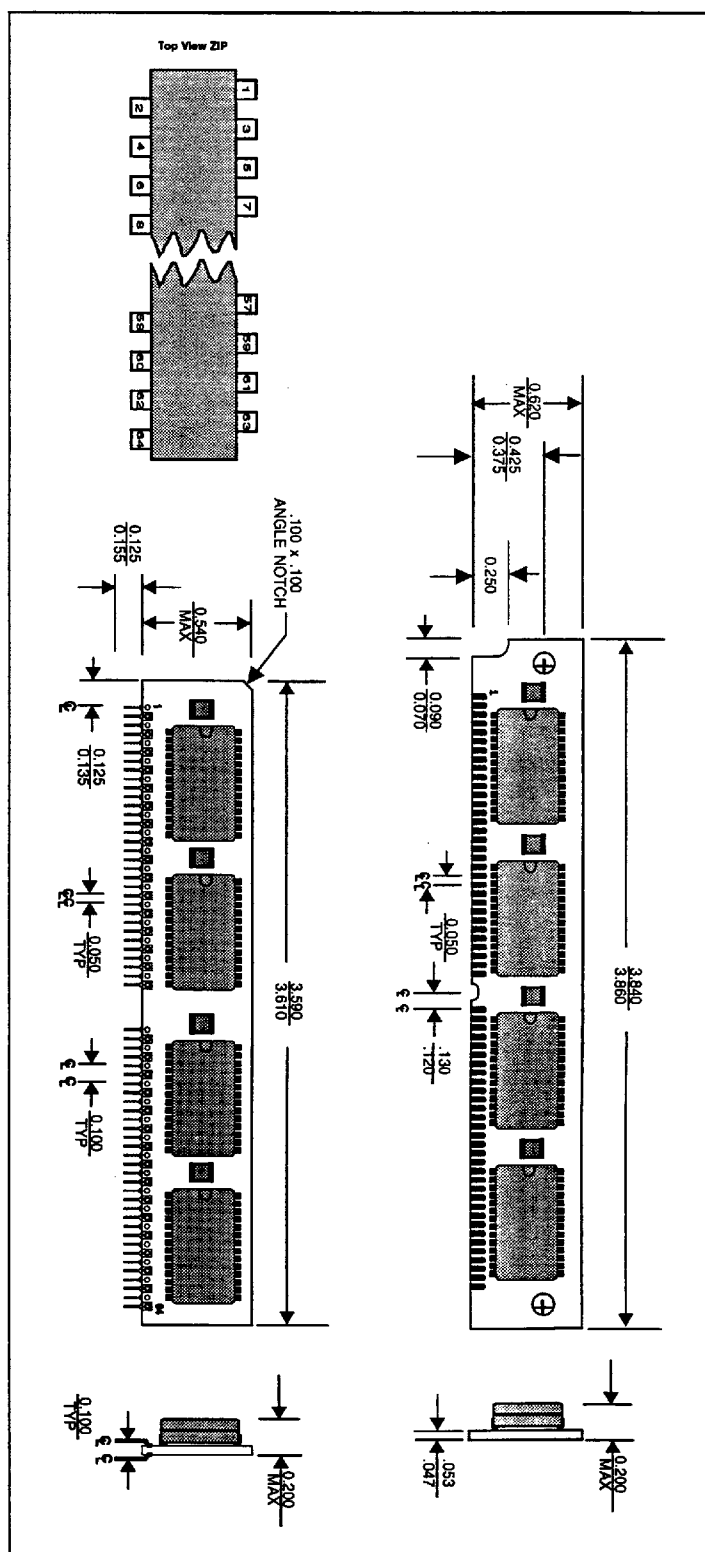
128K x 32, 15 nSEC SRAM Module, SIM Configuration

AK632128Z-25

128K x 32, 25 nSEC SRAM Module, ZIP Configuration

## MECHANICAL DIMENSIONS

Inches



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