AK7706

24bit 6ch input and 8ch output Audio DSP

General Description

The AK7706 is a highly integrated audio processing IC, including 24-bit output 8 channels and 24-bit input 6 channels, on-chip DSP. This DSP supports the standard audio sampling frequencies of 48,44.1 and 32kHz.

The programmable DSP is optimized for audio signal processing. The design allows up to 512 execution lines per audio sample cycle, with multiple functions per line. And it can allows up to 256 execution lines on double speed audio sample cycle (88.2kHz and 96kHz).

The AK7706 can be used to implement complete sound field control, such as echo, 3D, parametric equalization, etc. It is packaged in a 64-lead LQFP package. Also it is available to use on 3.3V power supply.

Features

DSP:

- **Word length: 24-bit (Data RAM)**
- **Instruction cycle time: 40.7ns (512fs, fs=48kHz @5.0V or 256fs, fs=96kHz @5.0V)**
- **54.2ns (384fs, fs=48kHz @3.3V)**
- **Multiplier: 24 x 16 → 40-bit**
- **Divider: 24 / 24 → 16-bit**
- **ALU: 34-bit arithmetic operation (Overflow margin: 4bit)**
- **24-bit arithmetic and logic operation**
- **Shift+Register: 1, 2, 3, 4, 8 and 15 bits shifted left**
- **1, 2, 3, 4, 8 and 15 bits shifted right**
- **Other numbers in parentheses are restricted. Provided with indirect shift function**
- **Program RAM: 512 x 32-bit**
- **Coefficient RAM: 384 x 16-bit**
- **Data RAM: 256 x 24-bit**
- **Offset RAM: 48 x 20-bit**
- **External Memory: Up to16Mbit DRAM or up to 1Mbit SRAM**
- **Sampling frequency: 32kHz to 96kHz**
- **Serial interface port for micro-controller**
- **Master clock: 512fs, 384fs, 256fs(512fs available only at 5.0V power supply)**
- **Master/Slave operation**
- **Serial signal input port (6 ch): 16/20/24-bit MSB-justify, I^2S, LSB-justify**
- **Serial signal output port (8 ch): 24-bit : MSB-justify, I^2S**

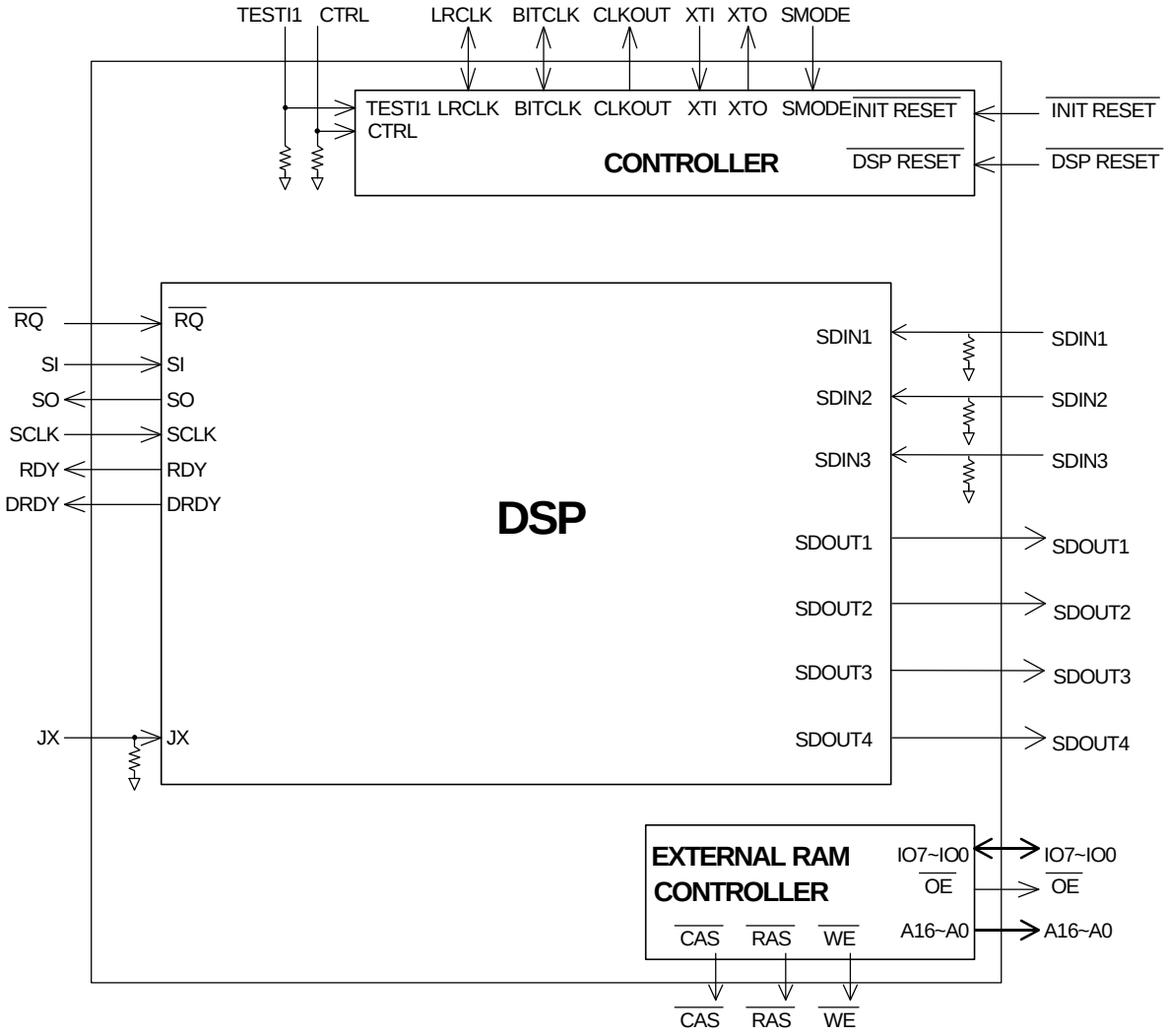
Other

- **Power supply: +5.0V±5% or +3.3V±10%**
- **Operating temperature range: -40°C~85°C**

Package: 64pin LQFP (0.5mm pitch)

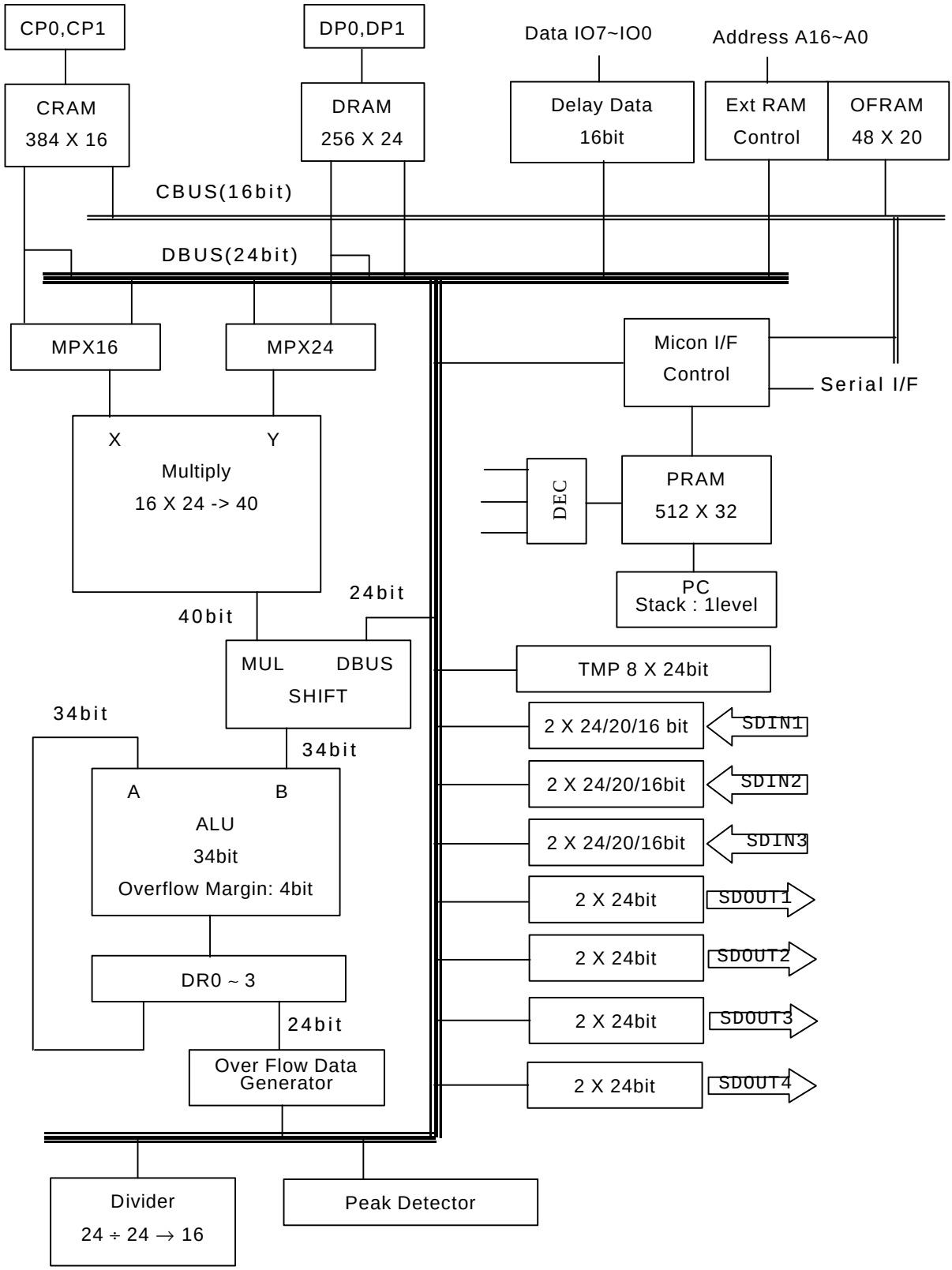
Block diagram

- **For standard operation (Internal connection mode: initial settings)**



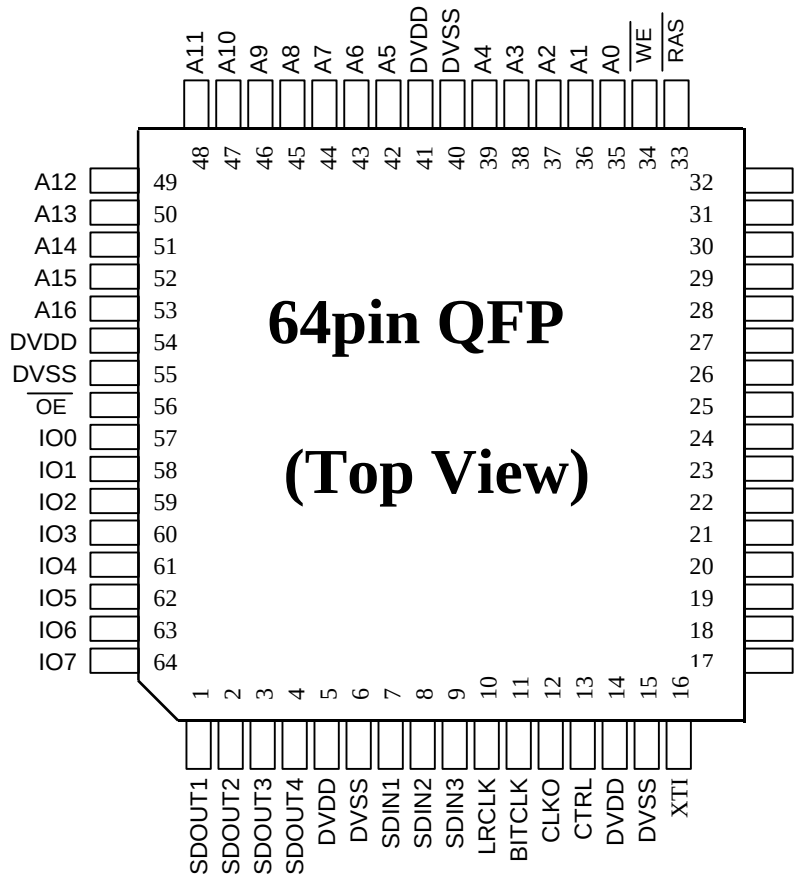
This block diagram is a simplified illustration of the AK7706; it is not a circuit diagram.

- **Block Diagram of AK7706 DSP Section**



Description of Input/Output Pins

(1) Pin layout



(2) Pin function

Pin No.	Pin name	I/O	Function	Classification
1	SDOUT1	O	**DSP Serial data output pin.** Outputs MSB justified 24-bit or IIS data.	Digital section Serial input/output data
2	SDOUT2	O	**DSP Serial data output pin.** Outputs MSB justified 24-bit or IIS data.	
3	SDOUT3	O	**DSP Serial data output pin.** Outputs MSB justified 24-bit or IIS data.	
4	SDOUT4	O	**DSP Serial data output pin.** Outputs MSB justified 24-bit or IIS data.	
5	DVDD	-	**Power supply pin for digital section 5V (typ)** +5V Digital power supply.	Power supply
6	DVSS	-	**Digital ground pin**	
7	SDIN1	I	**DSP Serial data input pin (Pulldown)** Compatible with MSB/LSB justified 24, 20 and 16 bits and IIS.	Digital section Serial input data
8	SDIN2	I	**DSP Serial data input pin (Pulldown)** Compatible with MSB/LSB justified 24, 20 and 16 bits and IIS.	
9	SDIN3	I	**DSP Serial data input pin (Pulldown)** Compatible with MSB/LSB justified 24, 20 and 16 bits and IIS.	

Pin No.	Pin name	I/O	Function	Classification
10	LRCLK	I/O	**LR channel select Clock pin** SMODE="L": Slave mode: Inputs the fs clock. SMODE="H": Master mode: Outputs the fs clock.	System clock
11	BITCLK	I/O	**Serial bit clock pin** SMODE="L": Slave mode: Inputs 64 fs or 48 fs clocks. SMODE="H": Master mode: Outputs 64 fs clocks.	
12	CLKO	O	**Clock output pin** Outputs the XTI clock. Allows the output to be set to "L" when CTRL is “H”.	
13	CTRL	I	**Clock output control pin** **CTRL=”L”: CLKO is enable.** **CTRL=”H”: CLKO outputs ”L”.**	Control
14	DVDD	-	**Power supply pin for digital section 5V or 3.3V (typ)** +5V Digital power supply.	Power supply
15	DVSS	-	**Digital ground pin**	
16	XTI	I	**Master clock input pin** Connect a crystal oscillator between this pin and the XTO pin, or input the external CMOS clock signal XTI pin.	System clock
17	XTO	O	**Crystal oscillator output pin** When a crystal oscillator is used, it should be connected between XTI and XTO. When the external clock is used, keep this pin open	
18	TESTI1	I	**Test pin: Leave open or connect to DVSS. (Pulldown)**	Test
19	$\overline{\text{INIT\_RESET}}$	I	**Reset pin (for initialization)** Used to input “L” initialize the AK7706 at power-on	Reset Control
20	$\overline{\text{DSP\_RESET}}$	I	**Reset pin** **Reset for DSP section.**	
21	SMODE	I	**Slave/master mode selector pin** Set LRCLK and BITCLK to input or output mode. SMODE="L": Slave mode (LRCLK and BITCLK are set to input mode.) SMODE="H": Master mode (LRCLK and BITCLK are set to output mode.)	Control
22	JX	I	**External condition jump pin (Pulldown)**	Microcomputer interface

Pin No.	Pin name	I/O	Function	Classification
23	$\overline{RQ}$	I	**Microcomputer interface writes request pin.** $\overline{RQ}$ ="L": Microcomputer interface enable.	Microcomputer interface
24	SCLK	I	**Microcomputer interface serial data clock pin.** When SCLK does not use, leave SCLK="H".	
25	SI	I	**Microcomputer interface serial data input and serial data output control pin.** When SI does not use, leave SI="L".	
26	DVSS	-	**Ground pin for digital section.**	Power supply
27	DVDD	-	**Power supply pin for digital section 5V or 3.3V (typ)**	
28	SO	O	**Serial data output pin for Microcomputer interfaces.**	Microcomputer interface
29	RDY	O	**Data write ready output pin for Microcomputer interface.**	
30	DRDY	O	**Output data ready pin for Microcomputer interface.**	
31	LSEL	I	**Input level selector pin.** When using 5.0V power supply, the level of this pin decides input pin level. When this pin level is "H", then TTL level input is available. When using 3.3V power supply, this pin must leave open or connects to DVSS.	Level select
32	$\overline{CAS}$	I	**$\overline{CAS}$ Pin for external DRAM.**	External RAM Inteface
33	$\overline{RAS}$	I	**$\overline{RAS}$ pin for external DRAM**	
34	$\overline{WE}$	O	**Writes enable pin for external SRAM/DRAM.**	
35 ~ 39	A0 ~ A4	O	**Address output for external RAM (A0~A4)**	
40	DVSS	-	**Ground pin for digital section 0V.**	Power supply
41	DVDD	-	**Power supply pin for digital section 5V or 3.3V (typ)**	
42 ~ 53	A5 ~ A16	O	**Address output for external RAM (A5~A16)**	External RAM Interface
54	DVSS	-	**Ground pin for digital section 0V.**	Power supply
55	DVDD	-	**Power supply pin for digital section 5V or 3.3V (typ)**	
56	$\overline{OE}$	O	**Output enable signal output for external SRAM/DRAM.**	External RAM Interface
57 ~ 64	IO0 ~ IO7	I/O	**Data input / output for external SRAM / DRAM.** These pins work as output pin unless READ data from external RAM instruction. If it does not connect external RAM then leave open.	

Absolute maximum rating

(DVSS = 0 V: All voltages indicated are relative to the ground.)

Item	Symbol	Min	Max	Unit
Power supply voltage Digital (DVDD)	VD	-0.3	6.0	V
Input current (except for power supply pin)	IIN	-	±10	mA
Digital input voltage	VIND	-0.3	6.0	V
Operating ambient temperature	Ta	-40	85	°C
Storage temperature	Tstg	-65	150	°C

WARNING: Operation at or beyond these limits may result in permanent damage of the device.
Normal operations are not guaranteed under these critical conditions in principle.

Recommended operating conditions

Power Supply : 5.0V

(DVSS = 0 V: All voltages indicated are relative to the ground.)

Items		Min	Typ	Max	Unit
Power supply voltage DVDD	VD	4.75	5.0	5.25	V

Power Supply : 3.3V

(DVSS = 0 V: All voltages indicated are relative to the ground.)

Items		Min	Typ	Max	Unit
Power supply voltage DVDD	VD	3.0	3.3	3.6	V

Electric characteristics

(1) DC characteristics

(DVDD=5.0V±5%,Ta=25°C)

Parameter	Symbol	Min	Typ	Max	Unit
High level input voltage In the case of LSEL="H" Input pins other than XTI, TESTI1 and IO7~0 XTI, TESTI1, LSEL and IO7~0 pins or all input pins in the case of LSEL = "L"	VIH	 2.4 70%DVDD			 V V
Low level input voltage In the case of LSEL="H" Input pins other than XTI, TESTI1 and IO7~0 XTI, TESTI1 and IO7~0 pins or all input pins in the case of LSEL = "L"	VIL			 0.6 30%DVDD	 V V
High level output voltage Iout=-100μA Low level output voltage Iout=100μA	VOH VOL	DVDD-0.5		 0.5	V V
Input leak current Note 1) Input leak current Pull down pin Note 1)	Iin Iid		 100	±10	μA μA

(DVDD=3.3V±10%,Ta=25°C)

Parameter	Symbol	Min	Typ	Max	Unit
High level input voltage All input pins.	VIH	 70%DVDD			 V
Low level input voltage All input pins.	VIL			 30%DVDD	 V
High level output voltage Iout=-100μA Low level output voltage Iout=100μA	VOH VOL	DVDD-0.5		 0.5	V V
Input leak current Note 1) Input leak current Pull down pin Note 1)	Iin Iid		 100	±10	μA μA

Note: 1. The pull down pins is not included.
2. The pull down pins is as follows (Typ 50kΩ):
TESTI1,SDIN1, SDIN2,SDIN3, CTRL, JX, LSEL

Note: Regarding the input/output levels in the text, the low level will be represented as "L" or 0, and the high level as "H" or 1. In principle, "0" and "1" will be used to represent the bus (serial/parallel) such as registers.

(2) Current consumption

(DVDD=5.0V±5%, Ta=25°C; master clock (XTI)=24.576MHz=512fs[fs=48kHz])

Power supply				
Parameter	Min	Typ	Max	Unit
Power supply current				
1) During operation				
DVDD Note 1)		42	65	mA
2) $\overline{\text{INIT RESET}}$ ="L" (Reference value) Note 2)		8		mA
Power consumption				
1) During operation				
DVDD Note 1)		210	330	mW
2) $\overline{\text{INIT RESET}}$ ="L" (Reference value) Note 2)		40		mW

(DVDD=3.3V±10%, Ta=25°C; master clock (XTI)=18.432MHz=384fs[fs=48kHz])

Power supply				
Parameter	Min	Typ	Max	Unit
Power supply current				
1) During operation				
DVDD Note 1)		20	35	mA
2) $\overline{\text{INIT RESET}}$ ="L" (Reference value) Note 2)		4		mA
Power consumption				
1) During operation				
DVDD Note 1)		65	120	mW
2) $\overline{\text{INIT RESET}}$ ="L" (Reference value) Note 2)		14		mW

Note 1 Varies slightly according to the frequency used and contents of the DSP program.
Note 2 This is a reference value in case of using the crystal oscillator.
Because of the most of power current at the initial reset state is oscillator section,
the varies slightly according to the types of crystal oscillators and external circuits.

(3) Switching characteristics

3-1) System clock

(DVDD=5.0V±5%,Ta=-40~85°C,CL=20pF)

Parameter	Symbol	min	typ	max	Unit
Master clock (XTI)					
a) With a crystal oscillator:					
256fs: frequency	fMCLK	11.000	11.2896	24.576	MHz
384fs: frequency	fMCLK	12.288	16.9344	18.432	MHz
512fs: frequency	fMCLK	16.384	22.5792	24.576	MHz
b)With a external clock:					
Duty factor (XTI ≤16.4MHz)		33	50	67	%
(16.4MHz < XTI ≤ 18.5MHz)		40	50	60	
(>18.5MHz)		45	50	55	
256fs:frequency	fMCLK	11.000	11.2896	12.288	MHz
: High level width	tMCLKH	30			ns
: Low level width	tMCLKL	30			ns
384fs:frequency	fMCLK	12.288	16.9344	18.432	MHz
: High level width	tMCLKH	20			ns
: Low level width	tMCLKL	20			ns
512fs:frequency	fMCLK	16.384	22.5792	24.576	MHz
: High level width	tMCLKH	16			ns
: Low level width	tMCLKL	16			ns
Clock rise time	tCR			6	ns
Clock fall time	tCF			6	ns
LRCLK Sampling frequency	fs	32	44.1	96	kHz
			1		fs
Slave mode :clock rise time	tLR			10	ns
Slave mode :clock fall time	tLF			10	ns
BITCLK Note 1)	fBCLK	48	64		fs
Slave mode: High level width	tBCLKH	65			ns
Slave mode: Low level width	tBCLKL	65			ns
Slave mode :clock rise time	tBR			6	ns
Slave mode :clock fall time	tBF			6	ns

Note 1) 48fs mode can be use only at slave mode.

(DVDD=3.3V±10%,Ta=-40~85°C,CL=20pF)

Parameter	Symbol	min	typ	max	Unit
Master clock (XTI)					
a) With a crystal oscillator:					
256fs: frequency	fMCLK	11.000	11.2896	24.576	MHz
384fs: frequency	fMCLK	12.288	16.9344	18.432	MHz
b)With a external clock:					
Duty factor (XTI ≤12.3MHz) (>12.3MHz)		40 45	50 50	60 55	%
256fs:frequency : High level width : Low level width	fMCLK tMCLKH tMCLKL	11.000 30 30	11.2896	12.288	MHz ns ns
384fs:frequency : High level width : Low level width	fMCLK tMCLKH tMCLKL	12.288 20 20	16.9344	18.432	MHz ns ns
Clock rise time Clock fall time	tCR tCF			6 6	ns ns
LRCLK Sampling frequency	fs	32	44.1 1	48	kHz fs
Slave mode :clock rise time Slave mode :clock fall time	tLR tLF			10 10	ns ns
BITCLK Note 1)	fBCLK	48	64		fs
Slave mode: High level width Slave mode: Low level width	tBCLKH tBCLKL	100 100			ns ns
Slave mode :clock rise time Slave mode :clock fall time	tBR tBF			6 6	ns ns

Note 1) 48fs mode can be use only at slave mode.

3-2) Reset

(DVDD=5.0V±5% or 3.3V±10%,Ta=-40~85°C,CL=20pF)

Parameter	Symbol	min	typ	max	Unit
$\overline{\text{INIT RESET}}$ Note 2)	tRST	150			ns
$\overline{\text{DSP RESET}}$	tRST	150			ns

Note 2) “L” is acceptable when power is turned on, but ”H” needs stable master clock input.

3-3) Audio interface

(DVDD=5.0V±5%,Ta=-40~85°C,CL=20pF)

Parameter	Symbol	min	typ	max	Unit
Slave mode					
BITCLKfrequency	fBCLK	48	64		fs
BITCLK low level width	tBCLKL	65			ns
BITCLK high level width	tBCLKH	65			ns
Delay time from BITCLK"↑" to LRCLK	tBLRD	40			ns
Delay time from LRCLK to BITCLK "↑"	tLRBD	40			ns
Delay time from LRCLK to serial data output	tLRD			70	ns
Delay time from BITCLK to serial data output	tBSOD			70	ns
Serial data input latch hold time	tBSIDS	40			ns
Serial data input latch setup time	tBSIDH	40			ns
Master mode					
BITCLK frequency	fBCLK		64		fs
BITCLK duty factor			50		%
Delay time from BITCLK"↑" to LRCLK	tBLRD	40			ns
Delay time from LRCLK to BITCLK"↑"	tLRBD	40			ns
Delay time from LRCLK to serial data output	tLRD			70	ns
Delay time from BITCLK to serial data output	tBSOD			70	ns
Serial data input latch hold time	tBSIDS	40			ns
Serial data input latch setup time	tBSIDH	40			ns

(DVDD=3.3V±10%,Ta=-40~85°C,CL=20pF)

Parameter	Symbol	min	typ	max	Unit
Slave mode					
BITCLKfrequency	fBCLK	48	64		fs
BITCLK low level width	tBCLKL	100			ns
BITCLK high level width	tBCLKH	100			ns
Delay time from BITCLK"↑" to LRCLK	tBLRD	80			ns
Delay time from LRCLK to BITCLK "↑"	tLRBD	80			ns
Delay time from LRCLK to serial data output	tLRD			140	ns
Delay time from BITCLK to serial data output	tBSOD			140	ns
Serial data input latch hold time	tBSIDS	80			ns
Serial data input latch setup time	tBSIDH	80			ns
Master mode					
BITCLK frequency	fBCLK		64		fs
BITCLK duty factor			50		%
Delay time from BITCLK"↑" to LRCLK	tBLRD	80			ns
Delay time from LRCLK to BITCLK"↑"	tLRBD	80			ns
Delay time from LRCLK to serial data output	tLRD			140	ns
Delay time from BITCLK to serial data output	tBSOD			140	ns
Serial data input latch hold time	tBSIDS	80			ns
Serial data input latch setup time	tBSIDH	80			ns

3-4) Microcomputer interface

(DVDD=5.0V±5%,Ta=-40~85°C,CL=20pF)

Parameter	Symbol	min	typ	max	Unit
Microcomputer interface signal					
$\overline{RQ}$ Fall time	tWRF			10	ns
$\overline{RQ}$ Rise time	tWRR			10	ns
SCLK fall time	tSF			10	ns
SCLKrise time	tSR			10	ns
SCLK low level width	tSCLKL	150			ns
SCLK high level width	tSCLKH	150			ns
Microcomputer to AK7706					
Time from $\overline{RESET}$ "↓" to $\overline{RQ}$ "↓"	tREW	200			ns
Time from $\overline{RQ}$ "↑" to $\overline{RESET}$ "↑" Note 1)	tWRE	200			ns
$\overline{RQ}$ high level width	tWRQH	200			ns
Time from $\overline{RQ}$ "↓" to SCLK"↓"	tWSC	200			ns
Time from SCLK"↑" to $\overline{RQ}$ "↑"	tSCW	6 x tMCLK			ns
SI latch setup time	tSIS	100			ns
SI latch hold time	tSIH	100			ns
AK7706 to microcomputer					
Time from SCLK"↑" to DRDY"↓"	tSDR			3 x tMCLK	ns
Time from SI"↑"to DRDY"↓"	tSIDR			3 x tMCLK	ns
SI high level width	tSIH	3 x tMCLK			ns
Delay time from SCLK"↓" to SO output	tSOS			100	ns
AK7706 to microcomputer (RAM DATA read-out)					
SI latch setup time (SI="H")	tRSISH	100			ns
SI latch setup time (SI="L")	tRSISL	100			ns
SI latch hold time	tRSIH	100			ns
Time from SCLK"↓" to SO	tSOD			100	ns

Note 1) Except for external jump code set at reset state.

(DVDD=3.3V±10%,Ta=-40~85°C,CL=20pF)

Parameter	Symbol	min	typ	max	Unit
Microcomputer interface signal					
$\overline{RQ}$ Fall time	tWRF			10	ns
$\overline{RQ}$ Rise time	tWRR			10	ns
SCLK fall time	tSF			10	ns
SCLKrise time	tSR			10	ns
SCLK low level width	tSCLKL	150			ns
SCLK high level width	tSCLKH	150			ns
Microcomputer to AK7706					
Time from $\overline{RESET}$ "↓" to $\overline{RQ}$ "↓"	tREW	300			ns
Time from $\overline{RQ}$ "↑" to $\overline{RESET}$ "↑" Note 1)	tWRE	300			ns
$\overline{RQ}$ high level width	tWRQH	300			ns
Time from $\overline{RQ}$ "↓" to SCLK"↓"	tWSC	300			ns
Time from SCLK"↑" to $\overline{RQ}$ "↑"	tSCW	6 x tMCLK			ns
SI latch setup time	tSIS	200			ns
SI latch hold time	tSIH	200			ns
AK7706 to microcomputer					
Time from SCLK"↑" to DRDY"↓"	tSDR			3 x tMCLK	ns
Time from SI"↑"to DRDY"↓"	tSIDR			3 x tMCLK	ns
SI high level width	tSIH	3 x tMCLK			ns
Delay time from SCLK"↓" to SO output	tSOS			200	ns
AK7706 to microcomputer (RAM DATA read-out)					
SI latch setup time (SI="H")	tRSISH	200			ns
SI latch setup time (SI="L")	tRSISL	200			ns
SI latch hold time	tRSIH	200			ns
Time from SCLK"↓" to SO	tSOD			200	ns

Note 1) Except for external jump code set at reset state.

5-5) External RAM interface

1) Read/Write Interface Timing of External RAM (Static RAM)
(DVDD=5.0V±5%, Ta=-40~85°C, CL=20pF, XTI=24.576MHz)

Parameter	Symbol	min	Max	Units
Address delay time from $\overline{OE}$ Low to High (Writing)	tAOEW	-15	15	ns
Address delay time from $\overline{OE}$ High to Low (Reading)	tAOER	-15	15	ns
Access time	tWCY	100		ns
Address set-up time	tWD	25		ns
Data set time	tDS	70		ns
Data hold time	tDH	8		ns
Pulse width to write	tWP	40		ns

2) Read/Write Interface Timing of External RAM (Dynamic RAM) (Fast Page Mode Read Cycle / Early Write Cycle)
(DVDD=5.0V ± 5%, Ta=-40~85°C, CL=20pF, XTI=24.576MHz)

Parameter	Symbol	min	Max	Units
Access time	tRAC	85		ns
Address delay time from $\overline{OE}$ "L" to "H" (Writing)	tAOEW	-15	15	ns
Write command setup time	tWCS	20		ns
Write command hold time	tWCH	20		ns
Address delay time from $\overline{OE}$ "H" to "L" (Reading)	tAOER	-15	15	ns
Read command setup time	tRCS	85		ns
Read command hold time to $\overline{CAS}$	tRCH	20		ns
Read command hold time to $\overline{RAS}$	tRRH	35		ns
$\overline{RAS}$ preceded address setup time	tSURA	0		ns
$\overline{RAS}$ followed address hold time	tHRA	5		ns
$\overline{CAS}$ preceded address setup time	tSUCA	0		ns
$\overline{CAS}$ followed address hold time	tHCLCA	35		ns
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	20		ns
$\overline{RAS}$ hold time	tRSH	20		ns
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	20		ns
Data setup time	tSUD	35		ns
Data hold time after write	tHWLD	35		ns
Pulse width of $\overline{CAS}$ "H"	tWCH	20		ns
Pulse width of $\overline{CAS}$ "L"	tWCL	35		ns

3) Refresh Interface Timing of External RAM (Dynamic RAM) (CAS before RAS Refresh)
(DVDD=5.0V±5%, Ta=-40~85°C, CL=20pF, XTI=24.576MHz)

Parameter	Symbol	Min	Max	Units
Read cycle	tCRD	260		ns
Pulse width of $\overline{RAS}$ "H"	tWRH	85		ns
Pulse width of $\overline{RAS}$ "L"	tWRL	170		ns
$\overline{RAS}$ Pre-charge / $\overline{CAS}$ hold time	tRPC	70		ns
$\overline{CAS}$ setup time at auto refresh	tSUR	5		ns
$\overline{CAS}$ hold time at auto refresh	tHRRC	100		ns

4) Read/Write Interface Timing of External RAM (Static RAM)
(DVDD=3.3V±10%, Ta=-40~85°C, CL=20pF, XTI=18.432MHz)

Parameter	Symbol	min	Max	Units
Address delay time from $\overline{OE}$ Low to High (Writing)	tAOEW	-15	15	ns
Address delay time from $\overline{OE}$ High to Low (Reading)	tAOER	-15	15	ns
Access time	tWCY	130		ns
Address set-up time	tWD	30		ns
Data set time	tDS	95		ns
Data hold time	tDH	10		ns
Pulse width to write	tWP	50		ns

5) Read/Write Interface Timing of External RAM (Dynamic RAM) (Fast Page Mode Read Cycle / Early Write Cycle)
(DVDD=3.3V ± 10%, Ta=-40~85°C, CL=20pF, XTI=18.432MHz)

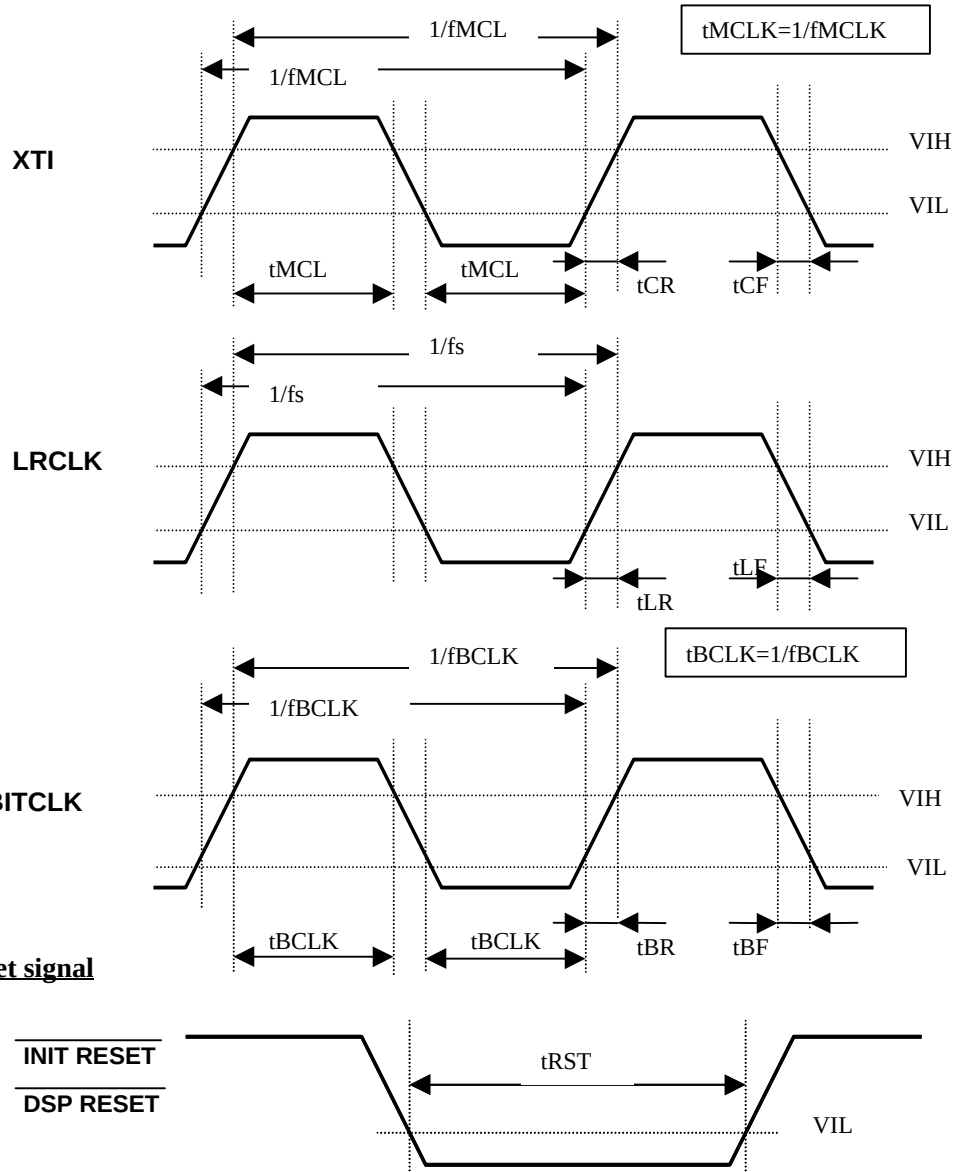
Parameter	Symbol	min	Max	Units
Access time	tRAC	110		ns
Address delay time from $\overline{OE}$ "L" to "H" (Writing)	tAOEW	-15	15	ns
Write command setup time	tWCS	30		ns
Write command hold time	tWCH	30		ns
Address delay time from $\overline{OE}$ "H" to "L" (Reading)	tAOER	-15	15	ns
Read command setup time	tRCS	110		ns
Read command hold time to $\overline{CAS}$	tRCH	30		ns
Read command hold time to $\overline{RAS}$	tRRH	50		ns
$\overline{RAS}$ preceded address setup time	tSURA	0		ns
$\overline{RAS}$ followed address hold time	tHRA	10		ns
$\overline{CAS}$ preceded address setup time	tSUCA	0		ns
$\overline{CAS}$ followed address hold time	tHCLCA	50		ns
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	30		ns
$\overline{RAS}$ hold time	tRSH	30		ns
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	30		ns
Data setup time	tSUD	50		ns
Data hold time after write	tHWLD	50		ns
Pulse width of $\overline{CAS}$ "H"	tWCH	30		ns
Pulse width of $\overline{CAS}$ "L"	tWCL	50		ns

6) Refresh Interface Timing of External RAM (Dynamic RAM) (CAS before RAS Refresh)
(DVDD=3.3V±10%, Ta=-40~85°C, CL=20pF, XTI=18.432MHz)

Parameter	Symbol	Min	Max	Units
Read cycle	tCRD	350		ns
Pulse width of $\overline{RAS}$ "H"	tWRH	100		ns
Pulse width of $\overline{RAS}$ "L"	tWRL	200		ns
$\overline{RAS}$ Pre-charge / $\overline{CAS}$ hold time	tRPC	80		ns
$\overline{CAS}$ setup time at auto refresh	tSUR	0		ns
$\overline{CAS}$ hold time at auto refresh	tHRRC	110		ns

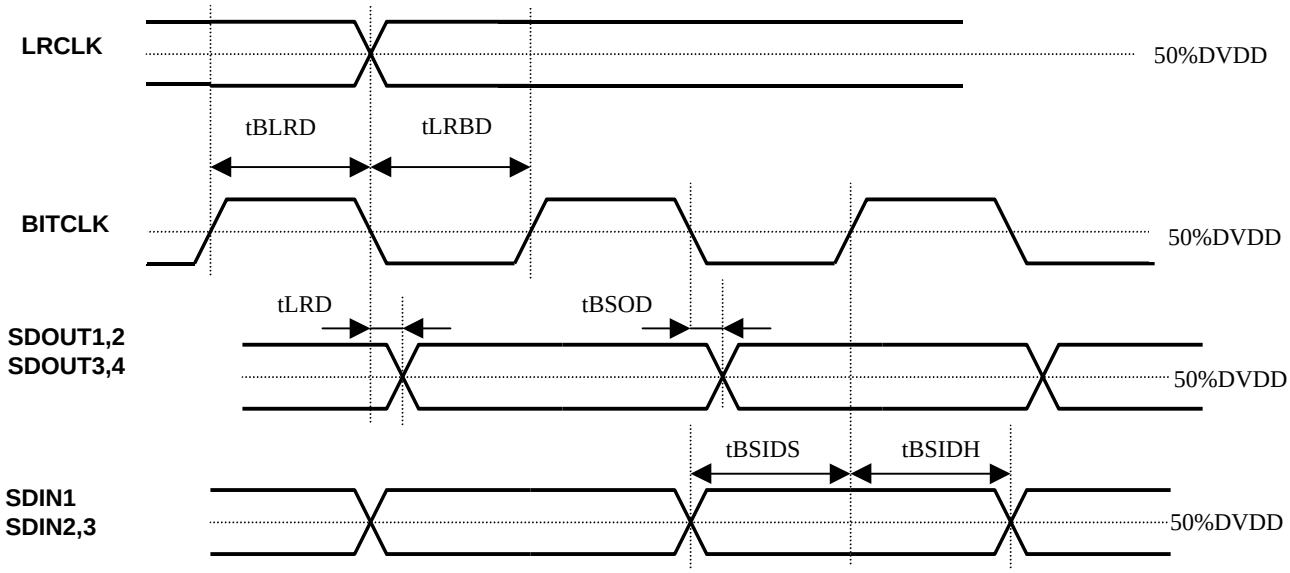
(4) Timing waveform

4-1) System clock



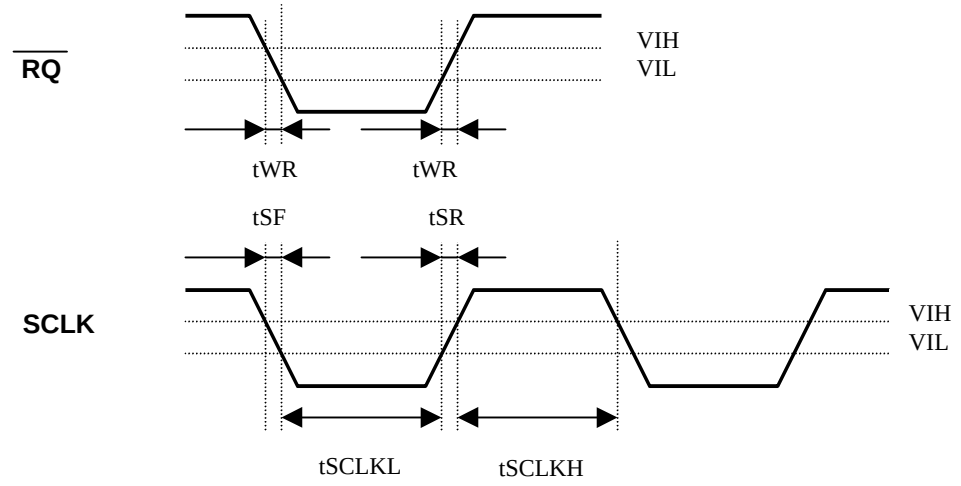
4-2) Reset signal

4-3) Audio interface

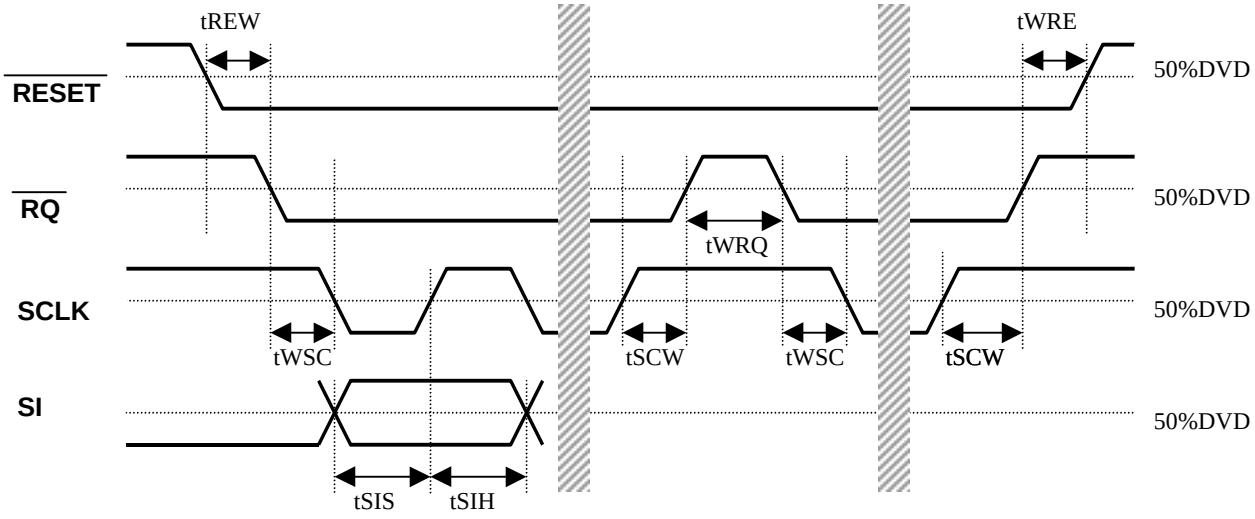


4-4) Microcomputer interface

- Microcomputer interface signals



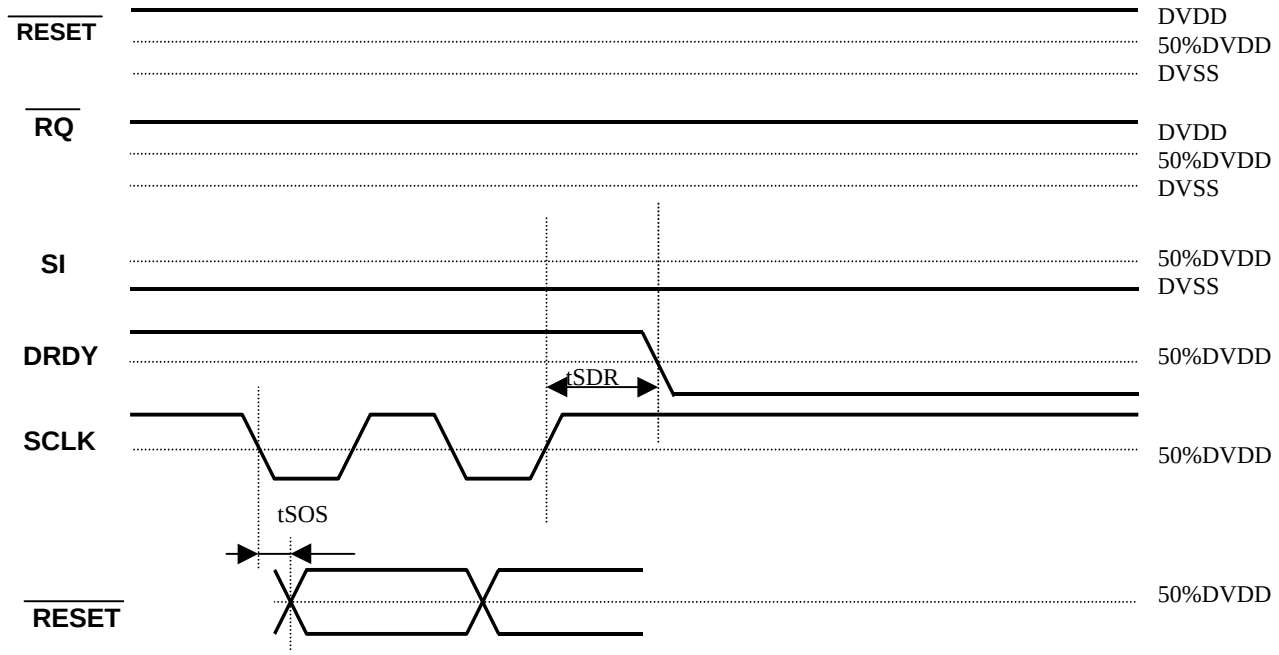
- Microcomputer to AK7706



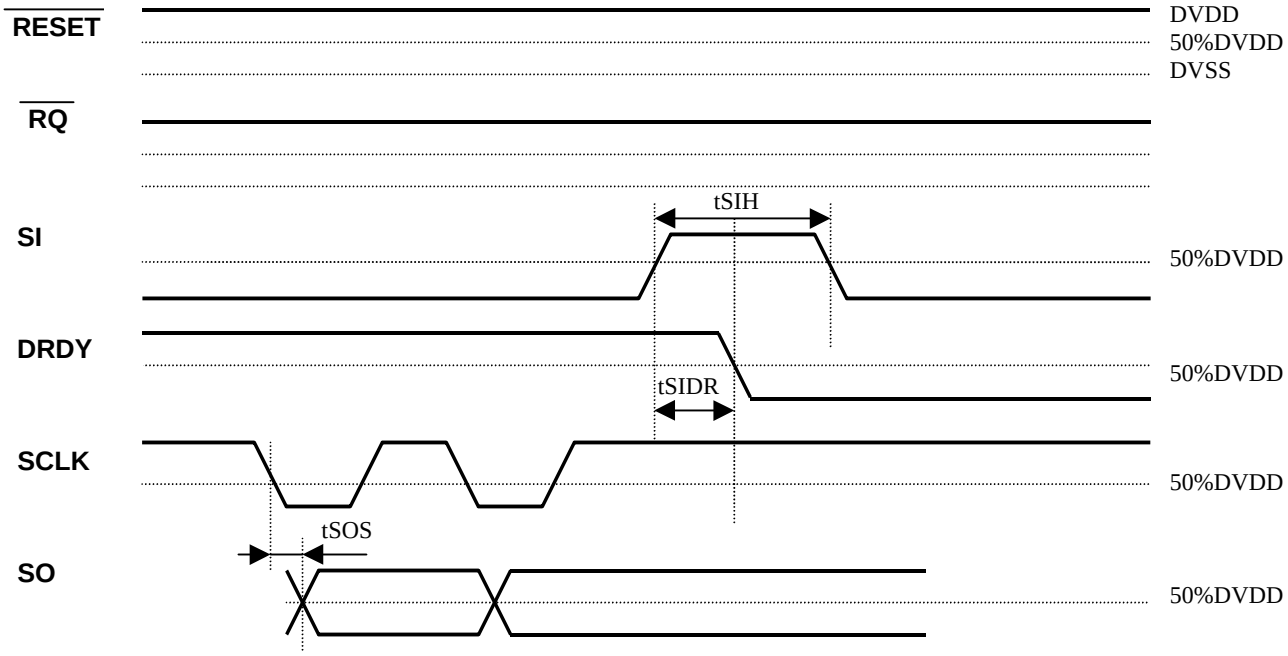
NOTE : Timing for RUN state is the same except that $\overline{\text{RESET}}$ is set to a "H"
$\overline{\text{RESET}}$ represents system reset in normal use.

- AK7706 to Microcomputer (DBUS data)

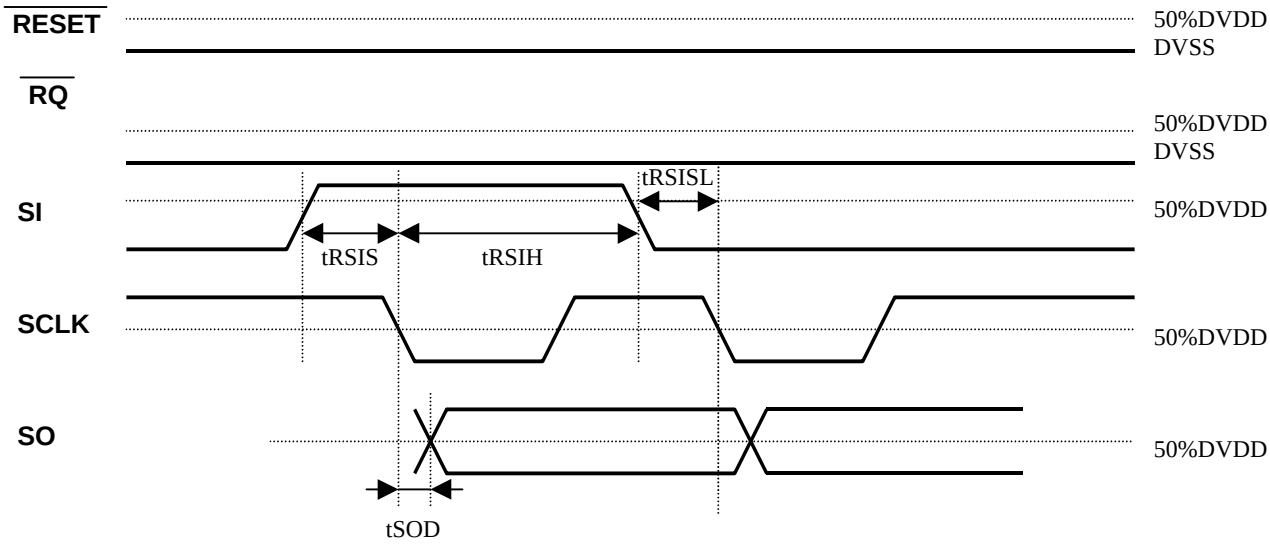
1) DBUS data in case of 24 bit data output.



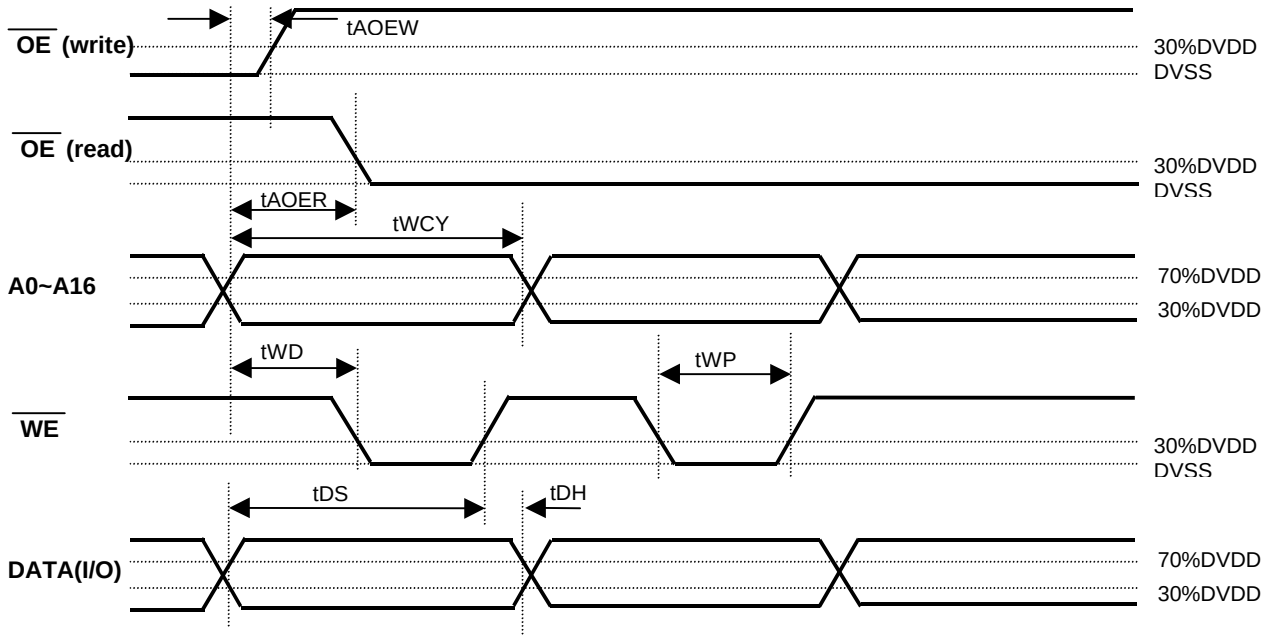
2) DBUS data less than 24 bits data output (in case of using SI)



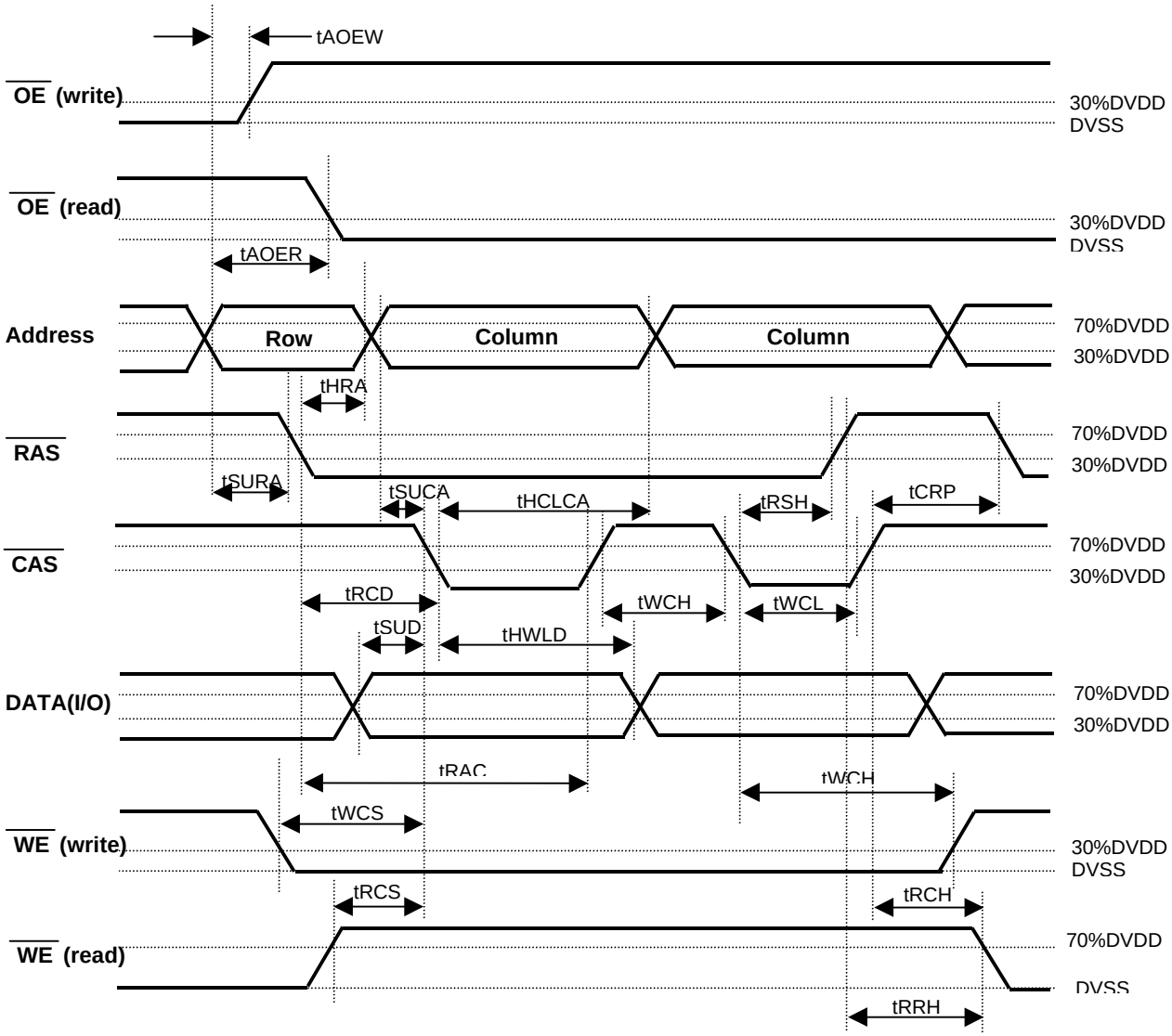
- AK7706 to Microcomputer (RAM DATA Read-out)



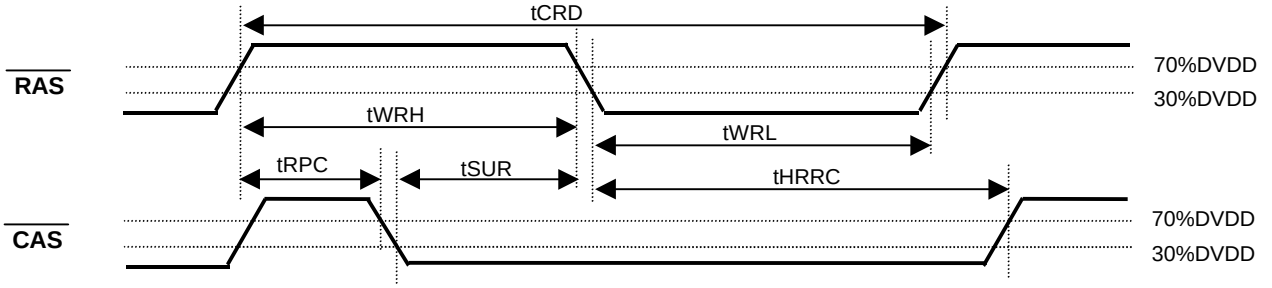
- AK7706 Read/Write Interface Timing of External SRAM



- AK7706 Read/Write Interface Timing of External DRAM



- AK7706 Refresh Interface Timing of External DRAM (CAS before RAS Refresh)



Function Description

(1) Various setting

1-1) CTRL (pin 13) : clock output control pins

CLKO will output a constant “L” or “H” by setting this pin to “L”.
When setting this pin to “H”, CLKO will output the frequency that is setting by control register.

1-2) SMODE (pin 21) : slave and master mode selector pin

Sets LRCLK (pin 10) and BITCLK (pin 11) to either inputs or outputs.
a) Slave mode :SMODE="L"
LRCLK(1fs) and BITCLK (64fs or 48fs) become inputs.
b) Master mode: SMODE="H"
LRCLK (1fs) and BITCLK (64fs). become outputs.

(2) Control registers

The control registers can be set via the microcomputer interface in addition to the control pins.
These registers are consisted by 4 parts and each register is 8-bit.
For the value to be written in the control registers see the description of the interface with microcomputer.
The following describes the control register map

TEST: for TEST (input 0,X: it ignore input data, but should input 0).

Command Code		Name	D7	D6	D5	D4	D3	D2	D1	D0	Default
Write	Read										
60h	70h	CONT0	CKS1	CKS0	DIF	DIF1	DIF0	DISCK	SELCKO	X	00h
64h	74h	CONT1	RAMCLR	RAMSEL1	RAMSEL0	PARSEL	ERAMAD	DATARAM	TEST	X	00h
68h	78h	CONT2	NON	NON	NON	DISOUT4	DISOUT3	NON	NON	X	00h
6Ch	7Ch	CONT3	NON	NON	NON	NON	DISOUT2	DISOUT1	MSET	X	00h

NON = does not use.

Data can be loaded into the control registers only when $\overline{\text{DSP RESET}}$ ="L". If used otherwise, on operation error will occur. Do not attempt to change any value in the control register when $\overline{\text{DSP RESET}}$ ="H".

CONT0 can be set only at system reset.

2-1) CONT0 : clock and interface selector

This register is enable only at system reset state ($\overline{\text{DSP\_RESET}}$ ="L").

Command Code		Name	D7	D6	D5	D4	D3	D2	D1	D0	Default
Write	Read										
60h	70h	CONT0	CKS1	CKS0	DIF	DIF1	DIF0	NON	SELCKO	X	00h

① **D7,D6: Master clock selector**

Mode	D7	D6	
1	0	0	512fs
2	0	1	384fs
3	1	0	TEST mode (Don't use).
4	1	1	256fs

Note) When fs=96kHz or 88.2kHz sampling mode, should be select Mode 4.

② **D5:DIF Audio interface selector**

0:AKM method

1: I^2S compatible (In this case, all input / output pins are I^2S compatible.)

③ D4,D3:DIF1,DIF0 SDIN1,SDIN2 Input mode selector

Mode	D4	D3	
1	0	0	MSB justified (24bit)
2	0	1	LSB justified (24bit)
3	1	0	LSB justified (20bit)
4	1	1	LSB justified (16bit)

Note) When D5= 1, the state is I^2S compatible independently of mode setting, however set to Mode 1.

④ **D2:Non use**

0: Normal Operation

⑤ **D1:SELCKO CLKO Output selector.**

0:CLKO outputs the same frequency as XTI.

1:CLKO outputs 1/2 frequency of XTI.

Note) In the case of select 1, after setting CONT0 (when the last clock of SCLK rise up) CLKO will change its frequency. So, the click noise comes out at this change.

Until $\overline{\text{INIT\_RESET}}$ changes to "L" or changes control register, the output frequency does not change.

Phase matching between CLKO and XTI is done at $\overline{\text{INIT\_RESET}}$ ="L".

⑥ **D0: Always 0**

Note) Underlines of the setting of ①~⑥mean default setting.

2-2) CONT1: RAM control

Command Code		Name	D7	D6	D5	D4	D3	D2	D1	D0	Default
Write	Read										
64h	74h	CONT1	RAMCLR	RAMSEL1	RAMSEL0	PARSEL	ERAMAD	DATARAM	TEST	X	00h

① **D7:RAMCLR Data reset and clear functions after RESET relese.**
0:Use (Normal setting)
1:Not use (for testing)

Normally, select 0. After release of system RESET ($\overline{\text{DSP RESET}}$ ="L", $\overline{\text{CODEC RESET}}$ ="L"), internal counter begins to start and it will issue a reset pulse near the rising point of 1fs clock (normally it is inverted LRCK phase).
In case of master mode, it is the rising point of the first LRCLK. In case of slave mode, it is 3rd LRCLK after release of the system RESET.
After the internal control circuit issues a reset pulse, the AK7716 will write all 0 data into all-internal RAM and external RAM. It takes 12,500LRCLK(max) whatever external RAM selected.
(LRCLK = 1/fs, fs=32kHz: 390ms fs=44.1kHz : 283ms , fs=48kHz : 260ms)

② **D6,D5:RAMSEL1,RAMSEL2 External RAM type selector.**

Mode	D6	D5	
1	0	0	SRAM 1Mbit
2	0	1	DRAM 1Mbit
3	1	0	DRAM 4Mbit
4	1	1	DRAM 16Mbit

③ **D4:PARASEL Parallel output selector**
0:Normal operation
1:Test mode
In the case of setting PARASEL=1, DBUS(Data bus) data outputs 24-bit to A16~A1 and IO7~IO0 (MSB first).

④ **D3:ERAMAD External RAM addressing mode selector**
0:Ring addressing mode
1:Linear addressing mode

⑤ **D2:DATARAM DATARAM addressing mode selector**
0:Ring addressing mode
1:Linear addressing mode
DATARAM has 256-word x 24-bit and has 2 addressing pointer (DP0, DP1).
The Ring addressing mode: Its start address increments 1 by every sampling time.
The Linear addressing mode: Its start address is always same, DP0 = 00h and DP1 = 80h.

⑥ **D1:TEST**
0:Normal operation. (Use at 0)
1: TEST mode.
This is an internal test mode and should not be used, please set this value to "0".

⑦ **D0: Input always 0**

Note) Underlines of the setting of ①~⑥ mean default setting.

2-3) CONT2 : Output control

Command Code		Name	D7	D6	D5	D4	D3	D2	D1	D0	Default
Write	Read										
68h	78h	CONT2	NON	NON	NON	DISOUT4	DISOUT3	NON	NON	X	00h

① **D7,D6,D5: Does not use.**
0:Normal operation (Use at 0)

② **D4: DISOUT4 SDOUT4 Disable select**
0:Normal operation
1: SDOUT4 pin outputs always “L” level.

③ **D3: DISOUT3 SDOUT3 Disable select**
0:Normal operation
1: SDOUT3 pin outputs always “L” level.

④ **D2, D1 Does not use.**
0:Normal operation

⑤ **D0: Always input 0**

Note) Underlines of the setting of ①~④ mean default setting.

2-4) CONT3: Other control

Command Code		Name	D7	D6	D5	D4	D3	D2	D1	D0	Default
Write	Read										
6Ch	7Ch	CONT3	NON	NON	NON	NON	DISOUT2	DISOUT1	MSET	X	00h

① **D7,D6,D5,D4: Does not use.**
0:Normal operation

② **D3:DISOUT2 SDOUT2 Disable**
0:Normal operation
1:SDOUT2 outputs always ”L” level.

③ **D2:DISOUT1 SDOUT1 Disable**
0:Normal operation
1:SDOUT1 outputs always ”L” level.

④ **D1:MSET Random number generator circuit selector**
0:Unused
1:Used
This DSP has a single feedback type shift-register [24,21,19,18,17,16,15,14,14,19,9,5,1] s independently from calculation block.
This register changes the data in every sampling time. And its output connected with DBUS, so in case of selected MSRG command at program code, then 24-bit random data will appear in every sampling.
In the case of using this random number generator, please set D1=1.

⑤ **D0: Always input 0**

Note) Underlines of the setting of ①~④ mean default setting.

(3) Power supply startup sequence

Turn on the power by setting to $\overline{\text{INIT RESET}}$ = "L", $\overline{\text{DSP RESET}}$ = "L".

Then the AK7706 is initialized by setting to $\overline{\text{INIT RESET}}$ = "H". Note 1)

Initialization by $\overline{\text{INIT RESET}}$ is sufficient if it is done only when the power is turned on.

Normally, $\overline{\text{INIT\_RESET}}$ setting is only done at turn on power.

Note 1): Set to $\overline{\text{INIT RESET}}$ = "H" after setting the oscillation when a crystal oscillator is used.

This setting time may differ depending on the crystal oscillator and its external circuit.

NOTE: Do not stop the system clock (slave mode: XTI, LRCLK, BITCLK, master mode: XTI) except when $\overline{\text{INIT RESET}}$ = "L".

If these clock signals are not supplied, excess current will flow due to dynamic logic that is used internally, and an operation failure may result.

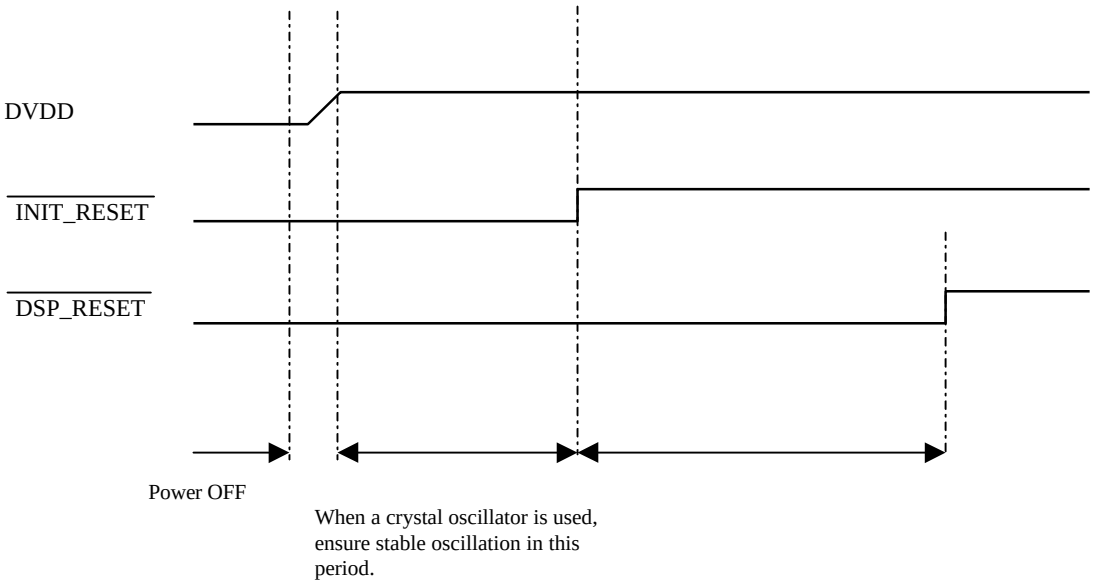


Fig. Power supply startup sequence

(4) Resetting

The AK7706 has two reset pins: $\overline{\text{INIT RESET}}$ and $\overline{\text{DSP RESET}}$.

The $\overline{\text{INIT RESET}}$ pin is used to initialize the AK7706, as shown in "Power supply startup sequence section 3)."

The system is reset when $\overline{\text{DSP RESET}}$ = "L" and $\overline{\text{CODEC RESET}}$ = "L". (Description of "reset" is for "system reset".)

Under the condition of system reset, the program write operation is normally performed (except for write operation during running). CLKO is output even during the system reset phase if CTRL = “L”, but LRCLK and BITCLK in the master mode will be inactive.

The system reset is released by setting $\overline{\text{DSP RESET}}$ to "H", and this will activate the internal counter. This counter generates LRCLK and BITCLK in the master mode: however, a hazard may occur when a clock signal is generated. When the system reset is released in the slave mode, internal timing will be actuated in synchronization with "↑" of LRCLK (when the standard input format is used). Timing between the external and internal clocks is adjusted at this time. If the phase difference in LRCLK and internal timing is within about -1/16 to 1/16 of the input sampling cycle (1/fs) during the operation, the operation is performed with internal timing remaining unchanged. If the phase difference exceeds the above range, the phase is adjusted by synchronization with "↑" of LRCLK (when the standard input format is used). This is a circuit to prevent failure of synchronization with the external circuit. For some time after returning to the normal state after loss of synchronization, normal data will not be valid. If you want to change the clock, do so while the system is in reset.

When $\overline{\text{DSP RESET}}$ is set to “H”, the reset state is cancelled, and the external RAM clear (“0” data writes) and the internal DRAM clear are executed from the rising edge of LRCLK. This period takes 12400 * 1/fs [sec] at 512fs mode and 16540 * 1/fs [sec] at 384fs mode. (fs : sampling frequency). After this “data reset function”, the function of [7-3) Write during RUN phase] is acceptable.

The AK7706 performs normal operation when both $\overline{\text{DSP RESET}}$ is set to "H".

After the internal control circuit issues a reset pulse, the AK7716 will write all 0 data into all-internal RAM and external RAM.
It takes 12,500LRCLK(max) whatever external RAM selected. (LRCLK = 1/fs, fs=44.1kHz : 283ms , fs=48kHz : 260ms) See.2-2)-①

(5) System clock

The required system clock is XTI (256 fs/384 fs/512 fs), LRCLK (fs) and BITCLK (64 fs or 48fs) in the slave mode, and is XTI (256 fs/384 fs/512 fs) in the master mode.
LRCLK corresponds to the standard digital audio rate (32 kHz, 44.1 kHz, 48 kHz, 88.2kHz, 96kHz).

Fs	XTI (Master clock)			BITCLK
	256fs	384fs	512fs	64fs
32.0kHz	Can not use	12.2880MHz	16.3840MHz	2.0480MHz
44.1kHz	11.2896MHz	16.9344MHz	22.5792MHz	2.8224MHz
48.0kHz	12.2880MHz	18.4320MHz	24.576MHz	3.0720MHz
88.2kHz	22.5792MHz	Can not use	Can not use	5.6448MHz
96.0kHz	24.5760MHz	Can not use	Can not use	6.1440MHz

5-1) Master clock (XTI pin)

The master clock is obtained by connecting a crystal oscillator between the XTI pin and XTO pin or by inputting an external clock into the XTI pin while the XTO pin is left open.

5-2) Slave mode

The required system clock is XTI (256 fs/384 fs/512 fs), LRCLK (1 fs) and BITCLK (48/64 fs).
The master clock (XTI) and LRCLK must be synchronized, but the phase is not critical.

5-3) Master mode

The required system clock is XTI (256 fs/384 fs/512 fs). When the master clock (XTI) is input, LRCLK (1 fs) and BITCLK (64 fs) will be outputted from the internal counter synchronized with the XTI.

LRCLK and BITCLK will not be active during initial reset ($\overline{\text{INIT RESET}}$ = "L") and system reset ($\overline{\text{DSP RESET}}$ = "L").

(6) Audio data interface (internal connection mode)

The serial audio data pins SDIN1, SDIN2 ,SDIN3, SDOUT1, SDOUT2, SDOUT3 and SDOUT4 are interfaced with the external system, using LRCLK and BITCLK. The data format is MSB-first 2's complement. Normally, the input/output format, in addition to the standard format used by AKM, can be changed to the I^2S compatible mode by setting the control register "CONT0 DIF(D5) to 1". (In this case, all input/output audio data pin interface are in the I^2S compatible mode.)

The input SDIN1,SDIN2 and SDIN3 formats are MSB justified 24-bit at initialization. Setting the control registers CONT0: DIF1, DIF0 will cause them to be compatible with LSB justified 24-bit, 20-bit and 16-bit.

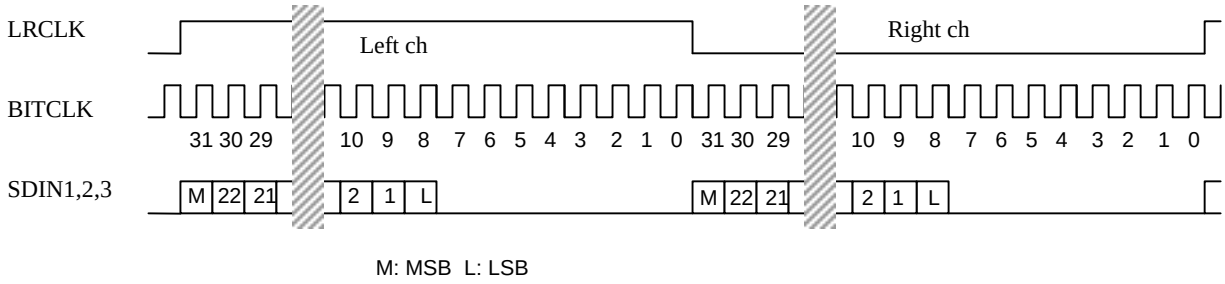
However, inidividul setting of SDIN1, SDIN2 and SDIN3 is not allowed.

The output SDOUT1, SDOUT2, SDOUT3 and SDOUT4 are fixed at 24 bits MSB justified.

At slave mode BITCLK corresponds to not only 64fs but also 48fs. But, we recommend 64fs. Following formats describe 64fs examples.

6-1) Standard input format (DIF = 0: default set value)

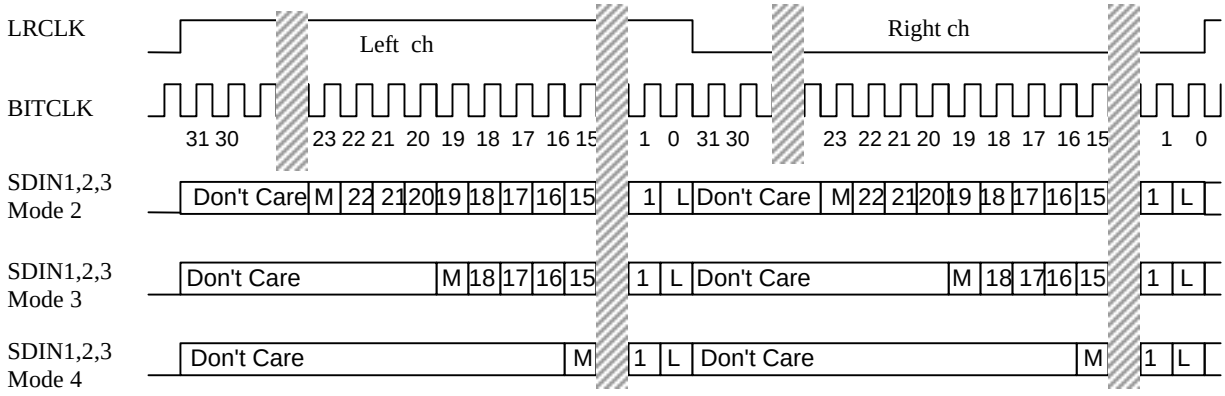
a) Mode 1 (DIF1, DIF0 = 0,0: default set value)



M: MSB L: LSB

* When you want to input the MSB-justified 20-bit data into SDIN1,2 and 3, input four "0s" following the LSB.

b) Mode 2, Mode 3, Mode 4



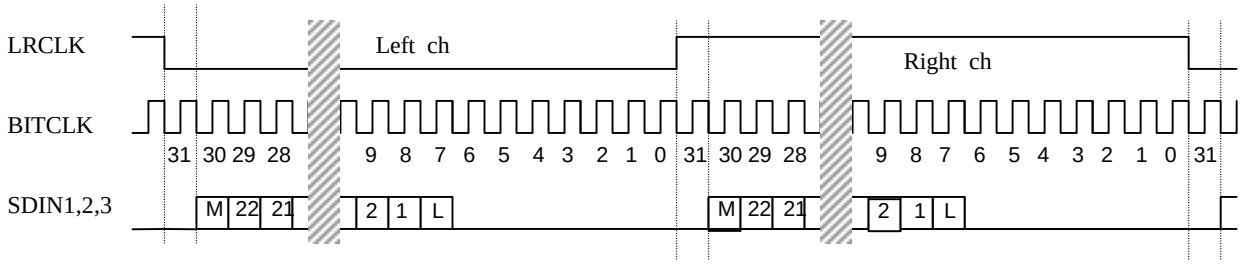
M: MSB , L : LSB

SDIN1,2,3 Mode 2: (DIF1, DIF0) = (0, 1) LSB justified 24-bit

SDIN1,2,3 Mode 3: (DIF1, DIF0) = (1, 0) LSB justified 20-bit.

SDIN1,2,3 Mode 4: (DIF1, DIF0) = (1, 1) LSB justified 16-bit

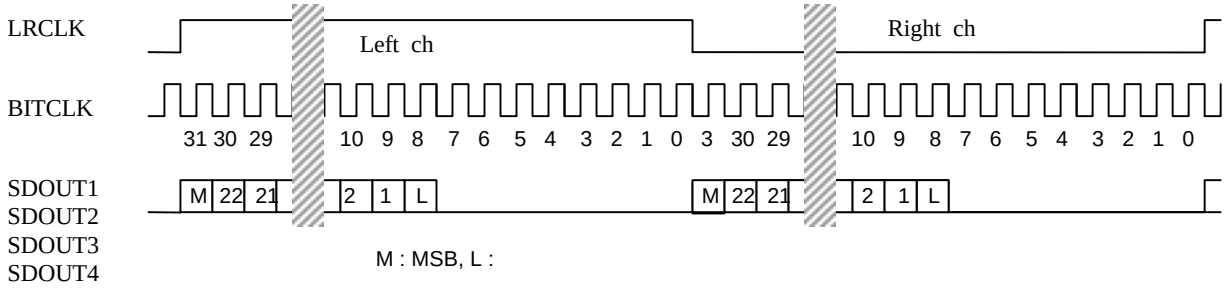
6-2) I²S compatible input format (DIF=1)



M : MSB, L : LSB

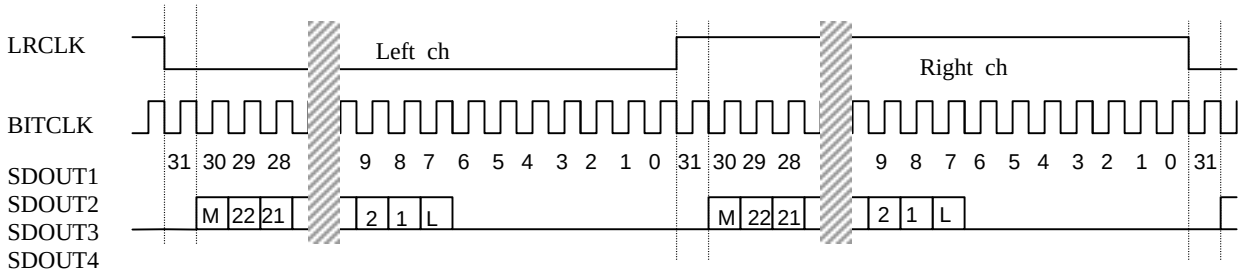
Mode 1: (DIF1, DIF0) = (0, 0) must be set.

6-3) Standard output format (DIF=0: default set value)



M : MSB, L :

6-4) I²S compatible output format (DIF=1)



M : MSB , L : LSB

(7) Interface with microcomputer

The interface to a microcomputer is provided by 6 control signals; $\overline{CS}$ (Chip Select Bar), $\overline{RQ}$ (ReQuest Bar), SCLK (Serial data input CLocK), SI (Serial data Input), SO (Serial data Output), RDY (ReaDY) and DRDY (Data ReaDY).
In the AK7706, two types of operations are provided; writing and reading during the reset phase (namely, system reset) and those during the run phase. During the reset phase, writing of the control register, program RAM, coefficient RAM, offset RAM, external conditional jump code, and reading of the program RAM, coefficient RAM and offset RAM, are enabled. During the run phase, writing of coefficient RAM, offset RAM and external conditional jump code, and reading of data on the DBUS (data bus) from the SO, are enabled.

When the AK7706 needs to transfer data to the microcomputer, it starts by $\overline{RQ}$ going "L".

The AK7706 reads SI data at the rising point of SCLK, and outputs to SO at the falling point of SCLK.
The AK7706 accepts first data as command then address data or some kinds of data input / output starts.

When $\overline{RQ}$ changes to "H", then one command is finished. So, new command requests needs to set $\overline{RQ}$ to "L" again.

When the DBUS data read, leave $\overline{RQ}$ ="H". (It does not need command code input."

When it needs to clear the output buffer (MICR), the SI pin uses for control. In this case, it is necessary to protect against a noise as SCLK.
Command code table is as follow.

Command code list

Conditions for use	Code name	Command code		Note:
		WRITE	READ	
RESET phase	CONT0	60h	70h	For the function of each bit, See the description of Control Registers.
	CONT1	64h	74h	
	CONT2	68h	78h	
	CONT3	6Ch	7Ch	
	PRAM	C0h	C1h	
	CRAM	A0h	A1h	
	OFRAM	90h	91h	
	External condition jump	C4h	-	
RUN phase	CRAM rewrite preparation	A8h	-	It needs to do before CRAM rewrite.
	CRAM rewrite	A4h	-	
	OFRAM rewrite preparation	98h	-	It needs to do before OFRAM rewite.
	OFRAM rewrite	94h	-	
	External condition jump	C4h	-	Same command as RESET

NOTE: Do not send other than the above command codes. Otherwise, operation error may occur.
If there is no communication with the microcomputer, set the SCLK to "H" and the SI to "L" for use.

7-1) Write during reset phase

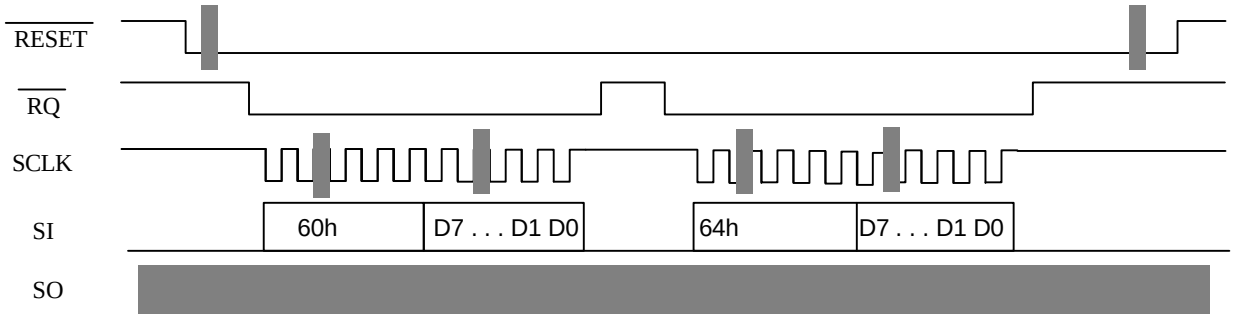
7-1-a) Control register write (during reset phase)

The data comprises a set of 2 bytes those are used to perform control register write operations (during reset phase). When all data has been entered. The new data is sent at the rising point of 16 count of SCLK.

Data transfer procedure

① Command code	60h,64h,68h,6Ch
② Control data	(D7 D6 D5 D4 D3 D2 D1 D0)

For the function of each bit, see the description of Control registers, see section 2).



Control registers write operation

Note) It must be set always 0 to D0.

7-1-b) Program RAM write (during reset phase)

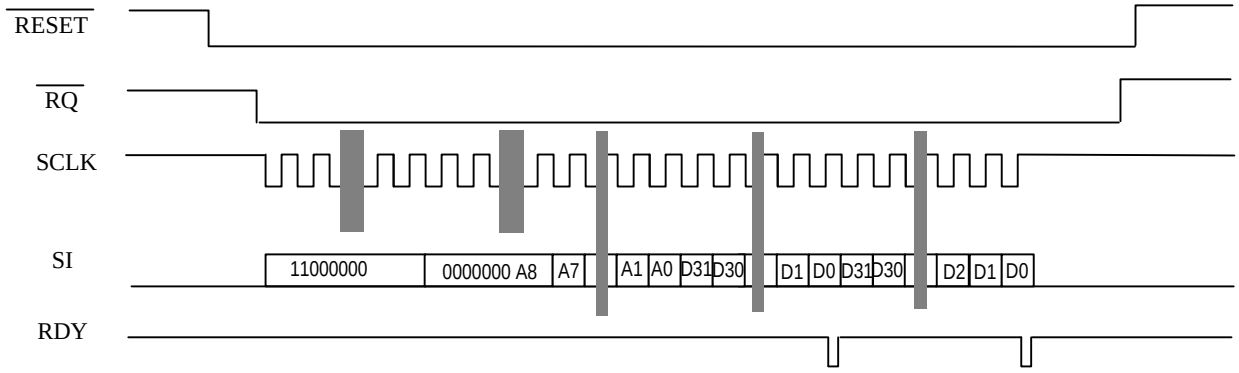
Program RAM write operation is performed during the reset phase according to the data comprising a set of 7 bytes. When all data have been transferred, the RDY terminal is set to "L". Upon completion of writing into the PRAM, RDY returns “H” to allow the next data bitinput. When data of continuous addresses are written, input the data as they are. (No command code or address is required.)

To write discontinuous data, shift the $\overline{RQ}$ terminal from "H" to "L" again. Then input the command code, address and data in that order.

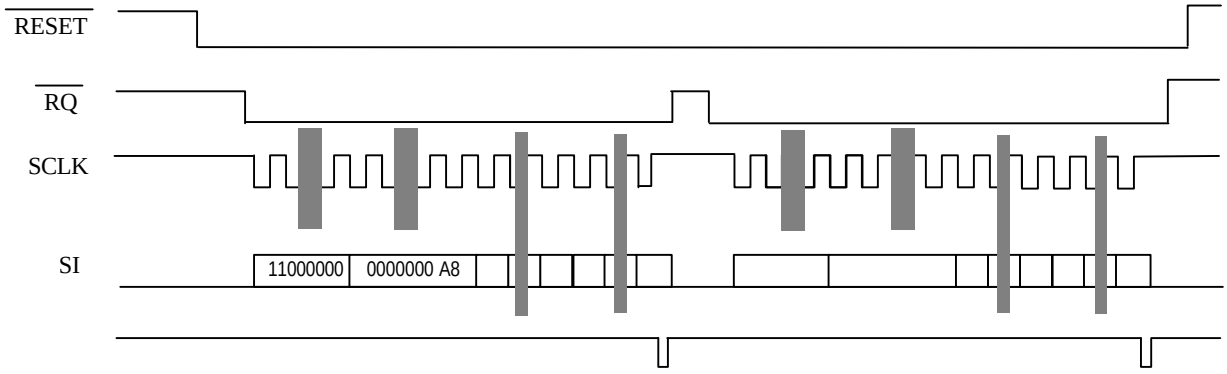
($\overline{RESET}$ means $\overline{DSP\ RESET}$)

Data transfer procedure

① Command code	C0h (1 1 0 0 0 0 0 0)
② Address upper	(0 0 0 0 0 0 0 A8)
③ Address lower	(A7 . . . . . A0)
④ Data	(D31 . . . . . D24)
⑤ Data	(D23 . . . . . D16)
⑥ Data	(D15 . . . . . D8)
⑦ Data	(D7 . . . . . D0)



Input of continuous address data into PRAM



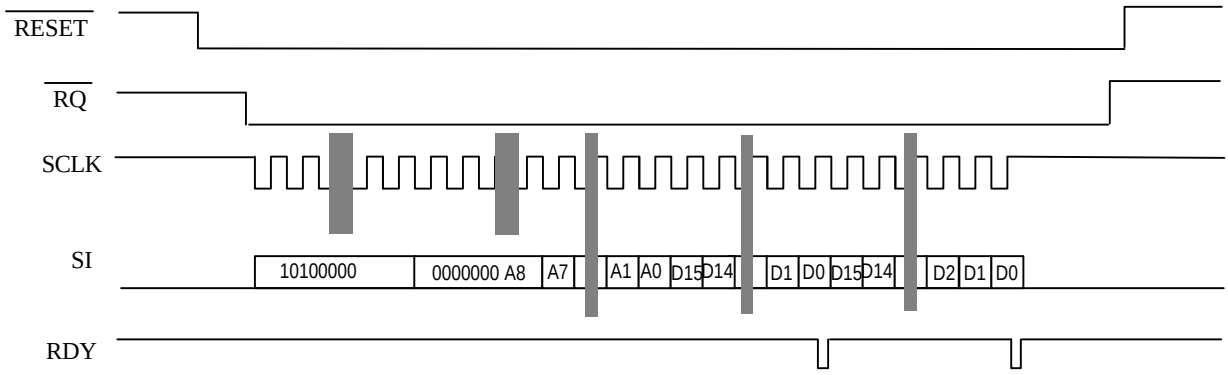
Input of discontinuous address data into PRAM

7-1-c) Coefficient RAM write (during reset phase)

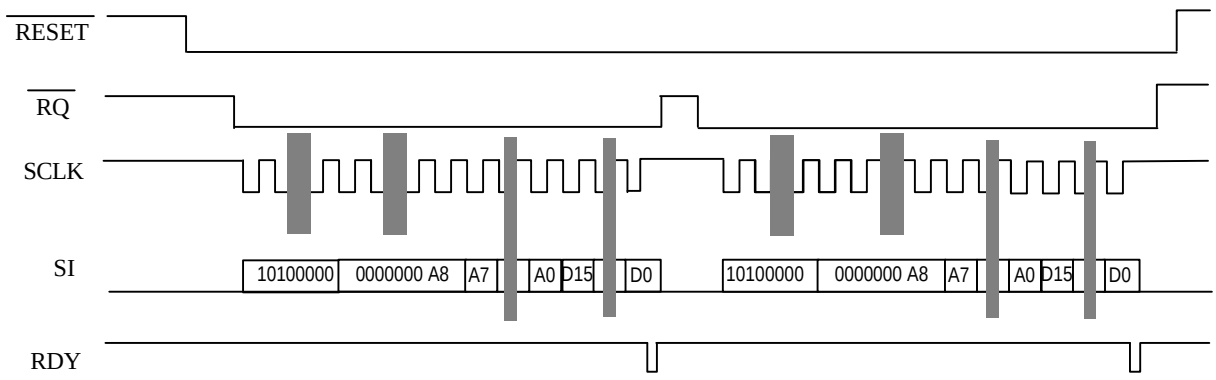
The data comprising a set of 5 bytes is used to perform coefficient RAM write operations (during reset phase). When all data has been transferred, the RDY terminal goes to "H". Upon completion of writing into the CRAM, it goes to "H" to allow the next data to be inputed. When data of continuous addresses are written, input the data as they are. To write discontinuous data, shift the $\overline{RQ}$ terminal from "H" to "L". Then input the command code, address and data in that order.
($\overline{RESET}$ means $\overline{DSP\ RESET}$)

Data transfer procedure

① Command code	A0h (1 0 1 0 0 0 0 0)
② Address upper	(0 0 0 0 0 0 0 A8)
③ Address lower	(A7 . . . . . A0)
④ Data	(D15 . . . . . D8)
⑤ Data	(D7 . . . . . D0)



Input of continuous address data into CRAM



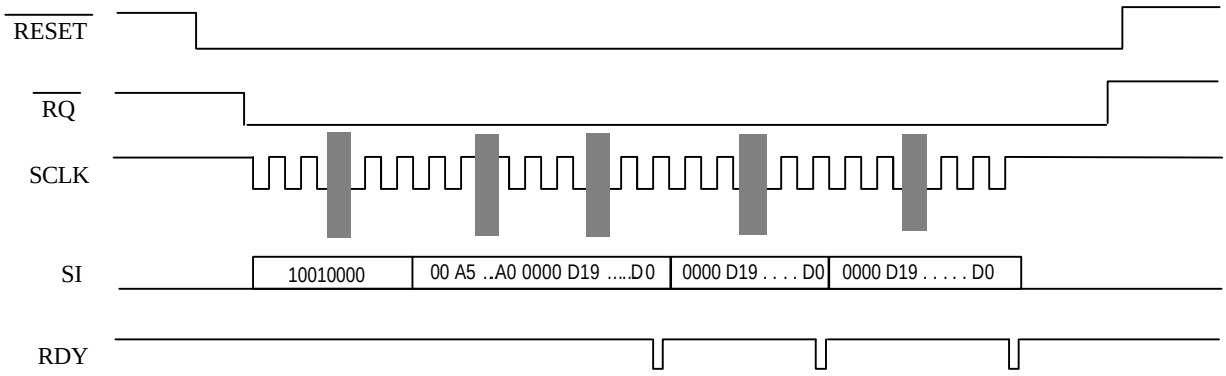
Input of discontinuous address data into CRAM

7-1-d) Offset RAM write (during reset phase)

The data comprising a set of 5 bytes is used to perform offset RAM write operations (during reset phase). When all data has been transferred, the RDY terminal goes to "H". Upon completion of writing into the OFRAM, it goes to "H" to allow the next data to be input. When data of continuous addresses are written, input the data as they are. To write discontinuous data, shift the $\overline{RQ}$ terminal from "H" to "L". Then input the command code, address and data in that order.
($\overline{RESET}$ means $\overline{DSP\ RESET}$)

Data transfer procedure

① Command code	90h	(1 0 0 0 1 0 0 0 0)
② Address		(0 0 A5 A4 . . . . A0)
③ Data		(0 0 0 0 D19 . . . D16)
④ Data		(D15 . . . . . D8)
⑤ Data		(D7 . . . . . D0)

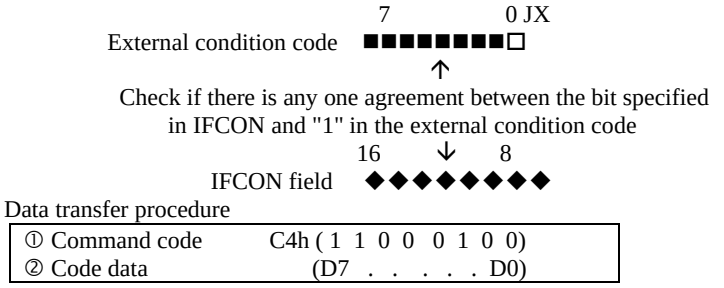


Input of data into OFRAM

7-1-e) External conditional jump code write (during reset phase)

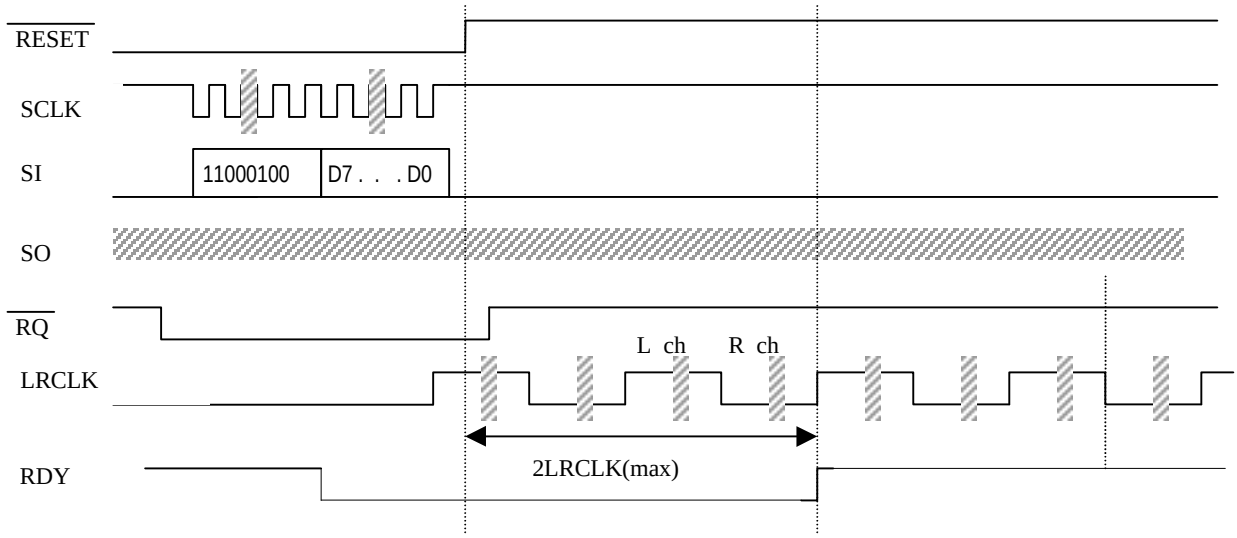
The data comprising a set of two bytes is used to perform an external conditional jump code write operation. The data can be inputed during both the reset and operation phases, and the input data are set to the specified register at the leading edge of the LRCLK. When all data bits have been transferred, the RDY terminal goes to "L". Upon completion of writing, it goes to "H". A jump command will be executed if there is any one agreement between "1" of each bit of external condition code 8 bits (soft set) plus 1 bit (hard set) at the external input terminal JX and "1" of each bit of the IFCON field. The data during the reset phase can be written only before release of the reset, after all data has been transferred. $\overline{RQ}$ Transition from "L" to "H" in the write operation during the reset phase must be execured after three LRCLK in the slave mode, one LRCLK in master mode, respectively, from the trailing edge of the LRCLK after release of the reset. Then the RDY goes to "H" after capturing the rise of the next LRCLK. A write operation from the microcomputer is disabled until the RDY goes to "H". The IFCON field provides external conditions written on the program.

Note: It should be noted that the LRCLK phase is inverted in the I2S-compatible state.



Data transfer procedure

① Command code	C4h (1 1 0 0 0 1 0 0)
② Code data	(D7 . . . . . D0)



Timing for external conditional jump write operation (during reset phase)

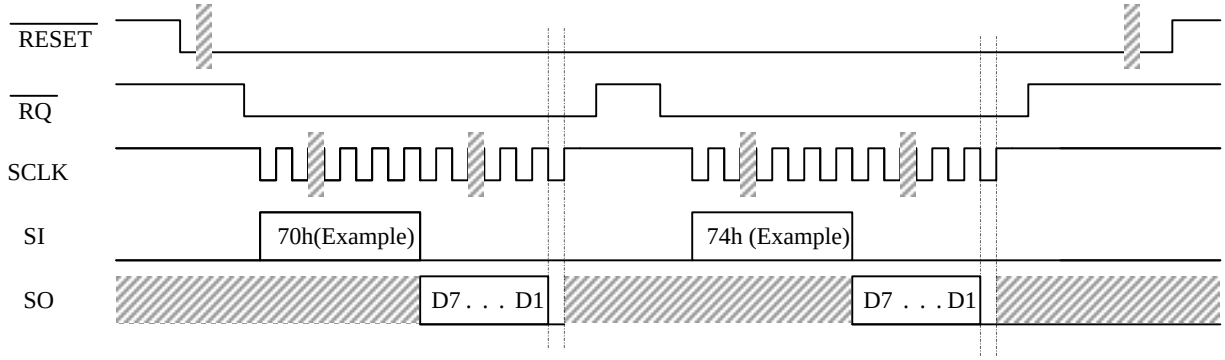
7-2) Read during reset phase

7-2-a) Control register data read (during reset phase)

To read data written into the control registers, input the command code and 16 bits of SCLK. After input command code, the data of D7 to D1 outputs from SO in synchronization with the falling edge of SCLK. D0 is invalid, so please ignore this bit.

Data transfer procedure

① Command code 70h,74h,78h,7Ch



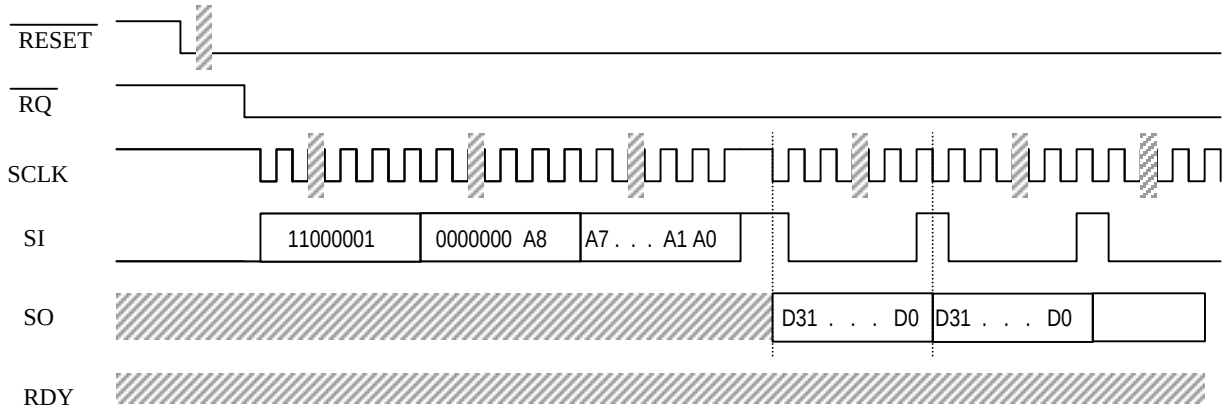
Reading of Control Register data

7-2-b) Program RAM read (during reset phase)

To read data written into PRAM, input the command code and the address you want to read out. After that, set SI to "H" and SCLK to "L". Then the data is clocked out from SO in synchronization with the falling edge of SCLK. (Ignore the RDY operation that will occur in this case.)
If there are continuous addresses to be read, repeat the above procedure starting from the step where SI is set to "H".

Data transfer procedure

①Command code input	C1h (1 1 0 0 0 0 0 1)
②Read address input	(0 0 0 0 0 0 0 A8)
	(A7 . . . . A0)



Reading of PRAM data

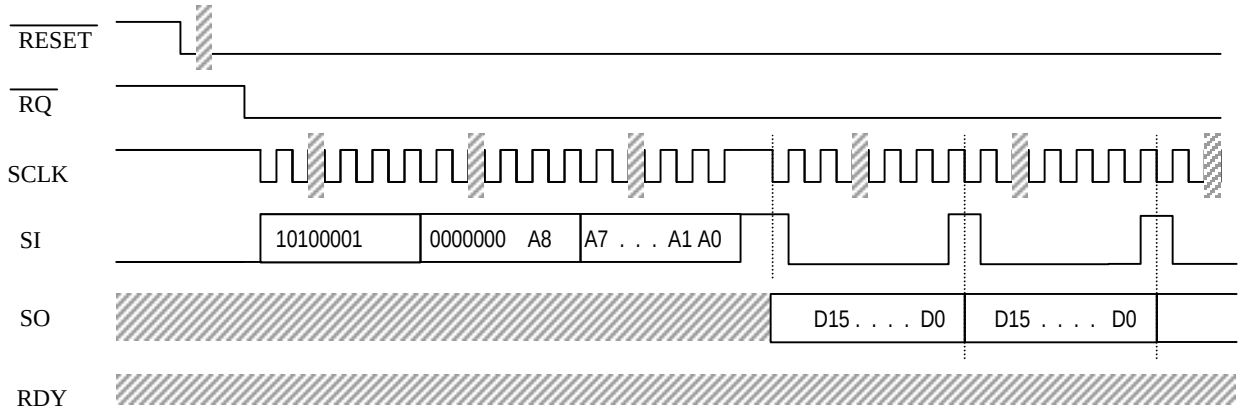
7-2-c) CRAM data read (during reset phase)

To read out the written coefficient data, input the command code and the address you want to read out. After that, set SI to "H" and SCLK to "L". Then, the data is clocked out from SO in synchronization with the falling edge of SCLK.
If there are continuous addresses to be read, repeat the above procedure starting from the step where SI is set to "H".

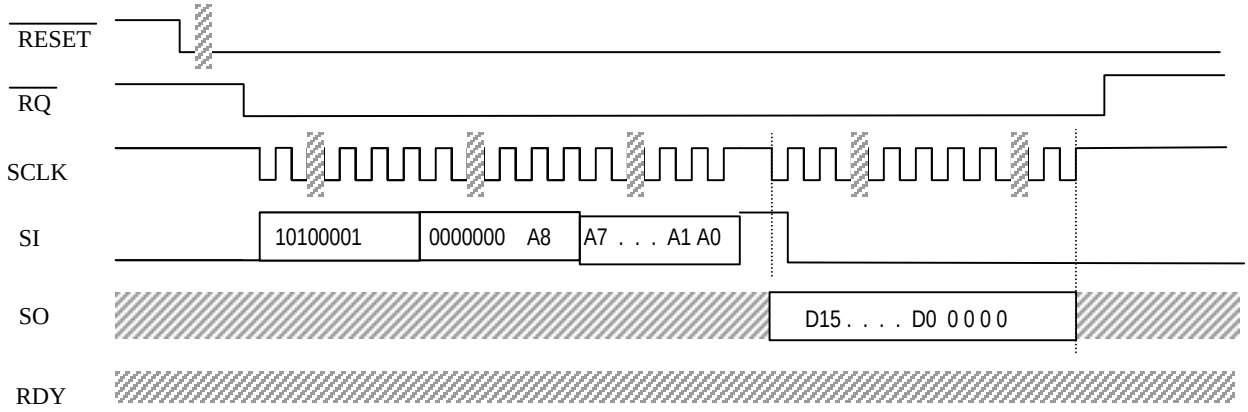
Note: This method should be read more than two data.
But, if it needs to read only one data, then it should be input more than 20-bit SCLK and ignore LSB 4-bit.

Data transfer procedure

① Command code A1h	(1 0 1 0 0 0 0 1)
② Address upper	(0 . . . . . A8)
③ Address lower	(A7 . . . . . A0)



Reading of CRAM data (more than 2 data)



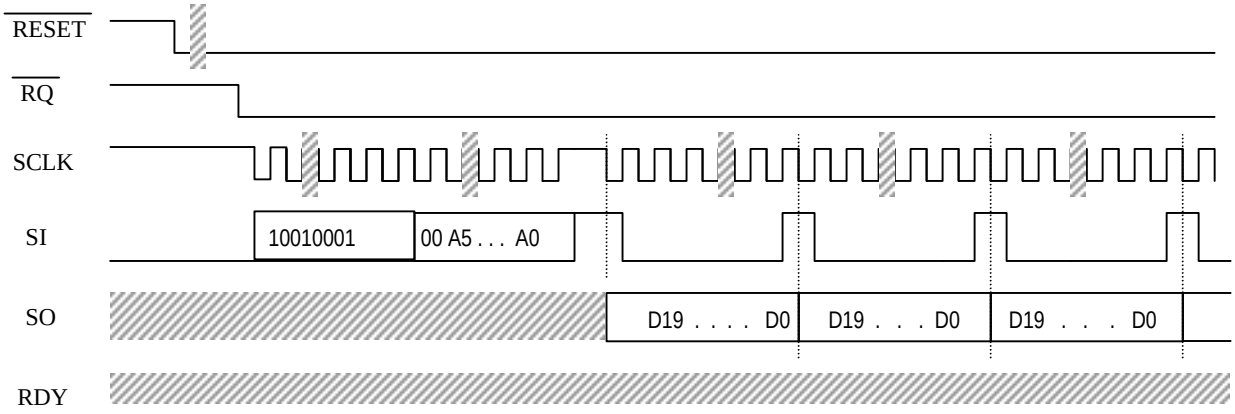
Reading of CRAM data (1 data only)

7-2-d) OFRAM data read (during reset phase)

The written offset data can be read out during the reset phase. To read it, input the command code and the address you want to read. After that, set SI to "H" and SCLK to "L". This completes preparation for outputting the data. Then set SI to "L", and the data is clocked out in synchronization with the falling edge of SCLK. If there are continuous addresses to be read, repeat the above procedure starting from the step where SI is set to “H”.

Data transfer procedure

① Command code	91h (1 0 0 0 1 0 0 0 1)
② Address	(0 0 A5 . . . . A0)



Reading of OFRAM data

7-3) Write during RUN phase

7-3-a) CRAM rewrite preparation and write (during RUN phase)

This function is used to rewrite CRAM (coefficient RAM) during the program execution. After inputting the command code, you can input a maximum of 16 data bytes of a continuous address you want to rewrite.
Then input the write command code and rewrite the leading address. Every time the RAM address to be rewritten is specified, the contents of RAM are rewritten. The following is an example to show how five data bytes from address "10" of the coefficient RAM are rewritten:

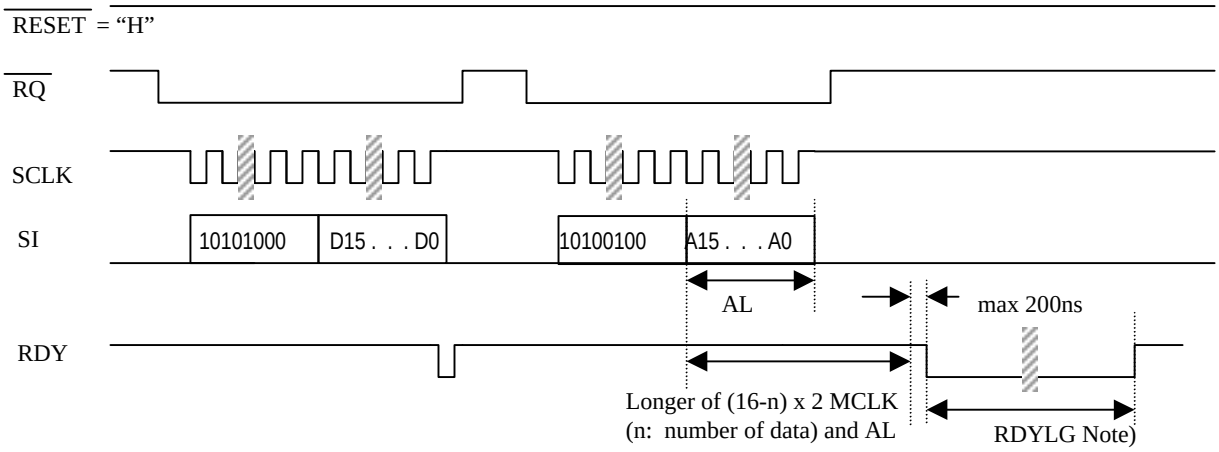
Coefficient RAM execution address 7 8 9 10 11 13 16 11 12 13 14 15

Rewrite position ↓ ↓ ↑ ↓ ↓ ↓

Note that address "13" is not executed until address "12" is rewritten.

Data transfer procedure

* Preparation for rewrite	① Command code	A8h (1 0 1 0 1 0 0 0)
	② Data	(D15 . . . . D8)
	③ Data	(D7 . . . . . D0)
* Rewrite	① Command code	A4h (1 0 1 0 0 1 0 0)
	② Address upper	(0 0 0 0 0 0 0 A8)
	③ Address lower	(A7 . . . . A0)



Note: The RDY signal will go to high within the maximum of two LRCLKs if the RDYLG width is programmed to ensure a new address to be rewritten within one sampling cycle.

CRAM rewriting preparation and writing

7-3-b) OFRAM rewrite preparation and write (during RUN phase)

This function is used to rewrite OFRAM (offset RAM) during program execution. After inputting the command code, you can input a maximum of 16 data bytes of a continuous address you want to rewrite.
Then input the write command code and rewrite the leading address. Every time the RAM address to be rewritten is specified, the contents of RAM are rewritten. The following is an example to show how five data bytes from address "10" of the coefficient RAM are rewritten:

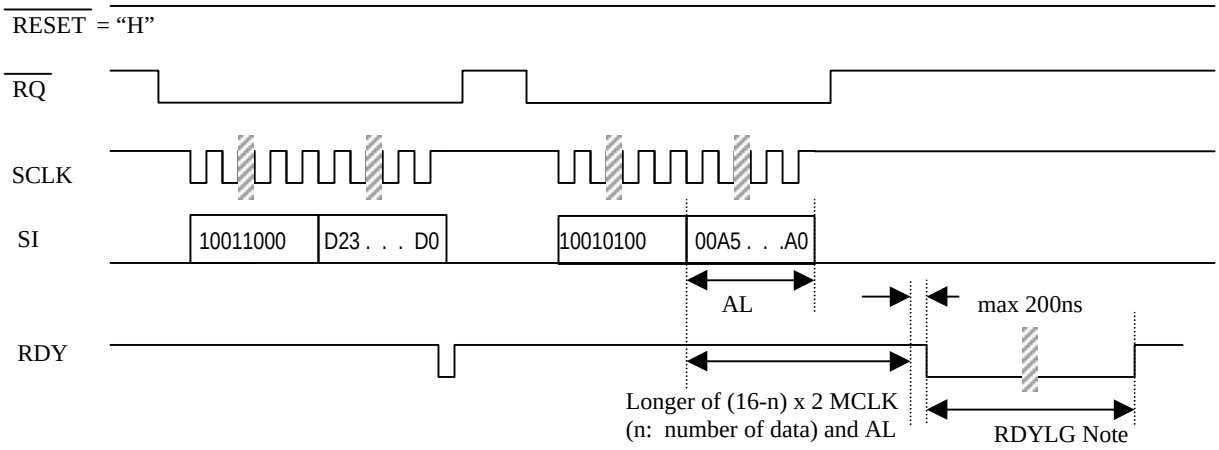
Offset RAM execution address 7 8 9 10 11 13 16 11 12 13 14 15

Rewrite position ↓ ↓ ↑ ↓ ↓ ↓
o o o o o

Note that address "13" is not executed until address "12" is rewritten.

Data transfer procedure

* Preparation for rewrite	① Command code	98h (1 0 0 0 1 1 0 0 0)
	② Data	(D23 . . . . . . D16)
	③ Data	(D15 . . . . . . D8)
	④ Data	(D7 . . . . . . D0)
* Rewrite	① Command code	94h (1 0 0 0 1 0 1 0 0)
	② Address	(0 0 A5A4 . . . A0)



Note: The RDY signal will go to high within the maximum of two LRCLKs if the RDYLG width is programmed to ensure a new address to be rewritten within one sampling cycle.

OFRAM rewriting preparation and writing

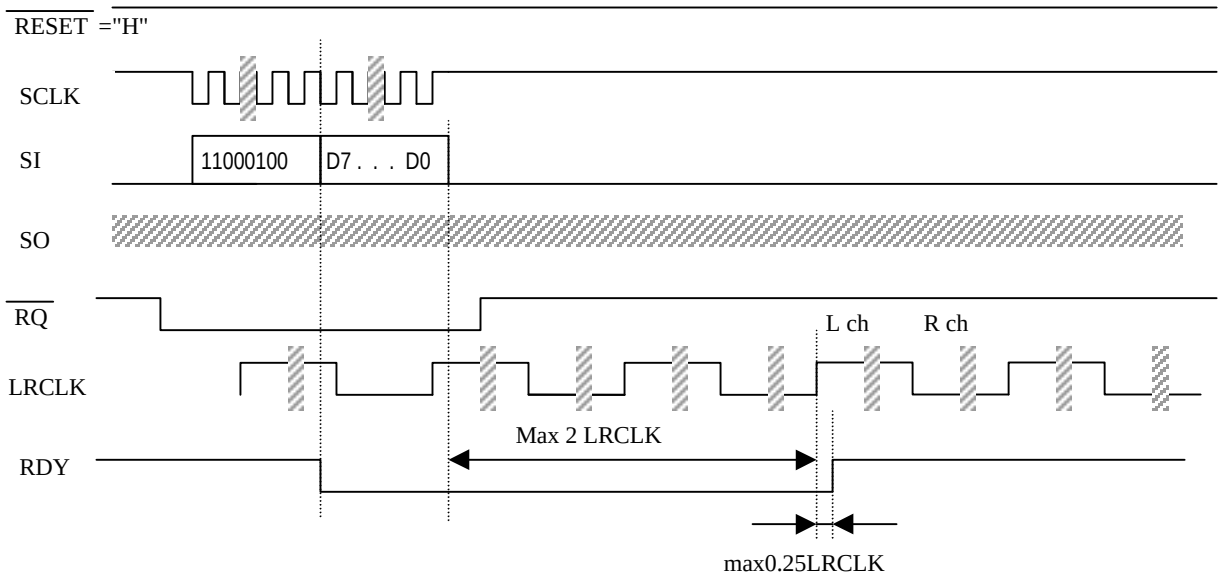
7-3-c) External conditional jump code rewrite (during RUN phase)

Data comprising a set of two bytes is used to write the external conditional jump code. Data can be input during both the reset and operation phases, and input data is set to the specified register at the rising edge of LRCLK. When all data has been transferred, the RDY terminal goes to "L". Upon completion of writing, it goes to "H". A jump command will be executed if there is any one agreement between each bit of the 8-bit external condition code and "1"of each bit of the IFCON field. A write operation from the microcomputer is disabled until RDY goes to "H".

Note: The LRCLK phase is inverted in the I2S-compatible state.

Data transfer procedure

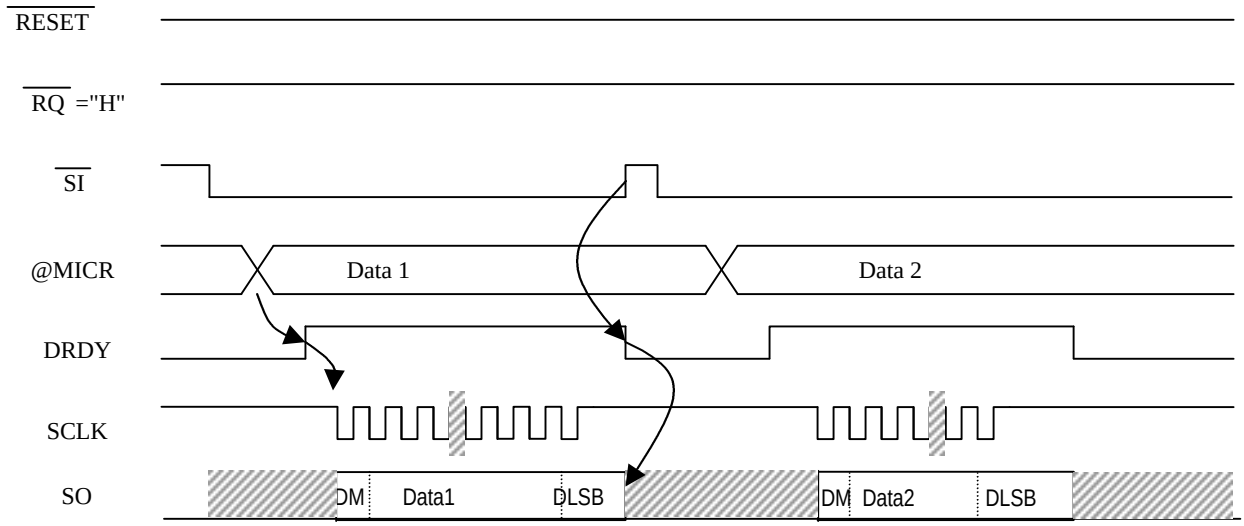
① Command code	C4h (1 1 0 0 0 1 0 0)
② Code data	(D7 . . . . . D0)



External condition jump write timing (during RUN phase)

7-4) Read-out during RUN phase (SO output)

SO outputs data on DBUS (data bus) of the DSP section. Data is set when @MICR the DST field specifies. Setting of data allows DRDY to go to "H", and data is output synchronized with the falling edge of SCLK. When $\overline{CS}$ goes to "H", DRDY goes to "L" to wait for the next command. Once DRDY goes to "H", the data of the last @MICR command immediately before DRDY goes to "H" will be held until $\overline{CS}$ goes to "H", and subsequent commands will be rejected.
A maximum of 24 bits are output from SO. After the required number of data (not exceeding 24 bits) is taken out by SCLK, the next data can be output by setting $\overline{CS}$ to "H".

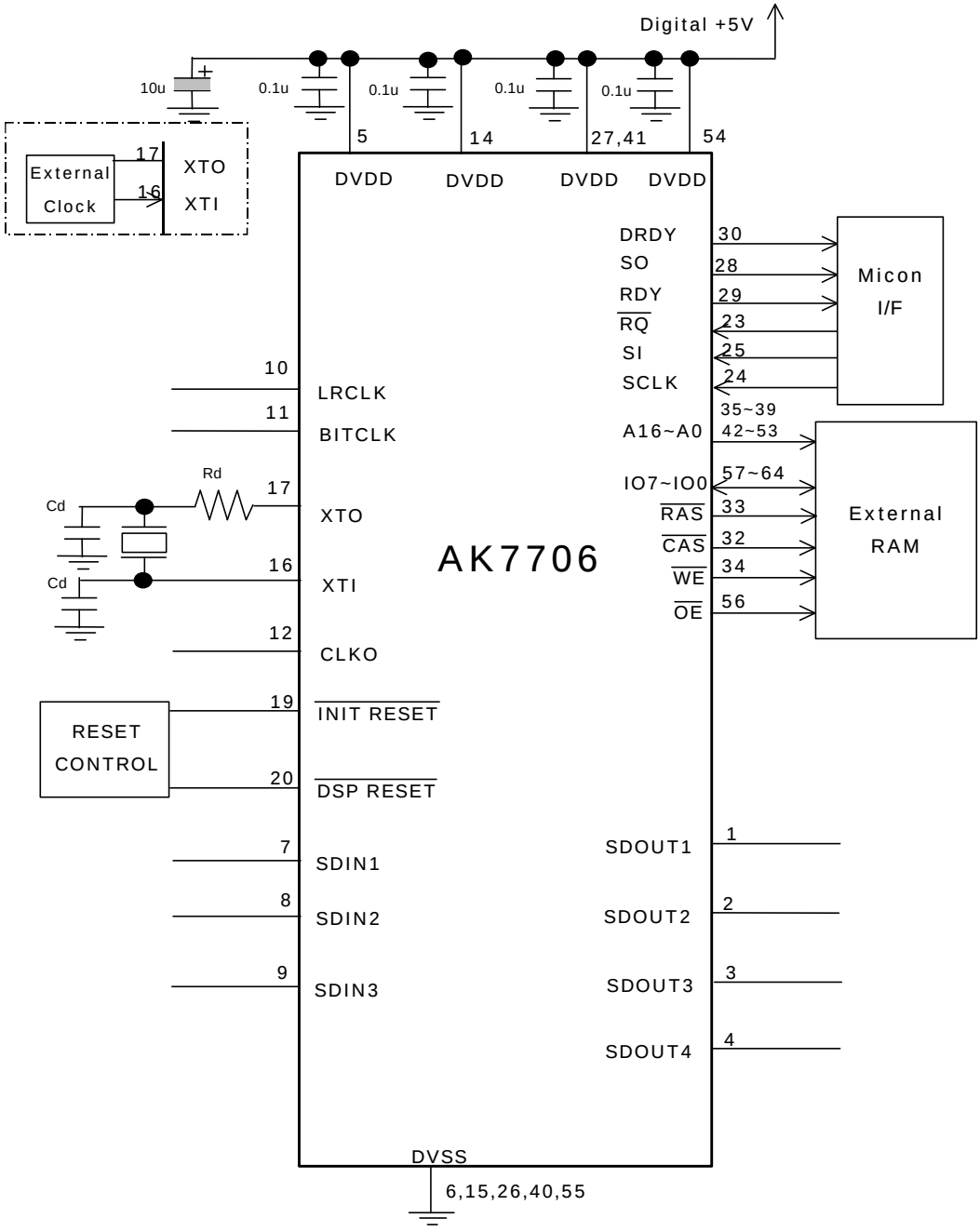


SO read (during RUN phase)

System Design

8-1) Example circuit (Internal connected mode OPCL : "L")

See (8-2) Peripheral circuit also.

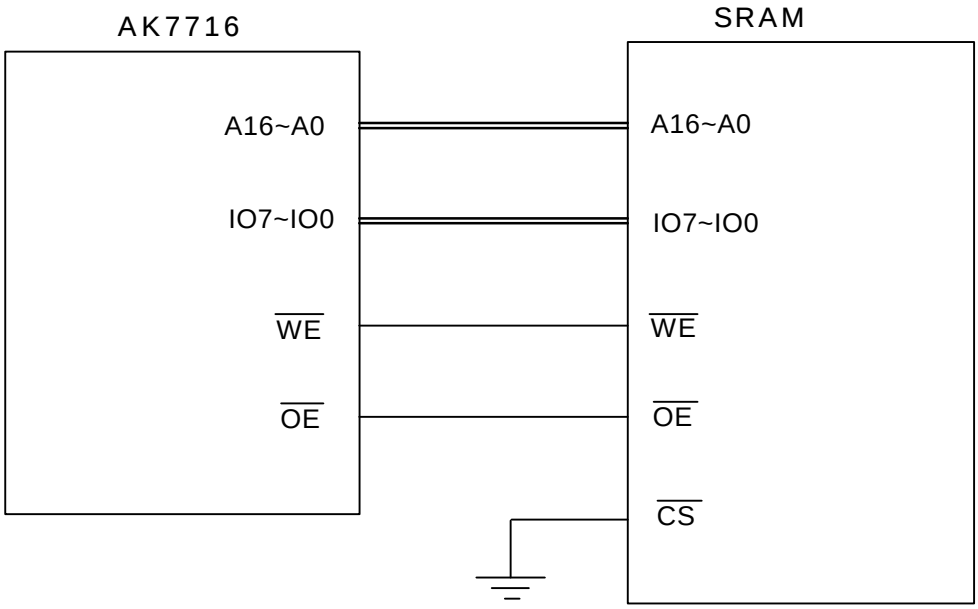


8-2) Peripheral circuit

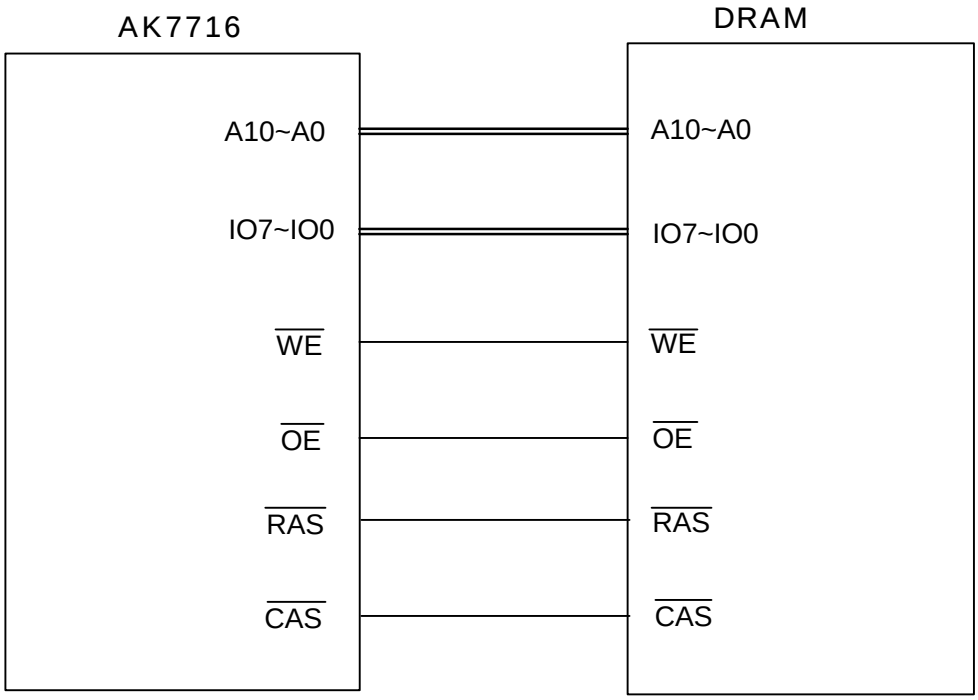
8-2-1) Connect with external RAM

The connections to external RAM (SRAM or DRAM) are as follows. It should be as short as possible to connect line.
Leave open, if it does not use external RAM.

① **SRAM**



② **DRAM**

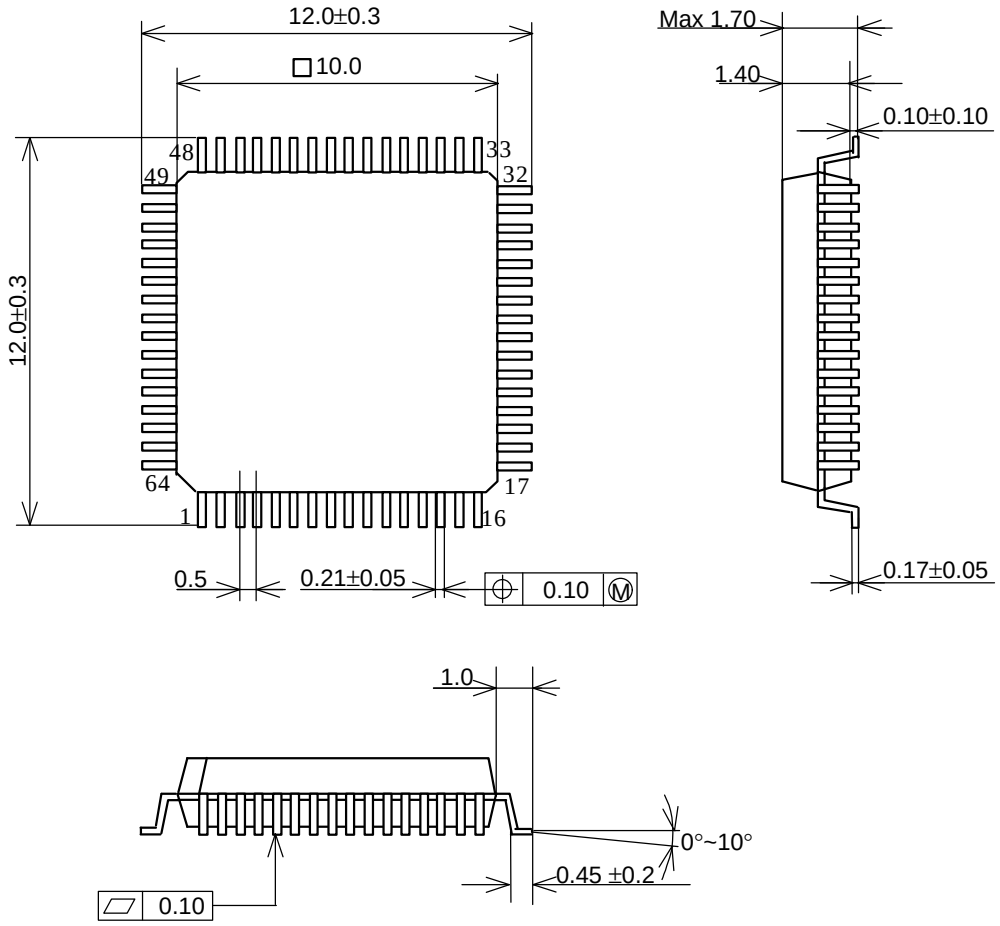


12-2-7) Connection to digital circuit

To minimize the noise resulting from the digital circuit, connect CMOS logic to the digital output. The applicable logic family includes the 4000B, 74HC, 74AC, 74ACT and 74HCT series.

Package

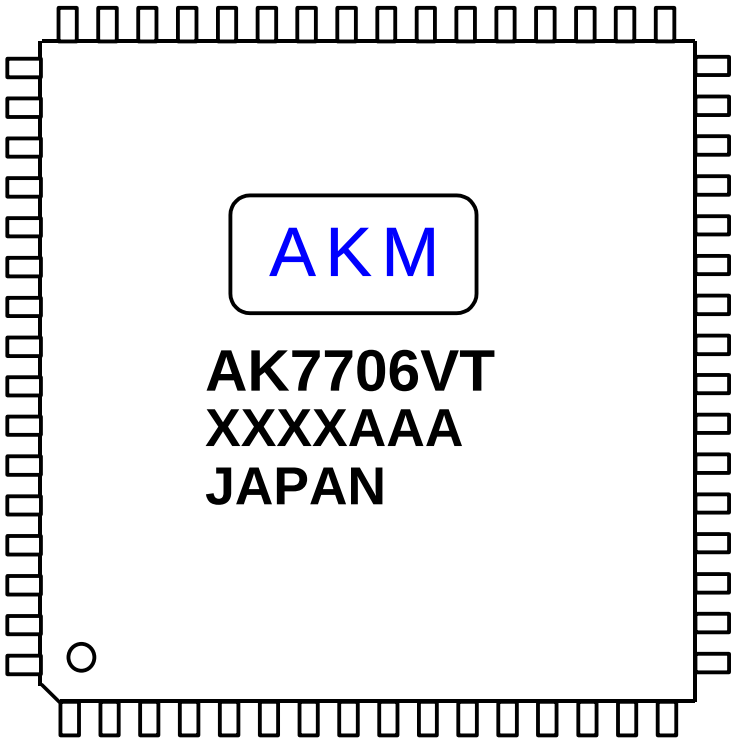
- 64-pin LQFP (Unit : mm)



- Material & Lead finish

Package:	Epoxy
Lead-frame:	Copper
Lead-finish	Soldering plate

Marking



Meanings of XXXXAAA
XXXX: Time of manufacture (numeral)
AAA: Lot numbers (Alphabet)

IMPORTANT NOTICE

- These products and their specifications are subject to change without notice. Before considering any use or application, consult the Asahi Kasei Microsystems Co., Ltd. (AKM) sales office or authorized distributor concerning their current status.
- AKM assumes no liability for infringement of any patent, intellectual property, or other right in the application or use of any information contained herein.
- Any export of these products, or devices or systems containing them, may require an export license or other official approval under the law and regulations of the country of export pertaining to customs and tariffs, currency exchange, or strategic materials.
- AKM products are neither intended nor authorized for use as critical components in any safety, life support, or other hazard related device or system, and AKM assumes no responsibility relating to any such use, except with the express written consent of the Representative Director of AKM. As used here:
  (a) A hazard related device or system is one designed or intended for life support or maintenance of safety or for applications in medicine, aerospace, nuclear energy, or other fields, in which its failure to function or perform may reasonably be expected to result in loss of life or in significant injury or damage to person or property.
  (b) A critical component is one whose failure to function or perform may reasonably be expected to result, whether directly or indirectly, in the loss of the safety or effectiveness of the device or system containing it, and which must therefore meet very high standards of performance and reliability.
- It is the responsibility of the buyer or distributor of an AKM product who distributes, disposes of, or otherwise places the product with a third party to notify that party in advance of the above content and conditions, and the buyer or distributor agrees to assume any and all responsibility and liability for and hold AKM harmless from any and all claims arising from the use of said product in the absence of such notification.