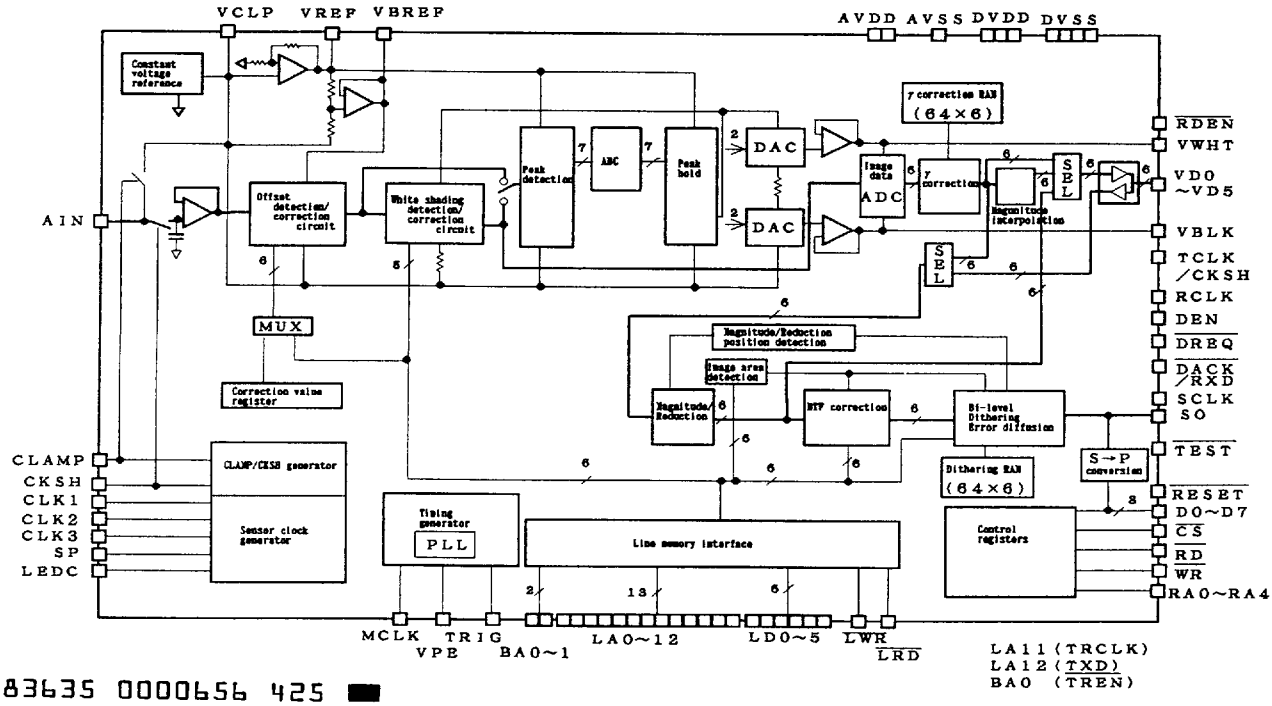
# =PRELIMINARY= AK8404

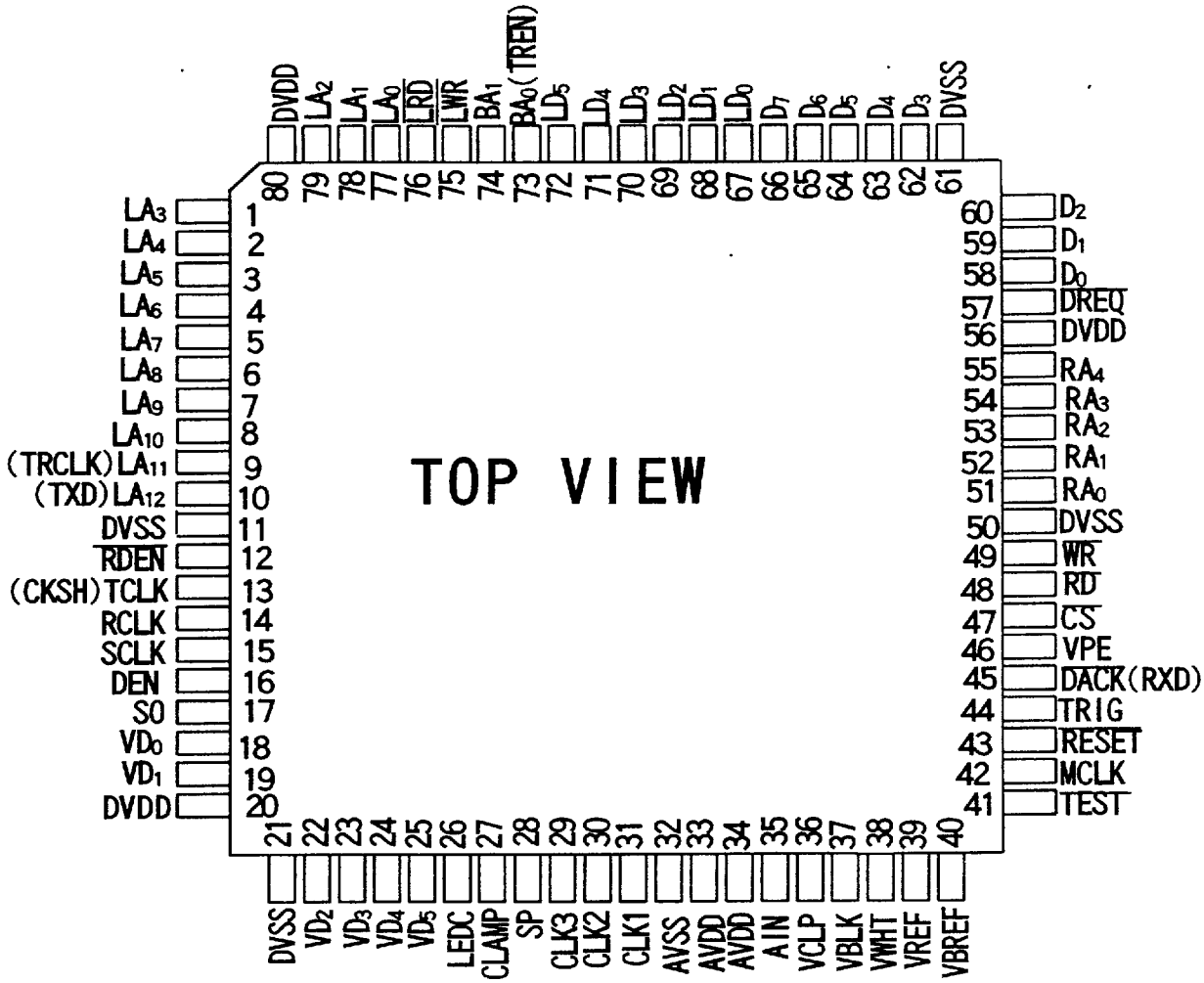
1Chip Image Processing LSI

## Features

- ☐Shading correction and Image processing LSI for CCD/CIS sensor
- ☐Input signal level 400mV$_{p-p}$～1.25V$_{p-p}$
- ☐Processing speed max 1.3Msample／sec
- ☐Max. sensor length 4096 (32pixels/step)
- ☐6bit ADC included (max 64scale)
  Contrast adjustment possible by 2×2bit DAC, which are volumes for black reference voltage and for white reference voltage of ADC.
- ☐ADC(detector) and analog multiplier(correcter) for white correction
  Correction 60% range of peak level by 5 bit(actual correction resolution is 6 bit)
- ☐6 bit ADC(detector) and DAC(correcter) for black correction
  correction resolution ±7mV(typ.)、correction range -135mV～205mV(typ.)
- ☐ABC function(7 bit peak detection/peak hold circuit included)
  Programmable tracking range(black/white limitter)
  ABC mode when binary scale、AGC mode when gray scale
- ☐Image data Control function
  RAMs for γ correction(64×6bit)、RAMs for dither(64×6bit) included
  Error diffusion function(Calculation by 10 bit internally)
  Image area separation、MTF correction(2 dimension、3×3 or 3×2)
  Magnification and reduction(programmable mag/red ratio: 1% step)
  magnification with interpolation possible
  (200DPI→300DPI, 300DPI→400DPI, 200DPI→400DPI) (external FIFO needed)
- ☐4 Line-memory supported
  Black shading memory(1)／White shading memory(1)／Image processing data memory(2 or 3)
  External RAM are sequential accessible
- ☐Sensor clock generation (CCD, CIS)
- ☐Serial I/F or parallel I/F(DMA) are available
- ☐Clock frequency:450KHz～1.3MHz(Data rate)、PLL included
- ☐CMOS monolithic LSI、+5V single power supply(5V±5%)、Constant voltage regulator included
- ☐80pin QFP



## Pin Assingnment



## Pin Description

| Pin No. | Pin Name | I/O | Function |
|---|---|---|---|
| | | Power Supply Pins | |
| 20,56,80 | DVDD | - | Digital power supply pins (5V typ.) |
| 11,21,50 61 | DVSS | - | Digital VSS |
| 33,34 | AVDD | - | Analog power supply pins (5V typ.) |
| 32 | AVSS | - | Analog VSS |
| | | Analog Pins | |
| 35 | AIN | I | Analog input pin. External capacitor for clamp is necesarry. |
| 36 | VCLP | O | Clamp voltage(1.25V) buffer output. Black correction is done to be matched to this voltage. External capacitor is necessary. |
| 40 | VBREF | O | Reference voltage(1.66V) buffer output for black correction. Full scale voltage of black correction is (VBREF-VCLP). |
| 39 | VREF | O | White-side reference voltage(2.5V) buffer output. |
| 37 | VBLK | O | Black-side reference voltage buffer output for image data ADC. |
| 38 | VWHT | O | White-side reference voltage buffer output for image data ADC. |
| | | Clock and Test Pins | |
| 42 | MCLK | I | Master clock input. Frequency will be same as the data rate (max 1.3MHz). |
| 41 | ($\overline{\text{TEST}}$) | I | Test pin. Pull up to 'H' level. |
| 44 | TRIG | I | Line start signal input. |
| | | CCD/CIS Drive Clock Pins | |
| 31,30,29 | CLK1,CLK2,CLK3 | O | Clock output pins for the sensor. |
| 28 | SP | O | Shift clock output pin for the sensor. |
| | | Sensor signal Input clock pins | |
| (13) | (CKSH) | O | Internal S/H clock output pin. (for monitoring) Sampled by 'H' level and holded by 'L' level. This pin common with TCLK pin. |
| 27 | CLAMP | O | Internal clamp clock output pin. Turned ON by 'H' level and turned OFF by 'L' level. |

| Pin No. | Pin Name | I/O | Function |
|---|---|---|---|
| | | Video Data Bus | |
| 14 | RCLK | O | Read clock output for FIFO. |
| 18~19<br>22~25 | VD0~VD5 | I/O<br>(3state) | 6 bit image data outputs. Or image data inputs from FIFO when magnification with interpolation mode. |
| 13 | TCLK | O | Write clock output pin for FIFO.<br>This signal must be used as the 6bit data sampling clock when magnification with interpolation mode. |
| 12 | $\overline{\text{RDEN}}$ | O | Read enable output pin for FIFO. |
| 16 | DEN | O | Video data enable signal, which shows data valid period. |
| 17 | SO | O | Image processed binary data output pin. |
| 15 | SCLK | O | Sampling clock ouput for binary or 6bit data.<br>MCLK can be used as the sampling clock also. |
| | | Micro-computer Interface | |
| 47 | $\overline{\text{CS}}$ | I | Chip select signal. |
| 48 | $\overline{\text{RD}}$ | I | Internal register read signal. |
| 49 | $\overline{\text{WR}}$ | I | Internal register write signal. |
| 51~55 | RA0~RA4 | I | Internal register address signals. |
| 43 | $\overline{\text{RESET}}$ | I | Internal register reset signal. Registers which are reset are shown in the section of "Register Function". |
| 58~60<br>62~66 | D0~D7 | I/O<br>(3state) | System data bus pins. |
| 57 | $\overline{\text{DREQ}}$ | O | DMA request output pin. |
| 45 | $\overline{\text{DACK}}$ | I | DMA acknowledge input pin. |
| | | Line memory interface pins | |
| 77~79<br>1~10 | LA0~LA12 | O | Line memory address pins. Max 4096 pixel sensor available. An extra bit is for magnification with interpolation mode. |
| 73~74 | BA0~BA1 | O | Line memory bank select signal. |
| 67~72 | LD0~LD5 | I/O<br>(3state) | Line memory data bus pins |
| 76 | $\overline{\text{LRD}}$ | O | Line memory read signal. |
| 75 | $\overline{\text{LWR}}$ | O | Line memory write signal. |

| Pin No. | Pin Name | I/O | Function |
|---|---|---|---|
| White shading data serial interface pins | | | |
| (9) | (TRCLK) | O | White shading data serial interface clock output This pin is common with LA11 pin. |
| (73) | (TREN) | O | White shading data serial interface enable signal. This pin is common with BA0 pin. |
| (10) | (TXD) | O | White shading data serial data output. This pin is common with LA12 pin. |
| (45) | (RXD) | O | White shading data serial data input. This pin is common with $\overline{\text{DACK}}$ pin. |
| Other pins | | | |
| 26 | LEDC | O | Peripheral output port suit for ON/OFF control of LED. Cleared by $\overline{\text{RESET}}$ signal. |
| 46 | VPE | I | Processing enable signal which determines whether to do processing next line data or not. |

## Function Description

### ■Analog circuit

□Reference Voltage generator

(1)Clamp reference voltage($V_{CLP}$) is generated by constant voltage regulator

$V_{CLP}$=1.25V(typ.)

(2)White-side reference voltage is generated by $2 \times V_{CLP}$.

$V_{REF}=2 \times V_{CLP}$=2.5V(typ.)

(3)ADC reference voltage($V_{BREF}$) for black shading detection/correction is generated by dividing $V_{REF}$ and $V_{CLP}$.

$V_{BREF}$=1.66V

□Sensor signal input circuit

(1)Polarity of input signal is white upward. If the polarity is inverted such as CCD sensor, input signal should be inverted.

(2)Internal analog switch and external capacitor makes up DC circuit.

(3)Bit-clamp and line-clamp modes are supported. In the line-clamp mode, clamp period is able to be set by (CLPEN). (CLPEN) is set by the control register.

□Black distortion detect ADC/correction circuit

(1)Correction data, which shows the difference between the clamp level and the signal level of each pixel, is detected by 6-bit ADC.

(2)Correction is achieved to subtract correction voltage, which is generated by the pre-detected correction data, from analog input signal.

(3)Detection range is 350mV(typ.).

□Peak detection/hold circuit

(1)Peak detect circuit is a low speed 7-bit ADC.

(2)Peak hold circuit is 7-bit DAC.

(3)Input signal into the peak detect circuit is the normalized one which is only black shading corrected signal when the peak fixed cycle of the peak detect mode, or black and white shading corrected one when scanning mode.

□White shading detect ADC/correction circuit

(1)White correction value is detected 5-bit ADC.
(Full-scale is 60% of difference between $V_{PEAK}$ and $V_{CLP}$.)

(2)Correction is achieved to amplify the black corrected analog signal by the pre-detected correction data.

□Reference voltage generator for 2-step flash ADC (DAC1, DAC2)

(1)DAC1, DAC2 are 2-bit DAC which generates black and white reference voltage for the ADC, which are relative voltage by $V_{PEAK}$ and $V_{CLP}$.

□2-step flash ADC

(1)6-bit ADC which converts the normalized analog signal finally.
Reference voltage is programmable by setttig above mentioned DACs.

□PLL

(1)Generate ×16 clock from sensor data rate clock(1.3MHz max).

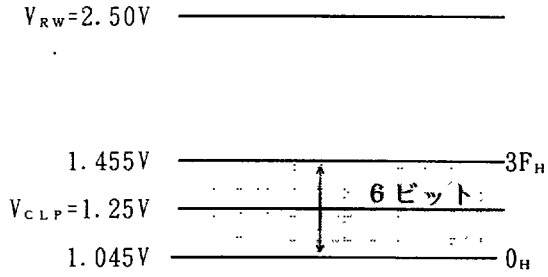



Fig.1-1 Black shading detect/correct

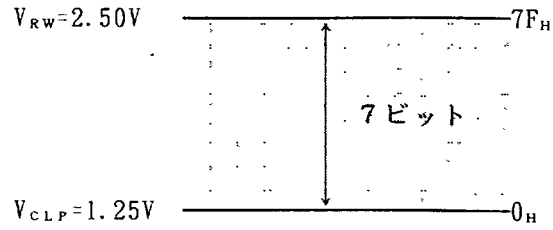



Fig.1-2 Peak detect/hold

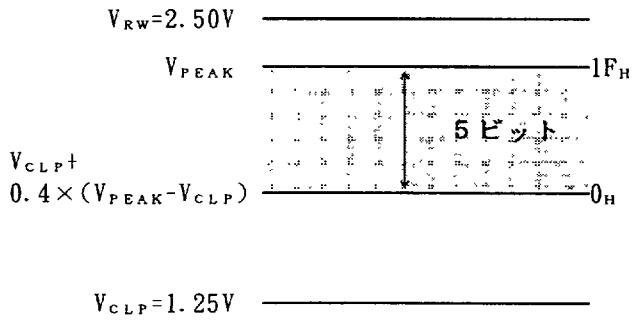



Fig.1-3 White shading detect/correct

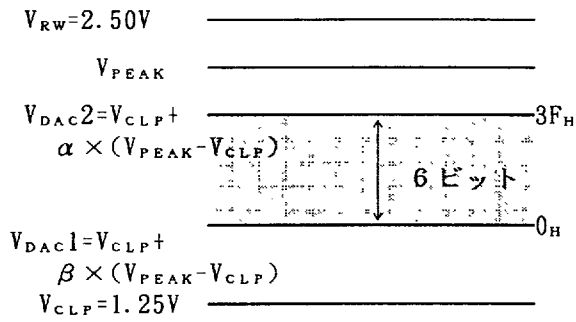



Fig.1-4 2-step flash ADC

**1)$V_{DAC1}$ and $V_{DAC2}$ are the voltage of DAC1 and DAC2 that generate reference voltage of image data ADC

■Black shading detect

Analog input includes following error.

(1)Pre-amplifier offset, AK8404 internal switch feed-through, and internal amplifier offset.

(2)Sensor offset and deviation occuring from dark current.

AK8404 supports following correction mode.

(1)Pixel to pixel correction mode (Uses external memory)

(2)Fixed offset cancel mode (Uses internal register)

□Pixel to pixel correction mode (Uses external memory)

(1)Detects the black shading data by 6-bit ADC and stores the data into the external SRAM with scanning black reference signal.

□Fixed offset cancel mode (Uses internal register)

(1)Detects the black shading data by 6-bit ADC and stores the data into internal register with scanning black reference signal. Before that, the position of the reference pixel by the control register.

■Peak detect

This mode is used to set the peak before white shading detect(the signal amplitude, to be matched with the full scale of the white shading detect use ADC), or to set initial peak value before scanning.
This mode consists of the 2 cycles.

□Peak pre-detect cycle

(1)AK8404 detects the maximum value(PPK) of 2-step flash ADC output to scan the white reference signal, with DAC1, DAC2 and peak hold circuit are set to the full scale.
(Internally, analog black correction to the white reference signal is achieved as shown below.)

(Pixel to pixel correction mode)

(black corrected white reference signal)$_i$ =
(white reference signal)$_i$ - $A$(black shading data)$_i$

(Fixed offset cancel mode)

(black corrected white reference signal)$_i$ =
(white reference signal)$_i$ − $A$(BOFF)

Besides, $A$(D) is an analog value which is DA-convert D.
BOFF is a contents of black correction register.

(2)Width of detect is same as the available length of sensor.

□Peak fix cycle

(1)The peak value is fixed by 7-bit peak detect circuit with re-scanning the white reference signal after setting the initial value arround PPK to the peak detect counter internally.

(2)Width of detect is same as the available length of sensor.

(3)PBL/PWL limitter is automatically inhibited.

(3)Finishing this mode, peak detect counter value is automatically loaded into the peak hold register.

■White shading detect

White shading detect is done for removing the deviation of the light emmition and the sensor sensitivity. Correction value is detected before the scanning.

(1)Black reference of white correction detect use 5-bit ADC is automatically set to 40% of $V_{PEAK}$. Full scale of the ADC is from $0.4 \times V_{PEAK}$ to $V_{PEAK}$.
Detects the white shading data by 5-bit ADC and stores the data into the external SRAM with scanning white reference signal.

■Shading correction in the scanning mode

☐ Black correction

Gets black shading corrected video signal by the following way.

(Pixel to pixel correction mode)

$(\text{Black corrected video signal})_i = (\text{Video signal})_i - A(\text{Black correction value})_i$

(Fixed offset cancel correction mode)

$(\text{Black corrected video signal})_i = (\text{Video signal})_i - A(\text{BOFF})$

Besides, $A(D)$ is an analog value which is DA-converted D.
BOFF is a contents of black correction register.

☐ White correction

Gets black/white shading corrected video signal by the following way.

$(\text{Black \& white corrected video signal})_i =$
$(\text{Black corrected video signal})_i \times 51.7/(20.7+(\text{White correction data})_i)$

## ■ABC function

The purpose of ABC function is to read clearly regardless groundwork density by following the white refewrence voltage of 2-step flash ADC to the change of groundwork density.
ABC function supports two modes, which are called "ABC mode (for the document with characters)" and "AGC mode (for the document with photographs)" .
ABC functions are enabled or disabled by the control register, and are also automatically disabled when VPE(line active)=0.

### □ABC mode

Detects the peak value of black and white shading corrected video signal during ABC enable(ABCEW), and that value should be as $PEAK_k$.
The peak hold value of the next line($PHD_{k+1}$) is determined by comparing the peak value($PEAK_k$) with the peak hold value of the present line($PHD_k$) according to the following equations.

$PEAK_k < PHD_k \rightarrow PHD_{k+1}=PHD_k-f$
$PEAK_k \geqq PHD_k \rightarrow PHD_{k+1}=PEAK_k$

Peak detect counter starts from reset state($0_H$) for the every each line.

ABC range is programmable by black and white limitter.
Following speed to the black-side is selectable as shown below.

| FSEL | Following speed (f) |
|---|---|
| 0 | 1 LSB is by 4 LINE (1/4LSB) |
| 1 | 1 LSB is by 2 LINE (1/2LSB) |
| 2 | 1 LSB is by 1 LINE (1LSB) |
| 3 | 2 LSB is by 1 LINE (2LSB) |

ABC following speed to the black-side

### □AGC mode

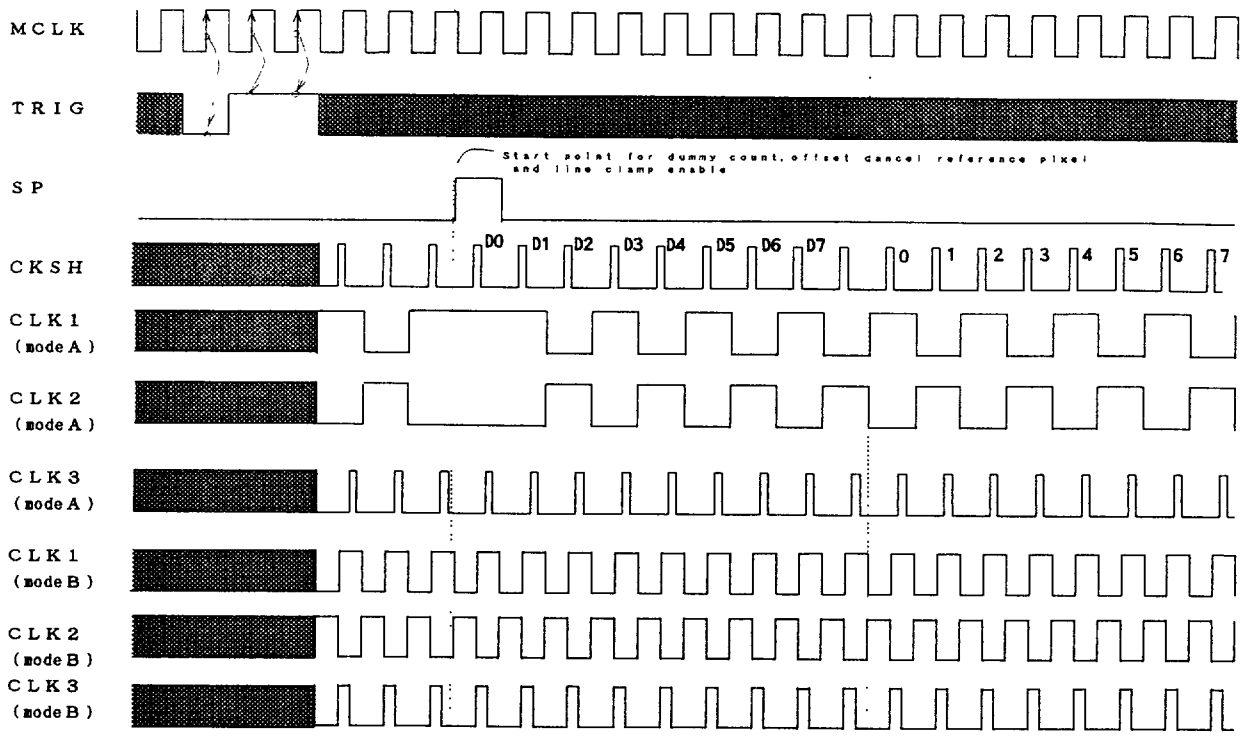
In AGC mode, peak value is determined by the following equations.

$PEAK_k < PHD_k \rightarrow PHD_{k+1}=PHD_k$
$PEAK_k \geqq PHD_k \rightarrow PHD_{k+1}=PEAK_k$

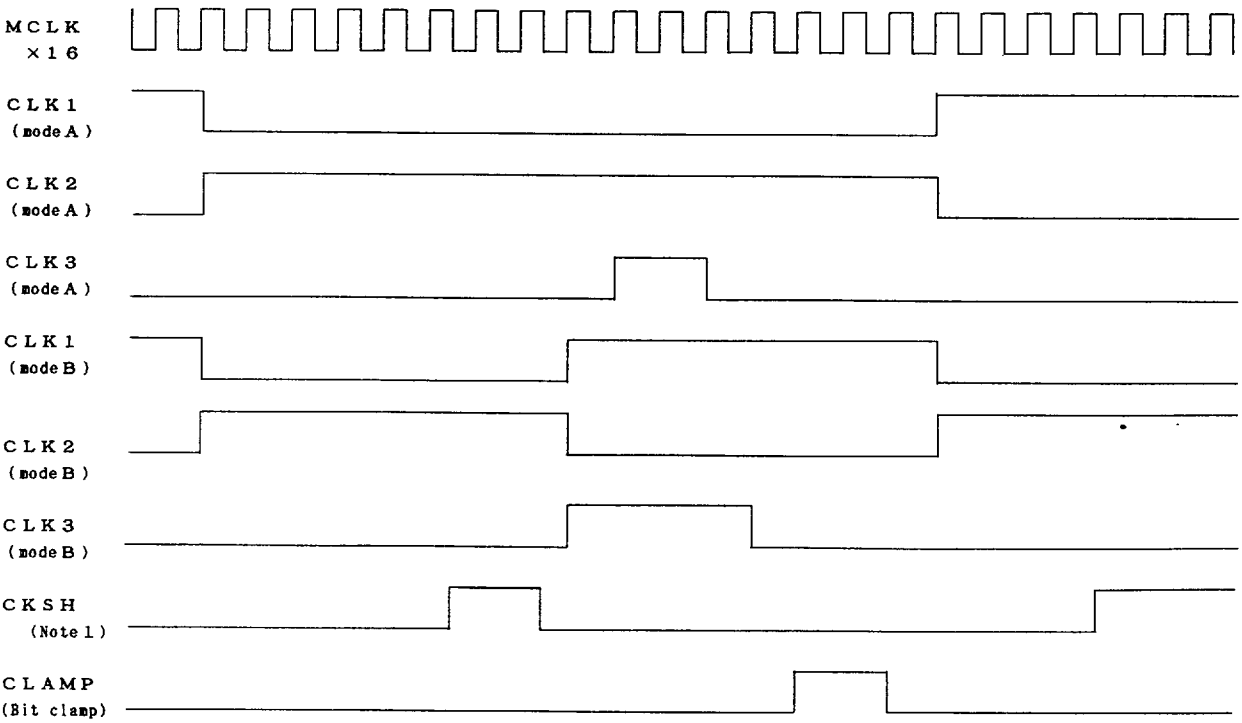
ABC range is programmable by white limitter.

■Sensor clocks generator

AK8404 support two types of clock generation modes, which are called as "MODE A" and "MODE B" for every CIS or CCD.




Detail timing for the above




(Note1)Line clamp mode A:CLPEN itself should be the CLAMP clock.
Line clamp mode B:CKSH&CLPEN should be the CLAMP clock.

■Timing control signals generator

AK8404 generates following 5 signals used for timing control.

1. (EN) :Input video signal enable
2. (ABCEW) :ABC enable width
3. (CLPEN) :Line clamp enable
4. (BOFFEN) :Black reference pixel enable
5. DEN :Output image data enable

□Input video signal enable (EN)

This is the video signal enable width, which is determined by dummy pixel count and pixel count registers.

□ABC enable (ABCEW)

This signal is the ABC enable when scanning mode mode.
Start pixel and end pixel can be set by each every 256 pixels by the control registers.

□Line clump enable(CLPEN)

This signal is the clamp enable width among a line in the line clamp mode, which can be set by every 1 pixel by the control register.
It should be set in dummy pixels.

□Black reference pixel enable (BOFFEN)

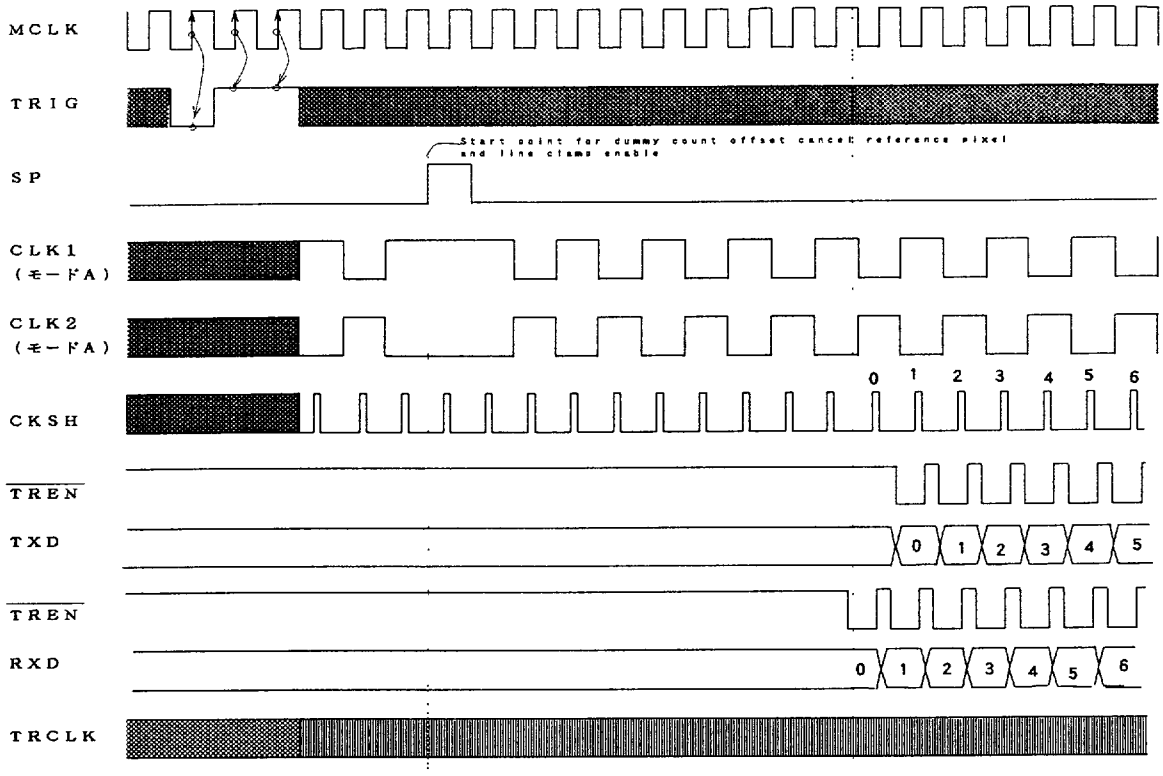
This signal is used to determine the black reference pixel when offset cancel mode, which can be set by every 16 pixel by the control register.
It can be set either in the dummy pixels or the effective pixels.

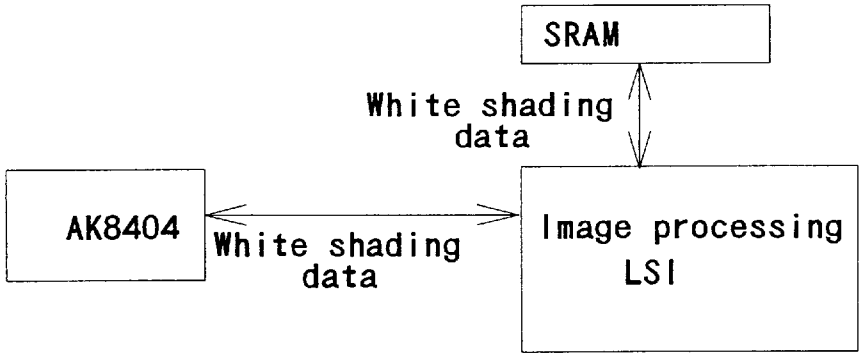
□Output image data enable DEN

This signal shows the data valid period in the line.
This signal becomes active at the line, which is determined as the enable line by VPE.
VPE is sampled at the beggining of the line.

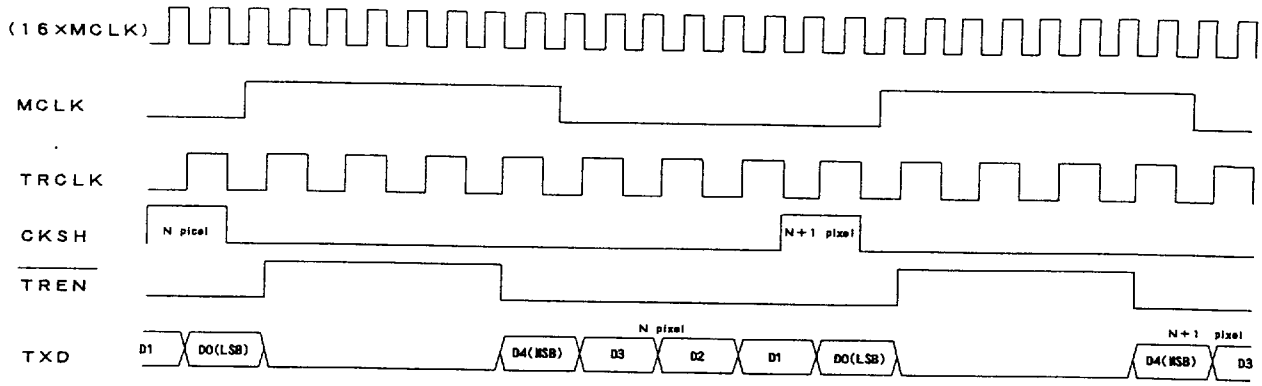
■Serial interface for white shading data

When the white shading data are stored in another SRAM, which is one controlled by another LSI, this interface can be used for transfer/receive the shading data.
When this interface is enabled, it transfers the shading data to the exernal in the white shading detect mode, and it receives the shading data from the external in the scanning mode.

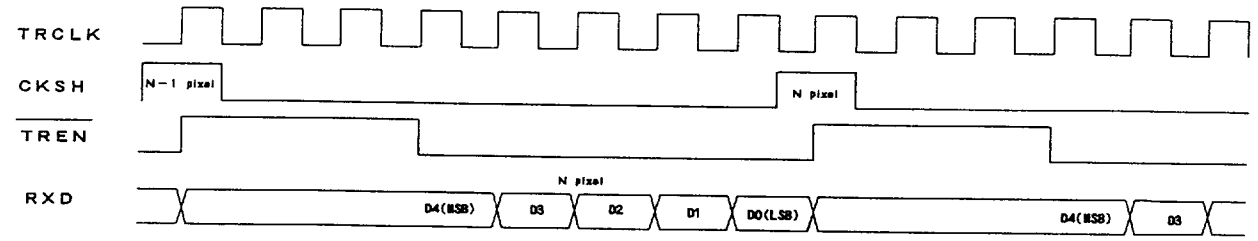



The total system configulation supposed to be by this interface is as the above.
In this system, the functions utilized are limited to shading correction, $\gamma$ correction and magnification and reduction and so on.
Please note that the related pins with this interface are all common with other functional pins.




(A) Transfer timing(White shading detect mode)




(B) Receive timing(Scanning mode)

Details timing

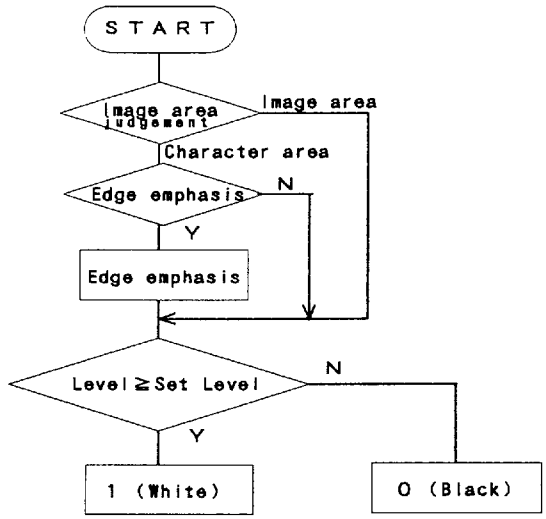
## ■Image processing

### □Image processing mode

AK8404 support 4 types of Image processing mode. Each Image processing mode is shown in the following flow chart.

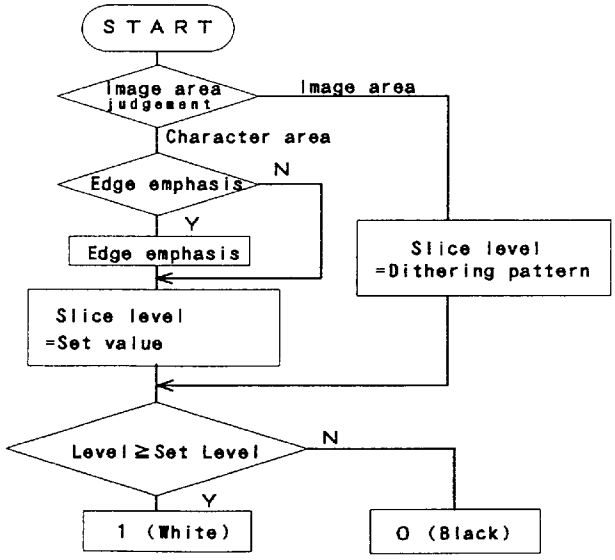
(1)Bi-level processing

Character area is by Bi-level processing(with edge enphasis), and image area is by simple Bi-level processing(without edge enphasis).
Edge emphasis for character area is set by the control register.



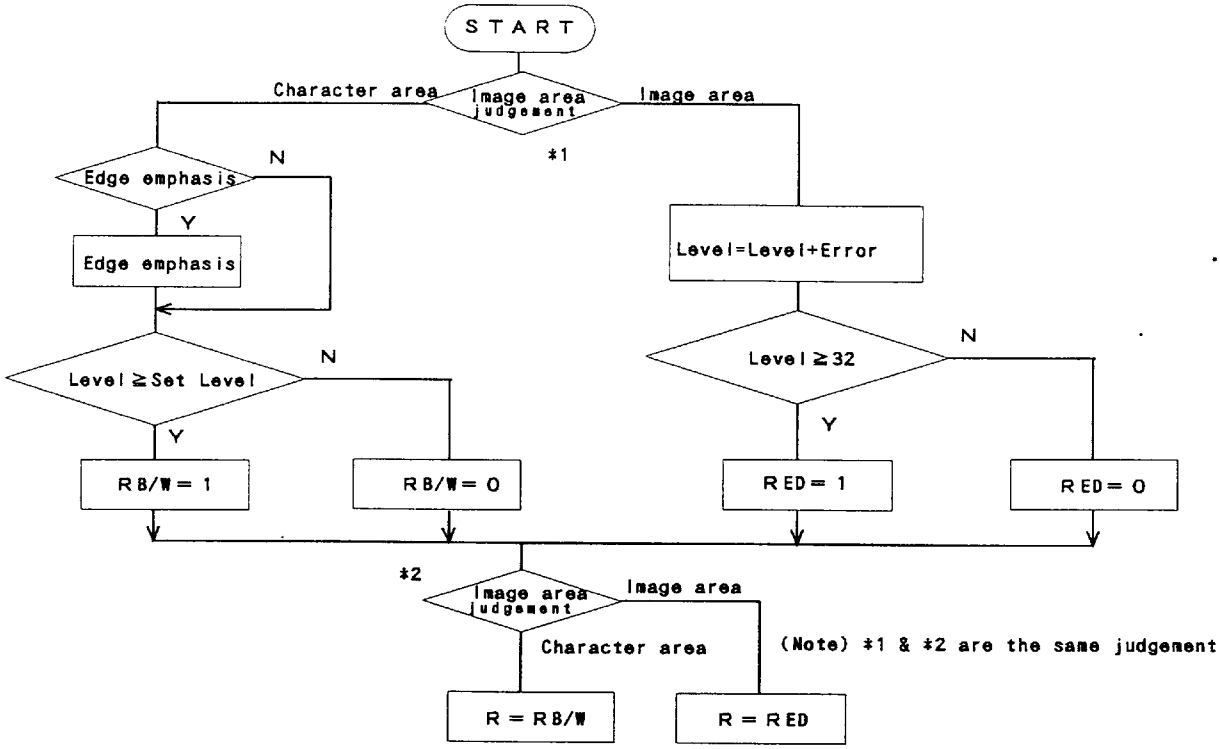

(2)Dithering

Character area is by Bi-level processing, and image area is by dithering.
Edge emphasis for character area is set by the control register.



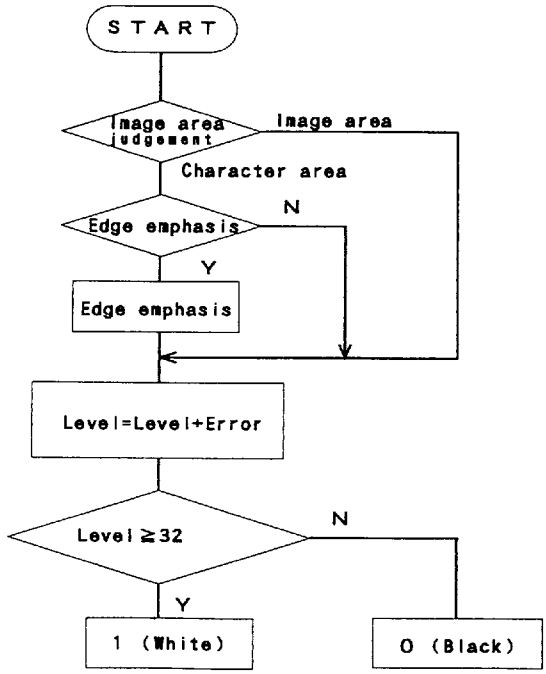
(3)Error diffusion A

Character area is by Bi-level processing, and image area is by error diffusion.
Edge emphasis for character area is set by the control register.




(4)Error diffusion B

All area is by error diffusion.
Edge emphasis for character area is set by the control register.



(5)Line memory for the image processing

AK8404 controls 4 banks of line memory. The contents of this memory is as the below table, depending on the image processing mode or other conditions.

| | Image processi -ng mode | Image processi -ng window | Black correcti -on type | Contests |
|---|---|---|---|---|
| Bank 0 | Bi-level Dither | X | X | Black shading data |
| | Error di -ffusion | 3 × 2 | X | Black shading data |
| | | 3 × 3 | pixel to pixel | Black shading data |
| | | | offset cansel | 6 bit image data for the before the previous line |
| Bank 1 | X | X | X | White shading data |
| Bank 2 | X | X | X | 6 bit image data for the before the previous line |
| Bank 3 | Bi-level Dither | X | X | 6 bit image data for the before the previous line |
| | Error di -ffusion | X | X | Error data |

As shown in the above table, pixel to pixel type black correction, error diffusion 3×3 window set at the same time is inhibited.
In this case, the black correction mode set is superior than the window set. As that result, when these parameters are set, Image processing window is automatically 3×2.

□Image area detect

Image area detection is performed by comparing target pixel level, differential data between target pixel level and surrounding pixels' one(3×2, 3×3 window) with each thereshold parameter.
Three parameters can be set by the control registers.

□MTF compensation

MTF compensation is performed by the Laplacian filter (3×2, 3×3window). Coefficients are fixed.

□Dithering

AK8404 executes dithering according to the arbitrary pattern in the internal RAM, which is defined by customers. Dithering RAM consists of 8×8 matrix, and all 64 bits of this matrix must be filled up.

(Example) 16 gray scale

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| P11 | P12 | P13 | P14 | P11 | P12 | P13 | P14 |
| P21 | P22 | P23 | P24 | P21 | P22 | P23 | P24 |
| P31 | P32 | P33 | P34 | P31 | P32 | P33 | P34 |
| P41 | P42 | P43 | P44 | P41 | P42 | P43 | P44 |
| P11 | P12 | P13 | P14 | P11 | P12 | P13 | P14 |
| P21 | P22 | P23 | P24 | P21 | P22 | P23 | P24 |
| P31 | P32 | P33 | P34 | P31 | P32 | P33 | P34 |
| P41 | P42 | P43 | P44 | P41 | P42 | P43 | P44 |

32 gray scale

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| P11 | P12 | P13 | P14 | P15 | P16 | P17 | P18 |
| P21 | P22 | P23 | P24 | P25 | P26 | P27 | P28 |
| P31 | P32 | P33 | P34 | P35 | P36 | P37 | P38 |
| P41 | P42 | P43 | P44 | P45 | P46 | P47 | P48 |
| P11 | P12 | P13 | P14 | P15 | P16 | P17 | P18 |
| P21 | P22 | P23 | P24 | P25 | P26 | P27 | P28 |
| P31 | P32 | P33 | P34 | P35 | P36 | P37 | P38 |
| P41 | P42 | P43 | P44 | P45 | P46 | P47 | P48 |

64 gray scale

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| P11 | P12 | P13 | P14 | P15 | P16 | P17 | P18 |
| P21 | P22 | P23 | P24 | P25 | P26 | P27 | P28 |
| P31 | P32 | P33 | P34 | P35 | P36 | P37 | P38 |
| P41 | P42 | P43 | P44 | P45 | P46 | P47 | P48 |
| P51 | P52 | P53 | P54 | P55 | P56 | P57 | P58 |
| P61 | P62 | P63 | P64 | P65 | P66 | P67 | P68 |
| P71 | P72 | P73 | P74 | P75 | P76 | P77 | P78 |
| P81 | P82 | P83 | P84 | P85 | P86 | P87 | P88 |

Slice level of bi-level processing is converted form 4bit format to 6bit format by the following equation.

$$\text{Slice level} = 4 \times (\text{set value}) + 3$$

And bi-level, dither is done as the below equations.

Level ≧ Slice level then 1 (white)
Level < Slice level then 0 (black)

□Error diffusion

AK8404 multiplies the errors(6 bit data with sign:-31～31) which occures when slicing by the fixed thereshold(32) by fixed coefficients, and diffuses these errors to the surrounding pixels.
To minimize the error by arithematic operation, AK8404's internal operation is done by 10bits.
When saving temporary products into the external memory, lower 4bits are ignored.

□ γ correction

AK8404 performs γ correction by setting data into the internal RAM.

(Example)

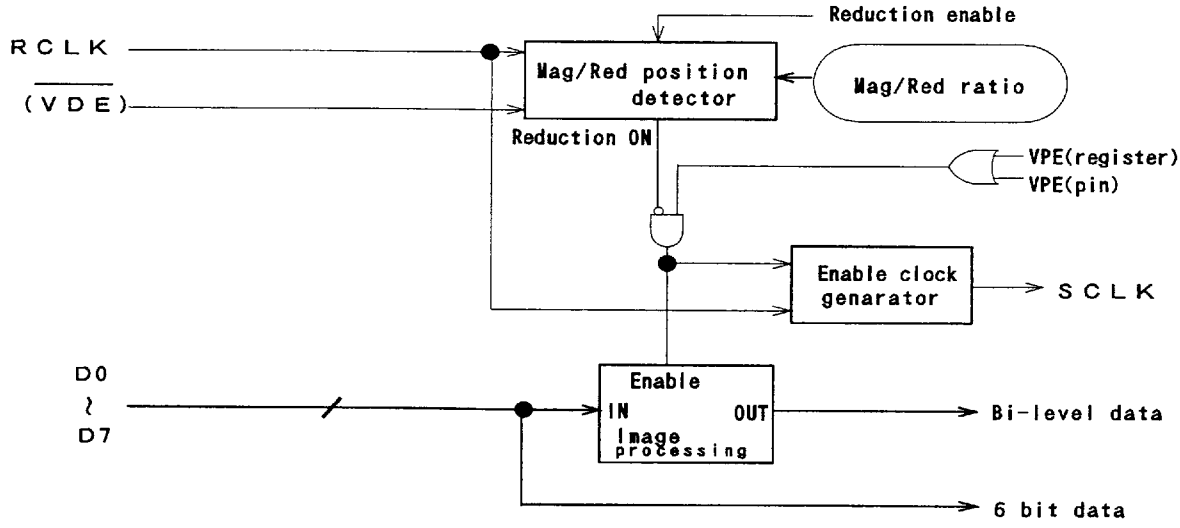
| Input Data (Address) | RAM Table | Output Data (γ correction) |
|---|---|---|
| 0 | 0 | 0 |
| 1 | 0 | 0 |
| 2 | 1 | 1 |
| 3 | 1 | 1 |
| | | |
| 62 | 63 | 63 |
| 63 | 63 | 63 |

□Magnification/Reduction

AK8404 supports reduction from 1% to 99% (1% step) and magnification from 101% to 200% (1% step). Besides, as to the magnification in the case of 200dpi→300dpi, 300dpi→400dpi, 200dpi→400dpi, magnification with interpolation is supported.

Continuity of the image processing in the reduction mode is mainteined by controlling execution/stop according to the reduction/magnification detector's judgement.
Magnification is performed by outputting 6 bit or bi-level data 2 times, according to the reduction/magnification detector's judgement.
Magnification/Reduction position detector circuit works for the left end pixel of document not to be lost.

In this type of magnification, the special SRAM is not necessary, because that the processing is done at the real time.



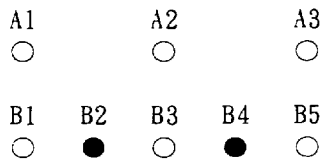
□Magnify interpolation

AK8404 supports magnification with interpolation mode in the following ratio.

200dpi→300dpi(150%), 300dpi→400dpi(133%), 200dpi→400dpi(200%)

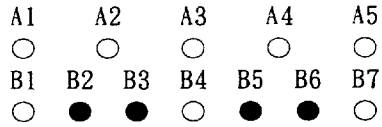
Interpolating data are created according to the following equations.

(200dpi→400dpi)



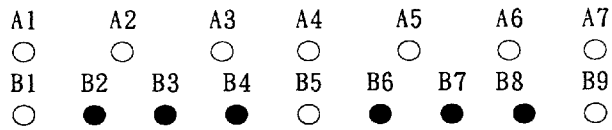

$B_{2i-1} = A_i$
$B_{2i} = (A_i + A_{i+1})/2$

(200dpi→300dpi)




$B_{3i-2} = A_{2i-1}$
$B_{3i-1} = 3/8*A_{2i-1}+5/8*A_{2i}$
$B_{3i} = 3/8*A_{2i+1}+5/8*A_{2i}$

(300dpi→400dpi)




$B_{4i-3} = A_{3i-2}$
$B_{4i-2} = 1/4*A_{3i-2} + 3/4*A_{3i-1}$
$B_{4i-1} = 1/2*A_{3i-1} + 1/2*A_{3i}$
$B_{4i} = 1/4*A_{3i+1} + 3/4*A_{3i}$

In this mode, line memory size which covers the increased pixel count is necessary.

Memory size = pixel count × magnification ratio × 4

(Example)
In the case of converting B4 size 200dpi(2048 pixel) to 400dpi.

Line memory 2K×2×4=16K byte (256K bit SRAM)

□FIFO interface

At the magnification with interpolation external FIFO memory is necessary.
2 types of interface clock modes can be selected by the control register. In the either case FIFO must be static type(SRAM), because AK8404 doesn't support the refresh circuit.

Mode A is for ICT FIFO products(ex. IDT7202) use, and mode B is for NEC FIFO products ($\mu$PD485505) use.

Necessary word count is according to the following equation.

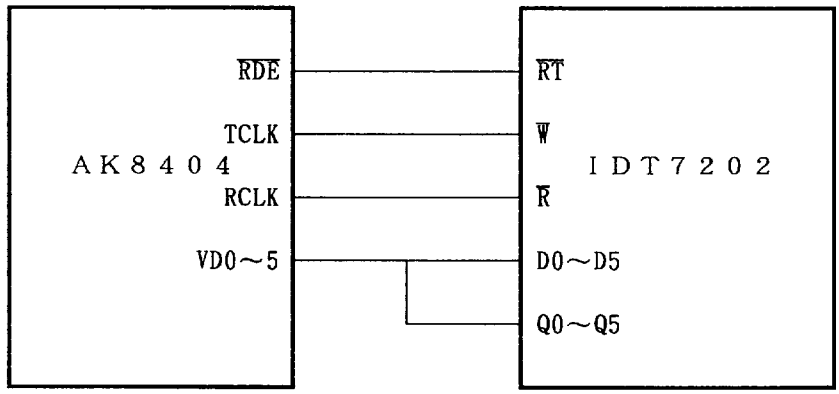
Memory word = pixel count × (magnification ratio-1) + 5

(Example)
In the case of converting A4 size 200dpi(1728 pixel) to 300dpi.

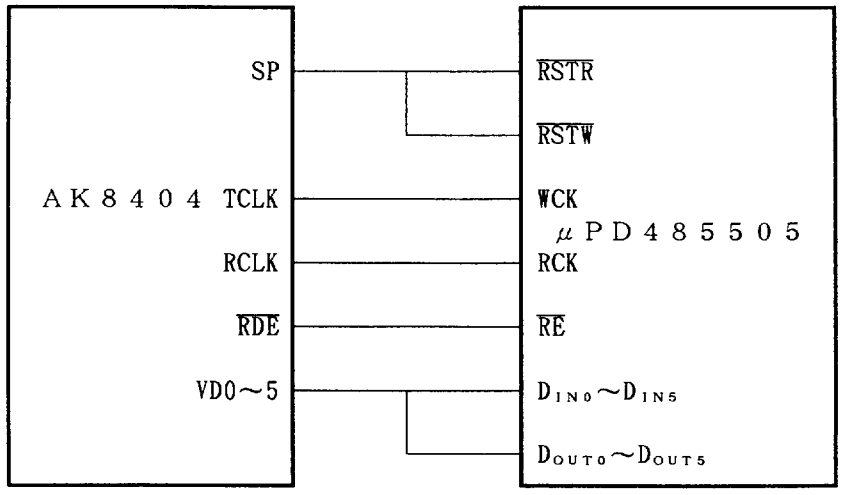
FIFO 1728×(1.5-1)+5=869 word

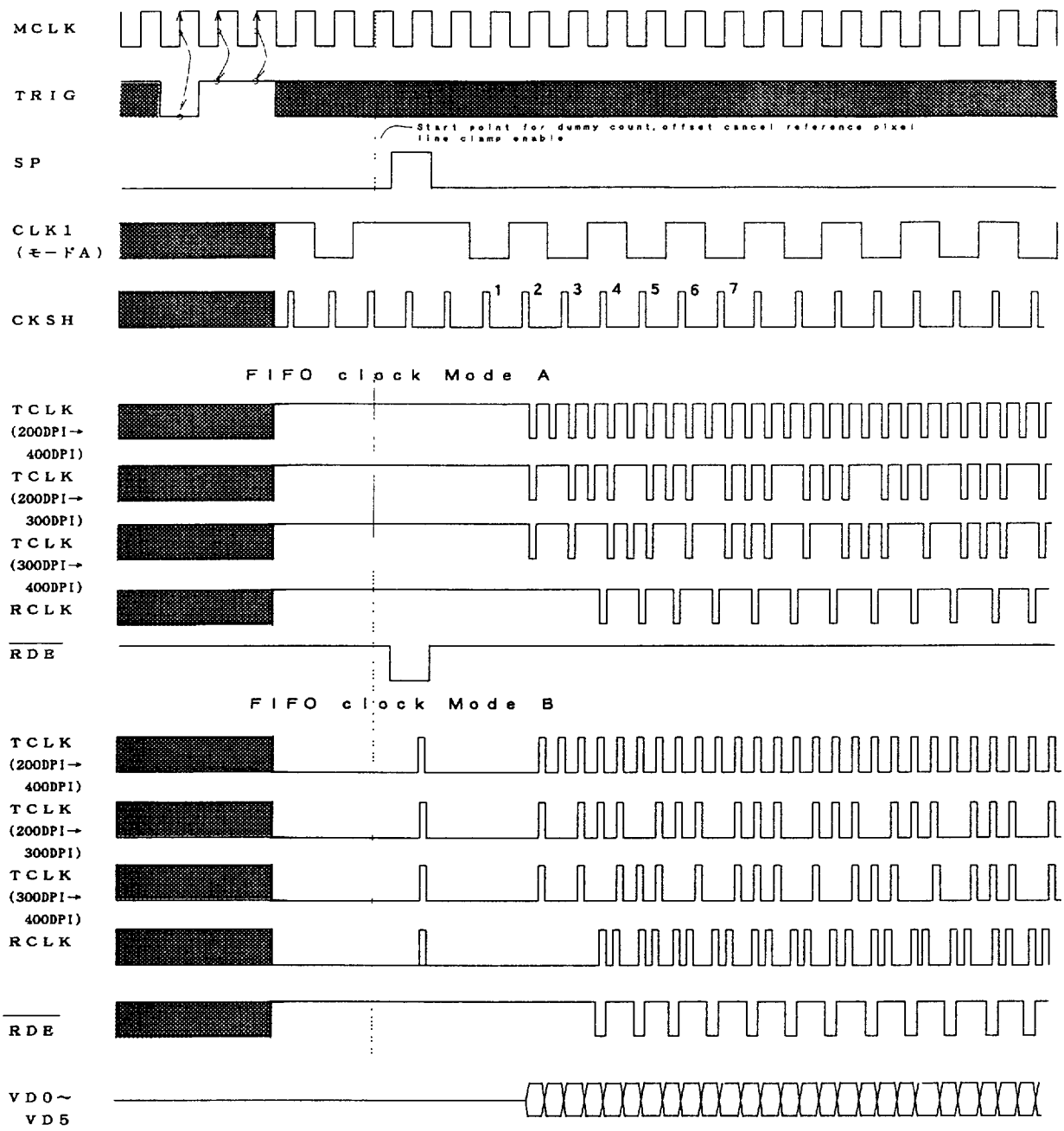
When VPE is "L", FIFO interface clocks, which are TCLK, RCLK and so on don't output.
Write cycle time equals to video signal rate by magnification ratio, on the other hand read cycle time and the successive image processing rate equal to video signal rate.
So please note that line time(TRIG pulse period) must be more longer to cover the increased pixel count.

Mode A




Mode B





## ■. Output data format

### □Serial output

AK8404 outputs 6 bit data through VD bus(VD0～VD5) and bi-level data through SO pin. In both cases, basic sampling clock is SCLK. In the reduction mode, some portion of SCLK are skipped, and in the magnification mode, some clocks are inserted.
6 bit data outputs through VD bus connected to FIFO at the magnification with interpolation mode also. In this case sampling clock should be TCLK, which is FIFO write clock.
MCLK also can be used as the sampling clock only in the cases without reduction/magnification.

### □Parallel output (DMA interface)

Bi-level data can be read through the system bus(D0～D7) after serial to parallel conversion.
When DMA controller receives AK8404 $\overline{DREQ}$ signal, it can read out 8 bit data by $\overline{DACK}$=L.

### □TCLK/SCLK/$\overline{DREQ}$

In serial or parallel interface case, SCLK, $\overline{DREQ}$, and TCLK count are shown below.

Without magnification and reduction

N : pixel number(multiple of 32)

$n_{SCLK}=N$

$n_{DREQ}=N/8=n$

With magnification or reduction

N : pixel number(multiple of 32)

k : Magnification or reduction ratio

[M] : Minimum integer which are not smaller than M

$n_{SCLK}=[N\times k]$

$n_{DREQ}=[[N\times k]/8]$

(Example 1) N=1728, k=0.71

$n_{SCLK}=[1728\times 0.71]=[1266.88]=1267$

$n_{DREQ}=[[1728\times 0.71]/8]=[[1266.88]/8]$
$=[1267/8]=[158.375]=159$

(Example 2) N=1728, k=1.15

$n_{SCLK}=[1728\times 1.15]=[1987.2]=1988$

$n_{DREQ}=[[1728\times 1.15]/8]=[[1987.2]/8]$
$=[1988/8]=[248.5]=249$

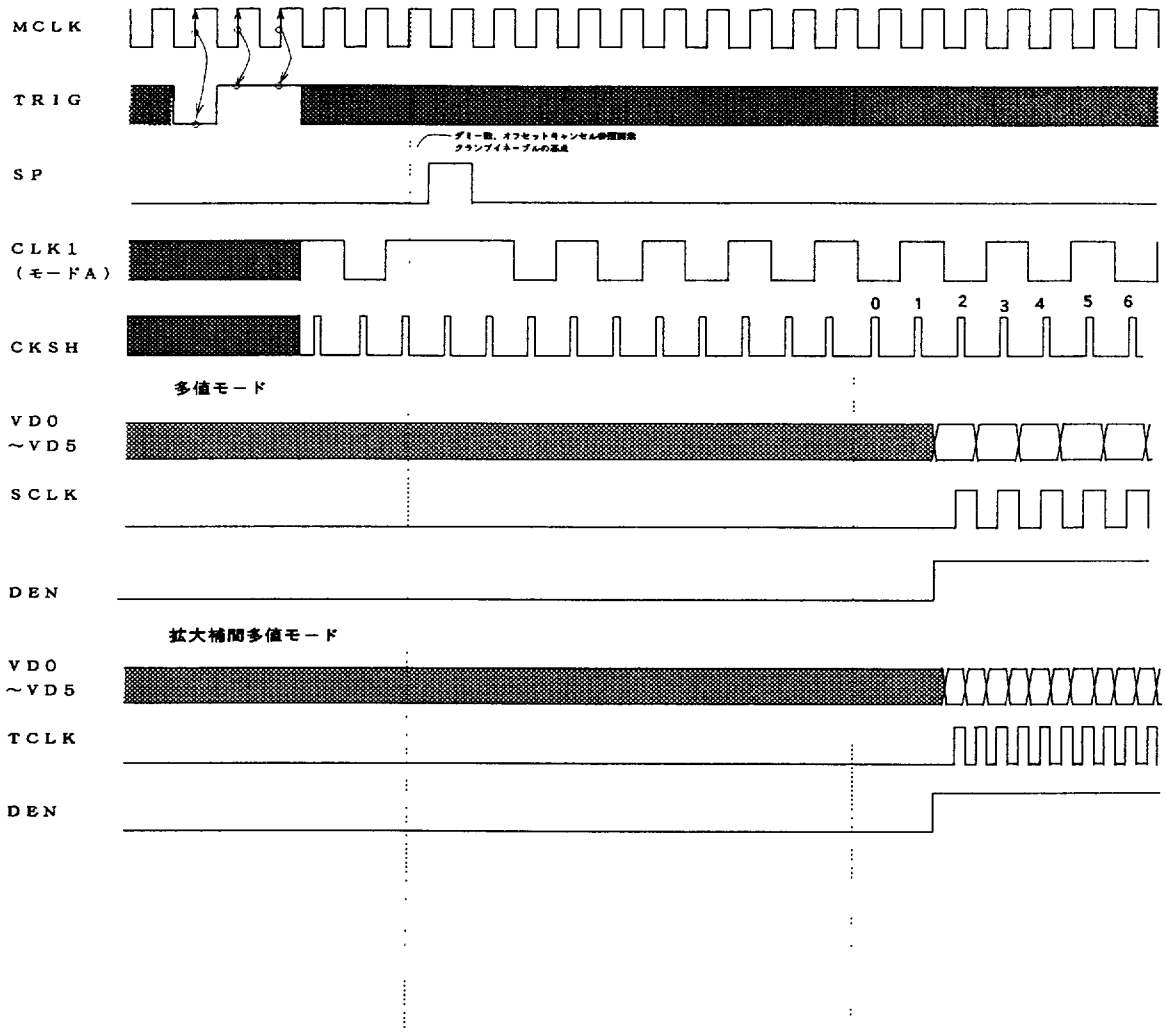
With magnification with interpolation

$n_{TCLK}=$

$n_{SCLK}=$

$n_{DREQ}=$

In the case of parallel interface, shortage data are filled by '0' to satisfy that data count number should be multiple of 8.
Please note that in the magnification mode, SCLK, TCLK, and $\overline{DREQ}$ frequency becomes twice.



## ■Operation control

### □Pre-processing stage

Before scanning the document, it is needed to detect shading data of the image sensor. Basic operation sequence of the pre-processing stage is

(1) Initial parameters set
(2) Black shading detect
(3) Peak detect
(4) White shading detect

After these operations are finished, shading data or peak value are stored in the in the external RAM or in the internal register.

When executing pre-processing modes such kind of procedure is typical, that setting OPERATION MODE bits and OPERATION ENABLE bit, the command becoming valid at the first TRIG after it is issued, waiting adequate time, and checking BUSY flag to confirm that executing each operation mode is finisfed.

In the mode except scanning mode, AK8404 turn into idle mode after execution of each operation mode.

Black shading detect mode, white shading detect mode takes 1 line cycle. Peak detect mode takes 2 cycle. In this period, wait state by the timer should be inserted.

### □Scanning stage

In the scanning mode, please set VIDEO PROCESSING ENABLE bit or VPE pin, and PAGE START bit to "H" state, in addition to OPERATION ENABLE bit and OPERATION MODE bits.

Command becomes valid at the first TRIG after it is issued.

After 1 line image processing, PAGE START bit is automatically cleared, and image data and sampling clocks(TCLK, SCLK), DMA request($\overline{\text{DREQ}}$) begins to output.

Because of 1 line output delay of the image data, the extra 1 line image proccesing is necessary to send out all data.

When reduction of sub-scan axis is done by skipping lines, or paper feed is stopped, image processing must be stopped. In this case please reset VIDEO PROCESSING ENABLE bit or VPE pin into "L" state. Same as enable command case, this command becomes valid at the first TRIG after it is issued.

### □Memory access

It is possible to access internal RAM( $\gamma$ correction table RAM or dithering pattern RAM) or external line memory through AK8404. In this mode, please reset VIDEO PROCESSING ENABLE bit and VPE pin to "L" state, and set LINE MEMORY ACCESS ENABLE bit to "L", and after that, to "H" state.

After that, you can read/write through the window register sequentially.

Bank select of black/white shading data, image data for the previous line, image data before for the previous line, and error data, which are all stored in the external RAM, and also $\gamma$ correction table or dithering pattern, which are stored in the internal RAM.

Access to the internal RAM is also sequential.

Dither pattern RAM can be accessed in order that Pij(j=1 to 8(i=1 to 8)).

$\gamma$ correction table RAM can be accessed in ADC's code order(0 to 63).

## Register

| Address (HEX) | Init. | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 00H | W (R) | Operation Ena. (BUSY) | Page Start | LEDC | Image Pro. Ena (VPE) | Memory Access Enable | ABC Enable | Operation mode | |
| 1 | 00H | W | Mag./ Reduct. Enable | Mag. w interp Enable | Magnify Interpolation Ratio | | ABC Time constant | | White Limitter Enable | ABC Mode |
| 2 | 08H | W | γ Correction Enable | MTF Correction Enable | Image Processing mode | | Bi-level Slice level | | | |
| | | | | | | | SL6 | SL5 | SL4 | SL3 |
| 3 | 00H | R/W | X | X | Window select | Bi-level 6bit data select | Black Correction type | Internal RAM/Line memory Bank select | | |
| 4 | 00H | R/W | X | X | CKSH/ TCLK select | W data serial I/F ena. | FIFO clock select | SP clock polarity select | Line clump pulse sel. | Sensor Clock Select |
| 5 | XXH | W | ABC White side limitter | | | | ABC Black side limitter | | | |
| | | | AWL3 | AWL2 | AWL1 | AWL0 | ABL3 | ABL2 | ABL1 | ABL0 |
| 6 | XXH | W | X | X | X | Image area separation Parm. (lower) | | | | |
| | | | | | | PBL4 | PBL3 | PBL2 | PBL1 | PBL0 |
| 7 | XXH | W | X | X | X | Image area separation Parm. (upper) | | | | |
| | | | | | | PWL4 | PWL3 | PWL2 | PWL1 | PWL0 |
| 8 | XXH | W | X | X | X | Image area separation Parm. (diff.) | | | | |
| | | | | | | PD4 | PD3 | PD2 | PD1 | PD0 |
| 9 | XXH | W | Magnification/Reduction ratio | | | | | | | |
| | | | DUM7 | DUM6 | DUM5 | DUM4 | DUM3 | DUM2 | DUM1 | DUM0 |
| A | 00H | W | Clump Mode | Line clump enable | | | | | | |
| | | | | CLP6 | CLP5 | CLP4 | CLP3 | CLP2 | CLP1 | CLP0 |
| B | 00H | R/W | X | X | Offset correction value | | | | | |
| | | | | | OF5 | OF4 | OF3 | OF2 | OF1 | OF0 |
| C | 00H | R | X | Peak detection counter monitor | | | | | | |
| | | | | PEAK6 | PEAK5 | PEAK4 | PEAK3 | PEAK2 | PEAK1 | PEAK0 |
| D | FFH | R/W | X | Peak hold setting | | | | | | |
| | | | | PHR6 | PHR5 | PHR4 | PHR3 | PHR2 | PHR1 | PHR0 |
| E | 00H | W | X | Offset ref. pixel | | | White ref. | | Black ref. | |
| | | | | REF2 | REF1 | REF0 | VWHT1 | VWHT0 | VBLK1 | VBLK0 |
| F | XXH | W | X | Sensor pixel count | | | | | | |
| | | | | PIX6 | PIX5 | PIX4 | PIX3 | PIX2 | PIX1 | PIX0 |
| 10 | 00H | W | X | Dummy pixel count | | | | | | |
| | | | | DUM6 | DUM5 | DUM4 | DUM3 | DUM2 | DUM1 | DUM0 |
| 11 | XXH | W | Peak detection width (end) | | | | Peak detection width (start) | | | |
| | | | PKE3 | PKE2 | PKE1 | PKE0 | PKS3 | PKS2 | PKS1 | PKS0 |
| 12 | XXH | R/W | X | X | Access window | | | | | |
| | | | | | ACC5 | ACC4 | ACC3 | ACC2 | ACC1 | ACC0 |

| DMA Register | XXH | R | Image signal data | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | $VD_{N-7}$ | $VD_{N-6}$ | $VD_{N-5}$ | $VD_{N-4}$ | $VD_{N-3}$ | $VD_{N-2}$ | $VD_{N-1}$ | $VD_N$ |

1. □
   is reseted by $\overline{RESET}$.
2. , is enabled by TRIG↑ just after writing.

(1)R0 register

1. D0～D1 : Operation mode

| D1 | D0 | |
|---|---|---|
| 0 | 0 | : Scanning mode(reset) |
| 0 | 1 | : Black shading detect mode |
| 1 | 0 | : White shading detect mode |
| 1 | 1 | : Peak detect mode |

When R0/R7=1, operation will start in the first TRIG↑ after the command issued.

2. D2 : ABC enable

0 : ABC disable(reset)
1 : ABC enable
When R0/R7=1, operation will start in the first TRIG↑ after the command issued.

3. D3 : Memory access enable
It is possible to access sequentially to memory selected by R3/D4～D6.
In this mode, R0/R7 must be disabled.
0 : Disable(reset)
1 : Enable

4. D4 : Image processing enable

0 : Image processing stop(reset)
1 : Image processing execute

5. D5 : LEDC port control

0 : LEDC = 0(reset)
1 : LEDC = 1

6. D6 : Page start

0 : Normal operation(reset)
1 : Page start

7. D7 : Operation enable

0 : Disable(reset)
1 : Enable

(2)R1 register

1. D0 : ABCM

   0 : ABC mode (reset)
   1 : AGC mode

2. D1 : White side limitter enable

   Execute enable control of ABC white side limitter.
   0 : Disable (reset)
   1 : Enable

3. D2～D3 : ABC time constant

| D1 | D2 | | |
|---|---|---|---|
| 0 | 0 | : | 1/4 LSB |
| 0 | 1 | : | 1/2 LSB (reset) |
| 1 | 0 | : | 1 LSB |
| 1 | 1 | : | 2 LSB |

4. D4～D5 : Magnification ratio(Magnification with interpolation)

   Select magnification ratio .
   0 : 133%
   1 : 150% (reset)
   2 : 200%
   3 : Inhibit

5. D6 : Magnification with interpolation enable

   0 : Disable (reset)
   1 : Enable

6. D7 : Magnification/Reduction enable

   0 : Disable (reset)
   1 : Enable

(3)R2 register

1. D0～D3 : Bi-level slice level

Relationship between set value(N) and actual slice level of $N_S$ is shown below.

$N_S = 4 \times N + 3$ (N=0～15, reset:N=8)

2. D4～D5 : Image processing mode
(MTF correction Enable for character area is set by R2/D6)

| D5 | D4 | Image processing mode (reset) |
|---|---|---|
| 0 | 0 | Bi-level(Character:bi-level, Image:simple bi-level) |
| 0 | 1 | Dithering(Character:bi-level, Image:dithering) |
| 1 | 0 | Error diffusion A mode(Char:bi-level, Image:error diff) |
| 1 | 1 | Error diffusion B mode(All:error diffusion) |

3. D6 : MTF correction enable

0 : Disable (reset)
1 : Enable

4. D7 : $\gamma$ correction enable

0 : Disable (reset)
1 : Enable

(4)R3 register

1. D0～D2 : Internal RAM/Line memory bank select

| Memory | R3/D2 | R3/D1 | R3/D0 | R2/D5 | R3/D6 | R3/D3 | Contents | BA1 | BA0 |
|---|---|---|---|---|---|---|---|---|---|
| External | 0 | 0 | 0 | 0 | X | X | Black shading data | 0 | 0 |
| | | | | 1 | 0 | X | Black shading data | | |
| | | | | | 1 | 0 | Black shading data | | |
| | | | | | | 1 | Image data before for the previous line | | |
| | | 0 | 1 | X | X | X | White shading data | 0 | 1 |
| | | 1 | 0 | X | X | X | Image data for the previous line | 1 | 0 |
| | | 1 | 1 | 0 | X | X | Image data before for the previous line | 1 | 1 |
| | | | | 1 | X | X | Error data | | |
| Internal | 1 | 0 | 0 | X | X | X | Dithering pattern | - | - |
| | | 0 | 1 | X | X | X | $\gamma$ correction table | - | - |
| | | 1 | 0 | X | X | X | inhibited | - | - |
| | | 1 | 1 | X | X | X | inhibited | - | - |

2. D3 : Black correction type

0 : All pixel mode (reset)
1 : Offset cancel mode

If black correction type is set into '0' then image area detection and MTF correction windows are set 3×2, and set into '1' then windows set 3×3.

3. D4 : Bi-level data/6 bit data select

0 : Bi-level(reset)
1 : 6 bit

(5)R4 register

1. D0 : Sensor clock mode set

   0 : Mode A (reset)
   1 : Mode B

2. D1 : Line clump clock set

   0 : Mode A (reset)
   1 : Mode B
   This is available when R7/D6=0.

3. D2 : SP clock polarity select

   0 : active high(reset)
   1 : active low

4. D3 : FIFO clock mode select

   0 : mode A(reset)
   1 : mode B

5. D4 : White shading data use serial interface enable

   0 : disable(reset)
   1 : enable

6. D5 : TCLK/CKSH clock select

   0 : TCLK(reset)
   1 : CKSH

(6)R5 register

1. D0～D3 (ABC black side limitter)
   Black side limitter set register in ABC mode.

   Relationship between set value(N) and actual limitter value of $N_{LB}$ is shown below.
   $N_{LB}=8\times N(N=0\sim15)$

2. D4～D7 (ABC white side limitter)
   White side limitter set register in ABC mode.

   Relationship between set value(N) and actual limitter value of $N_{LW}$ is shown below.
   $N_{LW}=8\times N+3(N=0\sim15)$

(7)R6 register

1. D0～D4 : Image area separation parameter (lower)

Relationship between set value of N and actual parameter of $N_{PB}$ is shown below.
$N_{PB}=N(N=0\sim31)$
If the data is less than this value, data is judged character area(black).

(8)R7 register

1. D0～D4 : Image area separation parameter (upper)

Relationship between set value of N and actual parameter of $N_{PW}$ is shown below.
$N_{PW}=N+32(N=0\sim31)$
If the data is more than this value, data is judged character area(white).

(9)R8 register

1. D0～D4 : Image area separation parameter (differential)

Relationship between set value of N and actual parameter of $N_{PD}$ is shown below.
$N_{PD}=N(N=0\sim31)$
If the data is more than this value, data is judged character area.

(10)R9 register (Magnify/Reduction rate set register)

D0～D7 : Magnify/Reduction rate set(1/100～200/100)

Set numerator value in normal magnification/reduction mode.

(11)RA register

1. D0～D6 : Line clump enable set
Set line clump enable falling edge timing in line clump mode.
Relationship between set value of N and actual falling edge CLP is shown below.
CLP↓=N+1(N=0～127, reset:N=0)

2. D7 : Clump mode

0 : Line clump (reset)
1 : Bit clump

(12)RB register (Offset correction value register)

In the case to use offset cancel mode, correction value which is correspond with reference pixel set other register is stored to execute black distortion detection.

(13)RC register (Peak detection counter monitor register)

Read peak detection counter value.

(14)RD register (Peak hold set register)

Set peak value into peak hold register through this register.

(15)RE register

1. D0～D3 (White/Black reference register)

Set white reference voltage(VWHT) and black reference(VBLK) using full scale of $V_{PEAK}$-$V_{CLP}$.
Resolution is 0.25×1/4, and actual value of coefficient($\alpha$, $\beta$) is calculated following way.
These set values are available in read mode.

$V_{WHT}=V_{CLMP}(1.25V\ typ.)+\alpha\times(V_{PEAK}-V_{CLMP})$
$V_{BLK}=V_{CLMP}(1.25V\ typ.)+\beta\times(V_{PEAK}-V_{CLMP})$
$V_{CLP}$:Clump voltage, $V_{PEAK}$:Signal peak voltage

| Set value | $\alpha$ | $\beta$ |
|---|---|---|
| 0 | 1.000 | 0.000 |
| 1 | 0.917 | 0.083 |
| 2 | 0.833 | 0.167 |
| 3 | 0.750 | 0.250 |

2. D4～D6 : Black reference pixel register

In the case to execute black correction with offset cancel mode, set reference pixel to take correction value. It is possible to set by 16pixel unit.

Relationship between set value of N and actual reference pixel position B is shown below.

B = 16×(N+1) (N=0～7)

It will be counted another counter from dummy counter, in the case to set more than dummy number, it is possible to set into available pixel.

(16)RF register (Reading pixel number register)

Set available sensor pixel number by 32 pixel unit. It doesn't include dummy pixel.
Maximum value is 4096 pixel.
Relationship between set value of N and available pixel number S is shown below.

S=32×(N+1) (N=0～127)

(17)R10 register (Before dummy pixel number set register)

Set before dummy pixel number of sensor by 1 pixel unit.
Relationship between set value of N and actual pixel number D is shown below.

D=N (N=0～127)

(18)R11 register (Peak detection start width set register)

1. D0～D3 : Peak detection width set (START)
Set peak detection width(PHEW). Start pixel is set by 256 pixel unit. It doesn't include dummy pixel.
Relationship between set value of N and start pixel position PS is shown below.

PS=256×N (N=0～15)

2. D4～D7 : Peak detection width set (END)
Set peak detection width(PHEW). End pixel is set by 256 pixel unit. It doesn't include dummy pixel.
Relationship between set value of N and start pixel position PE is shown below.

PE=256×(N+1) (N=0～15)>PS

(19)R12 register (Line memory/Internal RAM access register)

(20)DMA register

In the case to output bi-level data in parallel mode by 8 pixel unit, you should access this register.
The oldest data is stored MSB and the latest data is stored LSB.
It is needed to use DMA controller in 1-byte transfer mode.