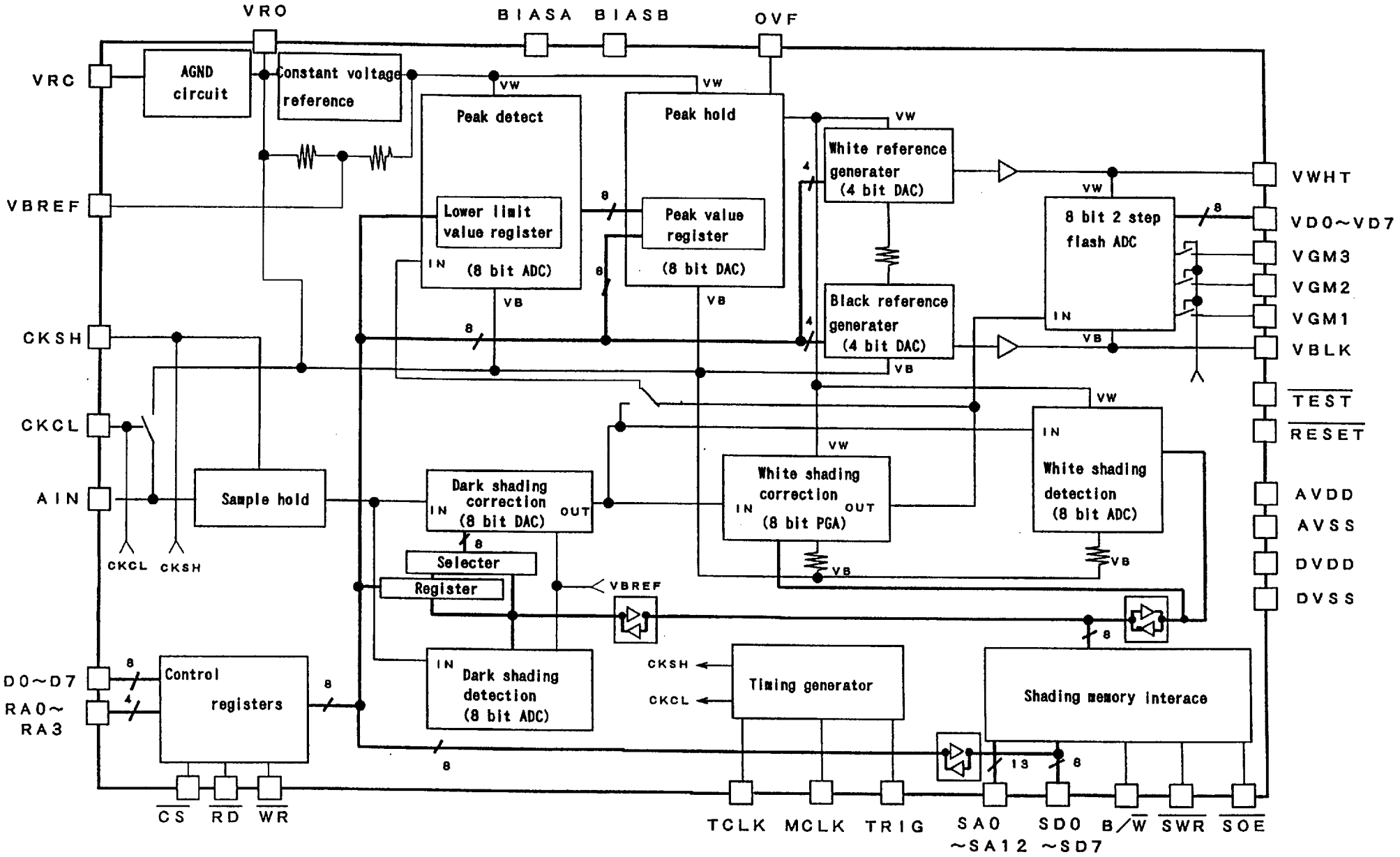
AKM

AK8406

Shading Correction LSI for 256 gray scale

Features

- ☐Shading correction LSI for CCD/CIS sensor
- ☐Input signal level: 250mVp-p～1.15Vp-p
- ☐Processing speed : 5M sample/sec
- ☐Max.sensor length : 8184
- ☐Sample hold and clump circuit included
- ☐8bit 2step flash ADC included
  - •Contrast adjustment possible by 2×4bit DAC, which are volumes for black reference voltage and for white reference voltage of ADC.
  - . γ correction possible by changing ADC conversion characteristics to logarithmic one (by 3 intermidiate tap pins of ADC)
- ☐8 bit ADC(detector) and analog multiplier(corrector) for white shading
  - •Pixel to pixel correction(External memory needed)
  - •External memory access possible through AK8406
  - •Correction range:up to 50%(actual correction resolution ia 9 bit)
- ☐8 bit ADC(detector) and analog adder(corrector) for black shading
  - •Pixel to pixel correction (external memory needed)
  - •Balansing DC level between even pixels and odd pixels(No external memory needed)
  - •Internal amplifier offset and switch feed-through cancelled simultaneously
  - •External memory accsess(R/W) possible through AK8406
  - •Internal registers access(R/W) possible
- ☐8 bit peak detector(ADC) and 8bit peak hold(DAC)
  - •Automatic gain control and automatic background control use
  - •Detect dinamic range programmable
  - •detect period (which part or the line sensor) programmable
  - •Internal register(peak value) accsess(R/W) possible
- ☐Constant voltage reference included
- ☐CMOS monolithic LSI
- ☐5V single power supply (5V±5%)
- ☐80pin QFP


VRO
BIASA
BIASB
OVF
VRC
AGND circuit
Constant voltage reference
VBREF
Peak detect
Peak hold
Lower limit value register
(8 bit ADC)
Peak value register
(8 bit DAC)
White reference generater (4 bit DAC)
Black reference generater (4 bit DAC)
8 bit 2 step flash ADC
VWHT
VD0~VD7
VGM3
VGM2
VGM1
VBLK
TEST
RESET
AVDD
AVSS
DVDD
DVSS
CKSH
CKCL
AIN
Sample hold
Dark shading correction (8 bit DAC)
White shading correction (8 bit PGA)
White shading detection (8 bit ADC)
Selecter
Register
VBREF
Dark shading detection (8 bit ADC)
Timing generator
Shading memory interace
D0~D7
RA0~RA3
Control registers
CS
RD
WR
TCLK
MCLK
TRIG
SA0 ~SA12
SD0 ~SD7
B/W
SWR
SOE

General Discription

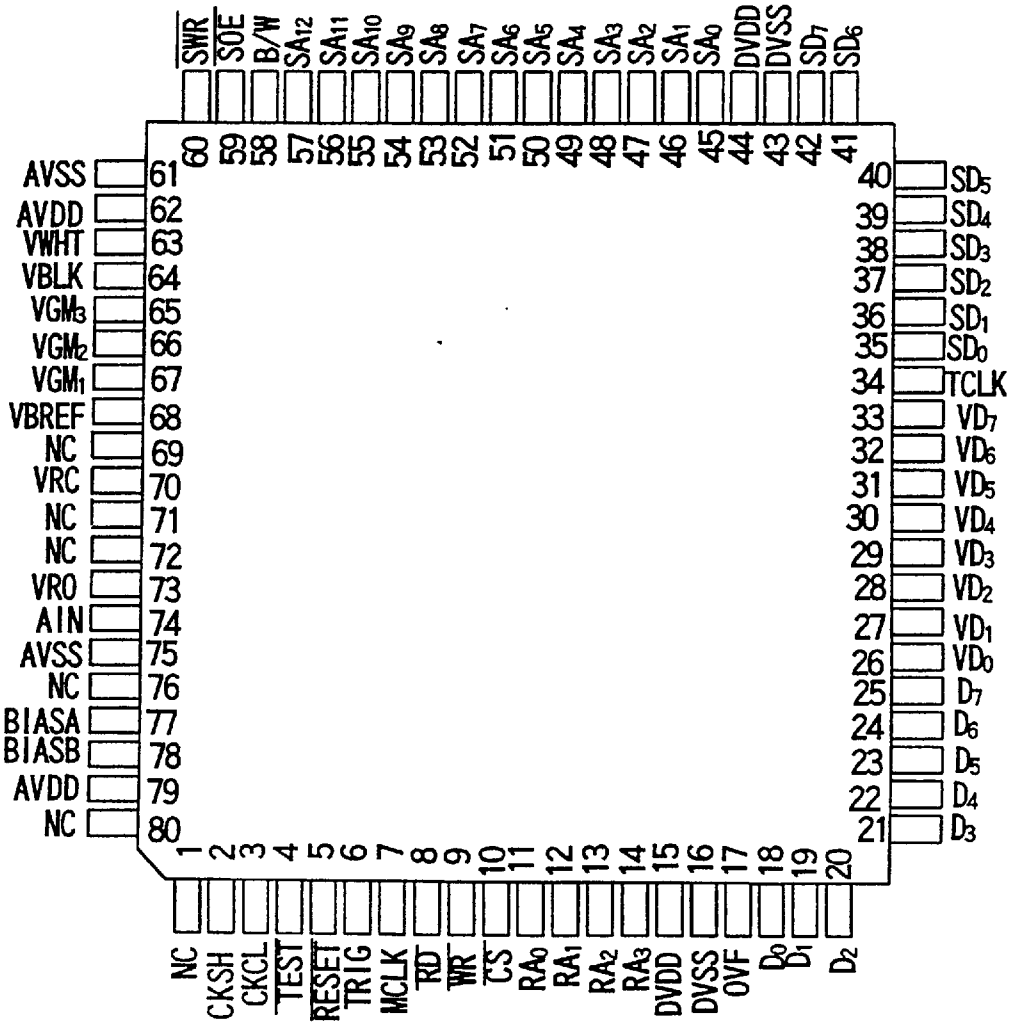
(1) AK8406 is a single chip, 5MS/s ADC with shading correction function, which produces 256 gray shade image from CCD or CIS.

(2) Because that AK8406 normalizes CCD or CIS output at the analogous stage, and produces 256 gray shade image, output grey levels doesn't decrease by shading correction.

(3) Shading correction functions of AK8406 are white shading correction, black shading corr -ection, AGC by peak hold, γ correction, contrast adjustment etc.

(4) AK8406 integrates clump and sample hold, shading correction functions above mentioned, , 2 step flush ADC, and programable shading memory address generator and so on.
No need of external components and adjustments at the mass production stage.

Pinouts



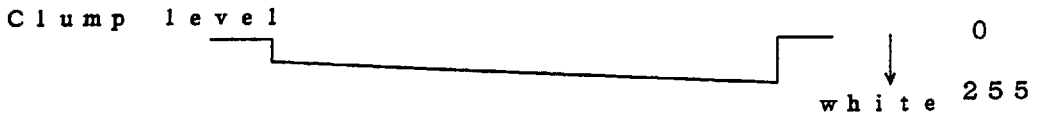
Pin Description

Pin Number	Pin Name	I/O	Function
			Power Supply Pins
15, 44	DVDD(2)	–	Digital power supply pins (5V typ)
16, 43	DVSS(2)	–	Digital VSS
62, 79	AVDD(2)	–	Analog power supply pins (5V typ)
61, 75	AVSS(2)	–	Analog VSS
			Analog Pins
74	AIN	I	Analog input pin. External capacitor for clump is necesarry.
77	BIASA	I	Bias current setting pin. Connect 10kΩ(±5%) between BIASA and VRO.
78	BIASB	I	Bias current setting pin. Connect 1kΩ(±5%) between BIASB and AVSS.
73	VRO	O	Clump or anlog ground voltage buffer output. (2.75V typ.)External capacitor is necessary.
70	VRC	O	Clump or anlog ground voltage non-buffer outpu-t.(2.75V typ.)External capacitor is necessary
68	VBREF	O	Reference voltage buffer output for black shad-ing detect/correction circuit(2.45V typ.) Full scale voltage is VRO(2.75V)-VBREF(2.45V)
63	VWHT	O	White-side reference voltage buffer output of 8 bit 2-step flash ADC.
64	VBLK	O	Black-side reference voltage buffer output of 8 bit 2-step flash ADC.
67, 66, 65	VGM1, VGM2 VGM3	I	Reference voltage inputs for 8 bit 2-step flash ADC γ correction use.

Pin number	Pin name	I/O	Function
Micro-computer interface			
19~25	D0~D7	I/O	System data bus pins. (3 state)
9	$\overline{WR}$	I	Write signal.
8	$\overline{RD}$	I	Read signal.
10	$\overline{CS}$	I	Chip select signal.
11~14	RA0~RA3	I	Address inputs for internal registers.
Clock and output signals			
7	MCLK	I	Master clock input. Freq. is multiplied data rate by 4.
2	CKSH	0	Sample hold control signal moniter output.
3	CKCL	0	Clump control signal moniter output.
6	TRIG	I	Line start signal input. (Edge triger) Phase synchronization of clocks(CKSH, CKCL etc), initializing counters, and start of operation are occurred by rizing edge of TRIG.
26~33	VD0~VD7	0	8 bit video data outputs.
34	TCLK	0	Clock output for VD0~VD7. AK8406 outputs VD0~VD7 by falling edge of this clock.
17	OVF	0	Overflow output of peak detect citcuit. When signal level becomes over 1.2V(typ.), this signal becomes active.
Shading Memory Interface			
35~42	SD0~SD7	I/O	Shading memory data bus pins. (3 state)
45~57	SA0~SA12	0	Shading memory address output pins.
58	B/W	0	Shading memory black/white bank select output pin.
59	$\overline{SOE}$	0	Shading memory read signal output pin.
60	$\overline{SWR}$	0	Shading memory write signal output pin.
Other pins			
5	$\overline{RESET}$	I	Reset signal input pin.
4	TEST	I	Test pin. Pull up to 'H' level normally.

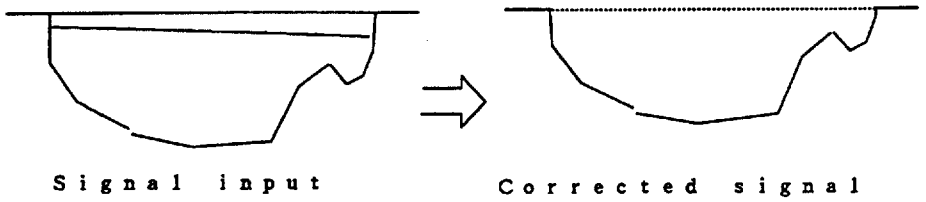
Polality/output codes of internal ADC/DACs

(1) Black shading detection use ADC/correction use DAC



AS the above figure, the signal input is larger, that is, the signal is closer to the white end, the output code of detection use ADC becomes larger in the black shading detect mode.

In the peak detect mode, white shading detect mode and the document read mode, the code is larger, the subtracted voltage generated by the correction use DAC is larger.

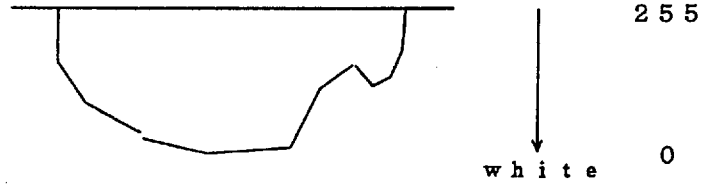


(2) Peak detect use ADC/peak hold use DAC

AS the above figure, the signal input is larger, that is, the signal is closer to the white end, the output code of detection use ADC is smaller in the peak detect mode.

In the white shading detect mode and the document read mode, the code is smaller, the output voltage of peak hold use DAC is closer to the white end.

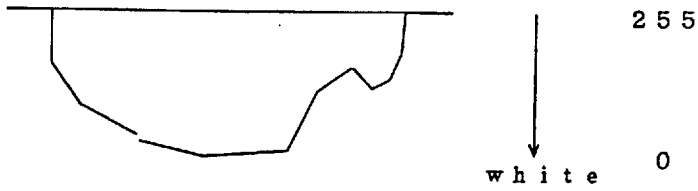
(3) White shading detection use ADC/correction use PGA



AS the above figure, the signal input is larger, that is, the signal is closer to the white end, the output code of detection use ADC is smaller in the white shading detect mode.

In the document read mode, correction use PGA operates division operation .

(4) 2 step flush ADC



AS the above figure, the signal input is larger, that is, the signal is closer to the white end, the output code of detection use ADC is smaller in the document read mode.

Registers

address (HEX)	OPE	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	X	W (R)	operation enable (Read possible)	Shading memory accsess control	Operation mode		Black correction type	Peak detect enable	Black/white memory bank select	γ correction enable
1	0	R/W	Peak register							
			PH7	PH6	PH5	PH4	PH3	PH2	PH1	PH0
2	X	W	Peak AGC range							
			PL7	PL6	PL5	PL4	PL3	PL2	PL1	PL0
3	X	W	Flush ADC white reference				Flush ADC black reference			
			VWHT3	VWHT2	VWHT1	VWHT0	VBLK3	VBLK2	VBLK1	VBLK0
4	0	R/W	DC balance data register(Even)							
			EO7	EO6	EO5	EO4	EO3	EO2	EO1	EO0
5	0	R/W	DC balance data register(Odd)							
			OO7	OO6	OO5	OO4	OO3	OO2	OO1	OO0
6	X	W	Clump pulse width(bit clump)	Clump mode	Sensor pixel counts(upper 2)		Peak detect period start(upper 2)		Peak detect period end(upper 2)	
					SL9	SL8	PS9	PS8	PE9	PE8
7	X	W	Sensor pixel counts(lower 8)							
			SL7	SL6	SL5	SL4	SL3	SL2	SL1	SL0
8	X	W	Peak detect period start(lower 8)							
			PS7	PS6	PS5	PS4	PS3	PS2	PS1	PS0
9	X	W	Peak detect period end(lower 8)							
			PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0
A	X	W	X					Black shading correction reference pixel		
								BR2	BR1	BR0
B	X	W	Pre-dummy pixel counts							
			DUM7	DUM6	DUM5	DUM4	DUM3	DUM2	DUM1	DUM0
C	0	R/W	Shading memory accsess window register							
			SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0

1. OPE=operation enable(R0/D7)
2. □ shows the bits which can be initialized by RESET.
3. ▒ shows the bits which becomes effective by TRIG.

(1) R0 register

1. D0 : γ correction enable

0 : Disable
1 : Enable

This bit controls the analog switch of γREF1～γREF3 reference inputs. In the disable state, 2 step flush ADC characteristics is linear. In the enable state, 2 step flush ADC characteristics is folded by 3 reference voltage(γREF1～γREF3). $\overline{\text{RESET}}$ sets this bit to disable state.

2. D1 : Shading memory bank(B/W) control

0 : B/W port=0(White)
1 : B/W port=1(Black)

This bit controls the shading memory bank(Black or White) only in the shading memory accsess mode. In the normal operation modes, this bit isn't effective.

3. D2 : Peak detect enable

0 : Disable(hold state)
1 : Enable

Only in the document read mode and white shading detect mode, this bit controls the peak detect operation. In the black shading detect mode, peak detect function is automatically disabled. And in the peak detect mode, this function is automati-cally enabled. $\overline{\text{RESET}}$ sets this bit to disable state.

The input into the peak detect circuit is automatically controlled by each ope-ration mode, that is. That is, in the peak detect mode and white shading detect mode, the input is the clumped sensor input after only black shading corrected, and in the document read mode, that is normalized sensor input after both black and white shading corrected.

In the state that this bit is set to the enabled, the detected 8 bit peak data of each line detected by peak detect circuit is automatically loaded to the peak hold circuit(R1 register) at the line-end timing. In the disabled state that this bit is set to the disabled, this load operation is inhibitted and the peak hold(DAC) holds the constant voltage according to the contents of R1 regis-ter.

The peak detect period is controlled by the R6, R8, R9 registers.

When the input exeeds the specified voltage(that is, white-side maximum input amplitude, 1.2V typ.), OVF becomes 'H' state. This signal is cleared at the line-end timing.

4. D3 : Black shading detect/correction type

0 : pixel to pixel
1 : odd even balance

With pixel to pixel correction type, the DC level deviation among every pixel can be corrected. The corretion data are stored in the external RAM.
With the odd/even balance correction type, the DC level difference between odd pixels and even pixels can be corrected. The correction data are stored in the internal registers. When this type of correction is selected, no external RAM needed.

5. D4~D5 : Operation mode

D5	D4		
0	0	:	Document read mode
0	1	:	Black shading detect mode
1	0	:	White shading detect mode
1	1	:	Peak detect mode

With the condition of R0/D7(Operation enable)=1, the first TRIG after that each mode is set starts the actual operation.

6. D6 : Shading memory accsess enable

0 : disable
1 : enable

With the condition of R0/D7(Operation enable)=0, the external shading memory can be accsessed through the RC window register.
By the 0→1 change of this bit, the internal address counter is initialized, and after that the counter is automatically incremented by the each accsess to the RC register.
$\overline{\text{RESET}}$ sets this bit to disable state.

7. D7 : Operation enable/Busy flag(W/R)

0 : disable/Ready
1 : enable/Busy

For executiong the operation modes, which is defined by R0/D4~D5, this bit must be set to the enable state. For accessing to the some registers, this bit must be set to the disable state.
In the each mode except the document read mode, that is, the black shading detect mode, the white shading detect mode, and the peak detect mode, this bit is automatically cleared to 0 by the operation completion, and AK8406 goes to the idling state.
The necessary line count for executing each mode are 2 for odd/even balance type of the black shading detect mode, 16 for pixel to pixel type, 16 for white the shading detect mode, and 1 for the peak detect mode.
This bit can be read as the BUSY flag. $\overline{\text{RESET}}$ sets this bit to disable state.

(2) R1 register(Peak register)

In the peak detect mode and the white shading detect mode/the document read mode with peak detecd enabled, the contents of this register is automatically renewed with the new peak value, detected by the peak detect circuit(ADC) at the line-end. The contents of this register corresponds to the output voltage of peak hold circuit(DAC).

The contents of this register can be read or written.

$\overline{\text{RESET}}$ or execution of black detect mode sets this register to the 0.

(3) R2 register(Peak AGC range register)

The contents of this register corresponds to the lower(black-side) limit of peak AGC range, that is, this parameter limits the output code of the peak detect(ADC). The upper limit(white-side) is 0 code.

In the peak detect mode and white shading detect mode/document read mode with peak detecd enabled, the contents of this register is effective.

If actually detected peak code(8 bit, 0:white-end, 255:black-end) is larger than the contents of this register, not the detected code but the contents of this register is loaded to the peak register(R1). The contents of this register is set to 0 by $\overline{\text{RESET}}$ signal.

(4) R3 register(white voltage reference and black voltage reference of flush ADC)

Upper nibble and lower nibble each sets white reference voltage(VWHT) and black reference voltage(VBLK) of flush ADC as the percentage of the fullscale(peak voltage-clump voltage). The resolution is 25%×1/16. Actual value is as the table.

code	VWHT	VBLK
F	0.776	0.000
E	0.781	0.016
D	0.797	0.031
C	0.813	0.047
B	0.828	0.063
A	0.844	0.078
9	0.859	0.093
8	0.875	0.109
7	0.891	0.125
6	0.906	0.141
5	0.922	0.156
4	0.938	0.172
3	0.953	0.188
2	0.969	0.203
1	0.984	0.219
0	1.000	0.234

(5) R4 register(DC level balance data register/for even pixels)

When odd/even balance type of black shading detect/correction is selected, 8 bit DC level balance data which corresponds to the even pixels is stored in this register by black shading detect mode execution.
Which pixel is used for reference pixel is defined by RA register.
In the peak detect mode , the white shading detect mode, and the document read mode with odd/even DC level balance type of correction is selected, the contents of this register corresponds to the voltage subtracted from input signal.
The contents of this register can be read or written.
When pixel to pixel type of black shading detect/correction is selected, 8 bit black shading data which corrects differences among the every pixel are stored in the external SRAM.
Note that which corresponds to the internal DC offset of AK8406 is also included in this code.

(6) R5 register(DC level balance data register/for odd pixels)

This register has the same function for odd pixels with R4 register.

(7) R6 register

1. D6 : clump method
   0 : bit clump
   1 : line clump
   Clump method can be selected by this bit. Please refer to the FIG1 in detail.
   Once the clump mode is set, the constant clump pulse continues to output independe -ntly with the operation enable state or the operation modes.
   $\overline{\text{RESET}}$ signal sets bit clump mode.

2. D7 : clump pulth width(effective only in the bit clump mode)
   0 : MCLK×1
   1 : MCLK×1/2

(8) R6 register(D4, D5), R7 register:sensor pixel counts register

The available pixel counts can be set by these registers with 8 pixel unit.
Pre-dummy pixels count is not included. Maximum counts is 8184.
If setting code is N, actual available pixels count S is as the below equation.

$$S = 8 \times N \quad (N = 1 \sim 1023)$$

(9) R6 register(D2, D3), R8 register:Peak detect piriod start pixel register

This register sets the start pixel of peak detect piriod by 8 pixel unit.
Pre-dummy pixels count is not included.
If setting code is N, actual start pixel PS is as the below equation.

$$PS = 8 \times N \ (N = 0 \sim 1023)$$

(10) R6 register(D0, D1), R9 register: Peak detect piriod end pixel register

This register sets the end pixel of peak detect piriod by 8 pixel unit. Pre-dummy pixels count is not included.
If setting code is N, actual end pixel PE is as the below equation.

$$PE = 8 \times N \ (N = 1 \sim 1023) > PS$$

(11) RA register

D0~D2 : Black correction reference pixel register

When odd/even balance type of black shading detect/correction is selected, actual reference pixel within pre-dummy pixels can be set by this register with 8 pixel unit.
If setting code is N, actual reference pixel B is as the below equation.

$$Bodd = 8 \times N + 1 < D \text{ (pre-dummy pixels count)} \ (N = 0 \sim 7)$$
$$Beven = 8 \times N + 2 < D \text{ (pre-dummy pixels count)} \ (N = 0 \sim 7)$$

(12) RB register(Pre-dummy pixels count register)

Pre-dummy pixels count can be set by this register with 1 pixel unit.
If setting code is N, actual pre-dummy pixel counts D is as the below equation.

$$D = N + 2 \ (N = 0 \sim 255)$$

(13) RC register(Shading memory accsess window register)

External shading memory can be accessed through this register. Before actual acce-ss, R0/D7(operation enable) must be set to 0 state, R0/D6(shading memory access en-able) must be changed 0→1 for address counter initializing.
After that the address counter is automatically incremented by each $\overline{RD}$, $\overline{WR}$ signal for RC register, shading memory can be sequencially accessed. Continue to access the memory until the access count reachs to the pixels count set by R6/R7 registe-rs.
Which bank(black or white) is accessed is controlled by R0/D1.

Operation mode/timing

Especially shading memory access timing of each mode operation is changed by which type of black shading detect/correction is selected. Nessesary shading memory access time is also changed. Refer FIG1~FIG9 and AC timing specifications.
In the each mode except shading memory access mode, by the first TRIG after operation mode and operation enable are set, actual operation begins. And in the each mode except document read mode, BUSY flag is reset and AK8406 goes to the idling after operation com-pleted.
In the document read mode, black/white shading corrected 8 bit video signal outputs syncronized with falling edge of the TCLK.
Control registers' setting and timings are described in the following pages.

R0 register / pins / Modes	operation mode control		operation enable	shading memory access enable	shading memory bank select	black shading type select	operation start	operation status (BUSY)	peak detect enable	γ correction enable
	D5	D4	D7	D6	D1	D3	pins	(D7)	D2	D0
document read	0	0	1	0	X	0/1	TRIG	X	0/1	0/1
black shading detect •odd/even balance •pix to pix	0	1	1	0	X	1 0	TRIG	effective	automatically disabled	X
white shading detect	1	0	1	0	X	0/1	TRIG	effective	0/1	X
peak detect	1	1	1	0	X	0/1	TRIG	effective	automatically enabled	X
shading memory access •black bank •white bank	X	X	0	1	1 0	X	$\overline{RD}/\overline{WR}$	X	X	X

X:Don't care or ineffective

Registers / Modes	peak value	peak AGC range	flush ADC balck/ white ref.	odd/even DC level balanc data	peak detect period	ref.pix for black correc-tion data	sensor line length	shadin-g memory window
	R1	R2	R3	R4, R5	R6, 8, 9	RA	R6, R7	RC
document read	auto. renew when PDE(R0/D2)=1	effect-ive when PDE(R0/D2)=1	effect-ive	effect-ive when R0/D1=1	effect-ive when PDE(R0/D2)=1	X	effect-ive	X
black shading detect	reset to 0	X	X	effect-ive when R0/D1=1	X	effect-ive when R0/D1=1	effect-ive when R0/D1=0	X
white shading detect	auto. renew when PDE(R0/D2)=1	effect-ive when PDE(R0/D2)=1	X	effect-ive when R0/D1=1	effect-ive when PDE(R0/D2)=1	X	effect-ive	X
peak detection	auto. renew	effect-ive	X	effect-ive when PDE(R0/D1)=1	effect-ive	X	effect-ive	X
shading memory access	X	X	X	X	X	X	X	effect-ive

X: Don't care or ineffective

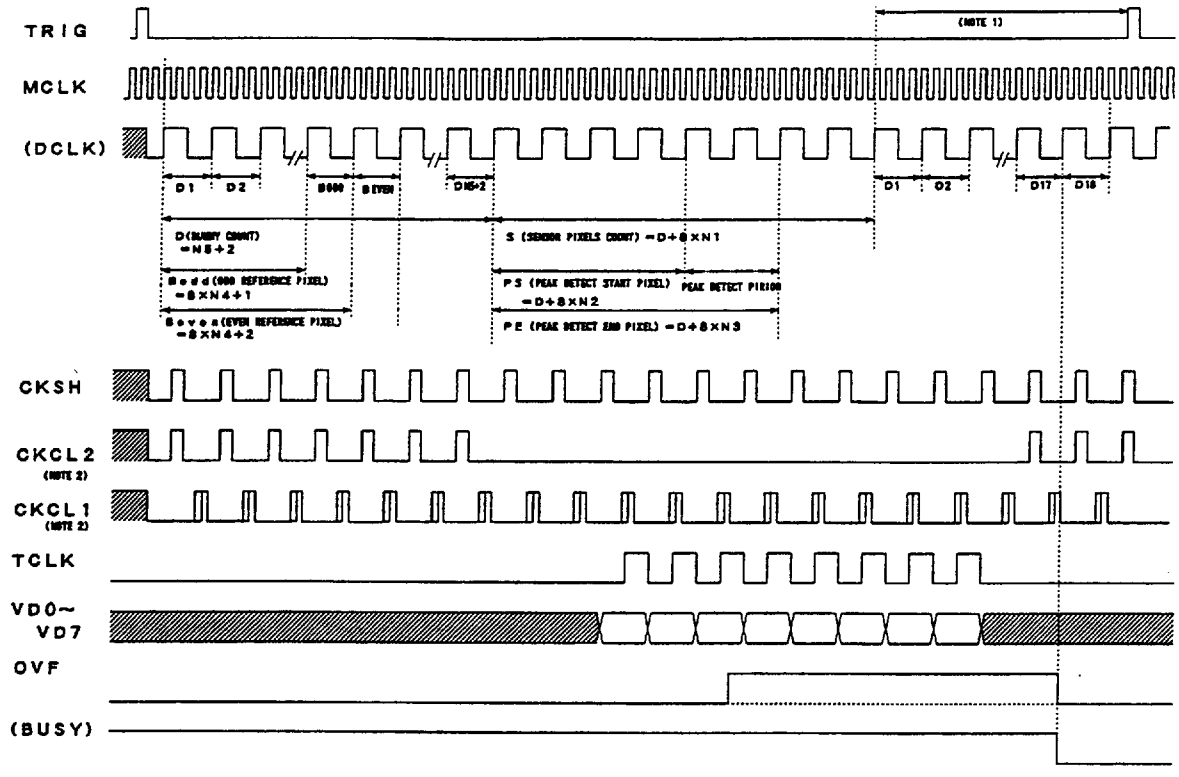


Fig1 Registers setting and clocks timing

(note 1)

1. Bit clump

Sensor integral time, that is TRIG pulse period, must be {PRE-DUMMY COUNTS(D)+SENSOR PIXELS COUNT(S)+18}×4/MCLK at minimum.

(ex.)

When MCLK is 20MHz(Data sampling rate=5MHz), and the sensor, which pixels count=4864, pre-dummy pixels count=128, is used

Minimum integral time=(128+4864+18)×4/20M=1.02mS

2. Line clump

Clump is done during the blanking period.

The necessary capacitor value and integral time must be calculated by discha-rge from sample hold in the available pixels piriod, and charge in the clump piriod.

(NOTE 2) CKCL1 is the clump pulse in the bit clump mode. CKCL2 is the clump pulse in the line clump mode.

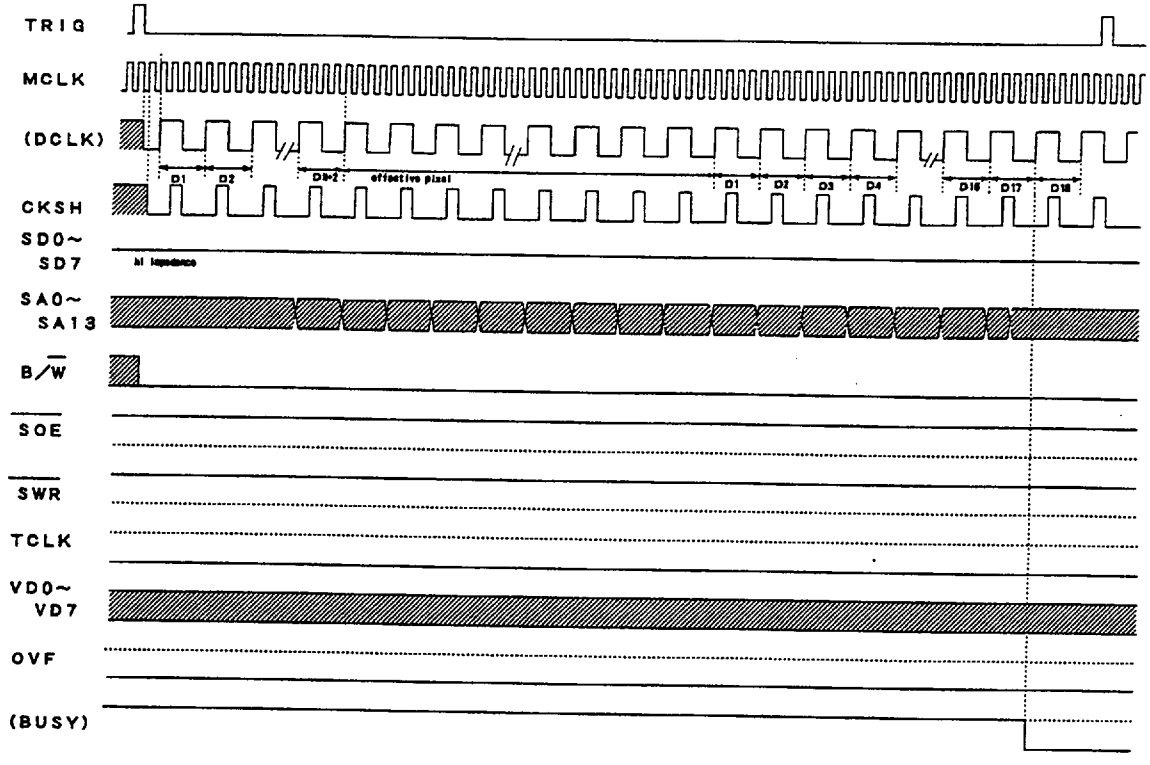


FIG2 Black shading detect mode(odd/even balance type)

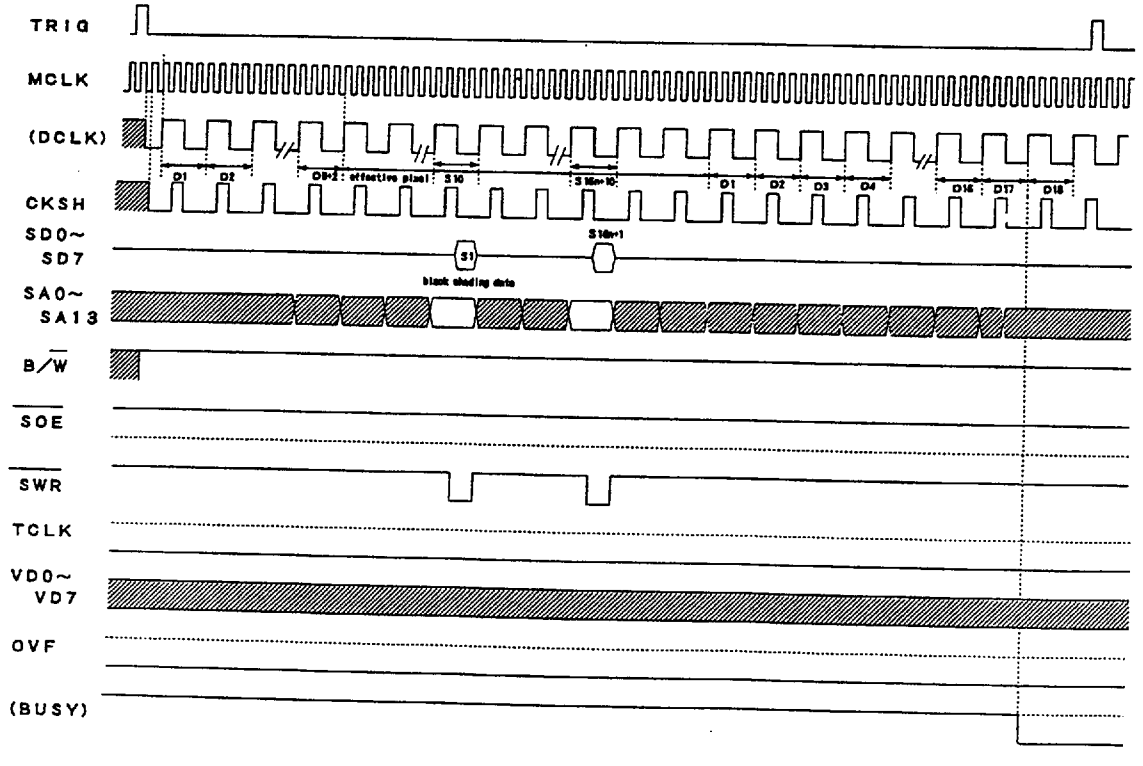


FIG3 Black shading detect mode(pixel to pixel type)

0983635 0001291 893

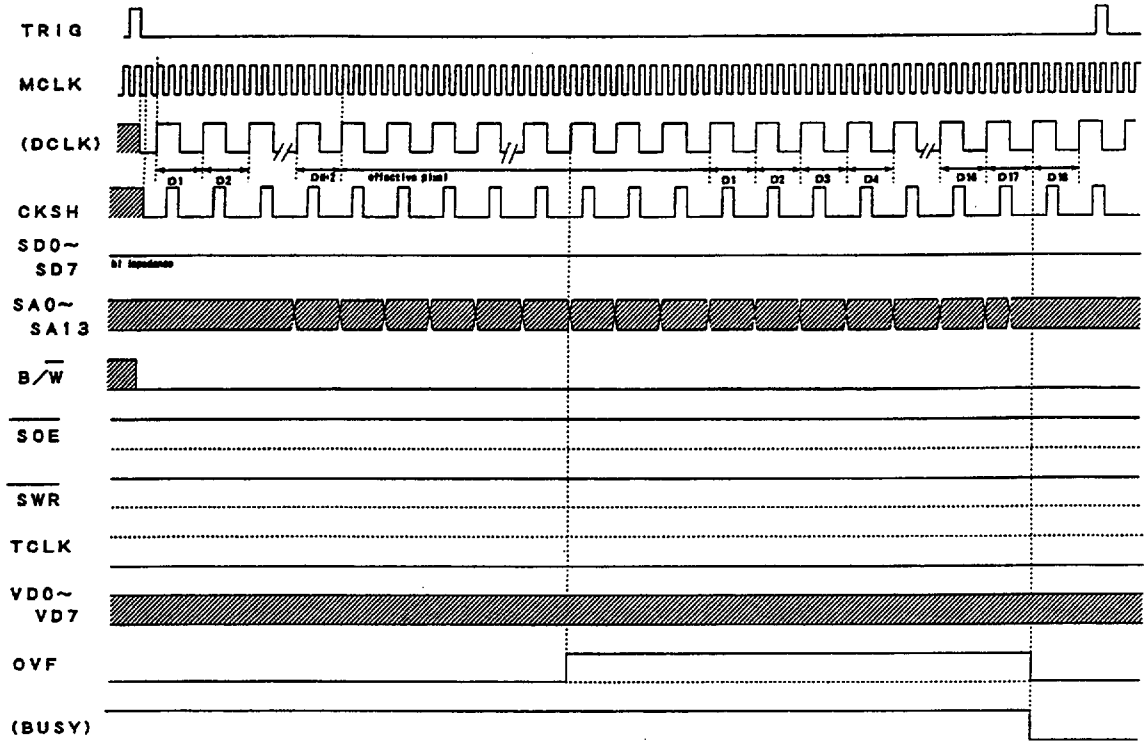


FIG 4 Peak detect mode(odd/even balance type black correction)

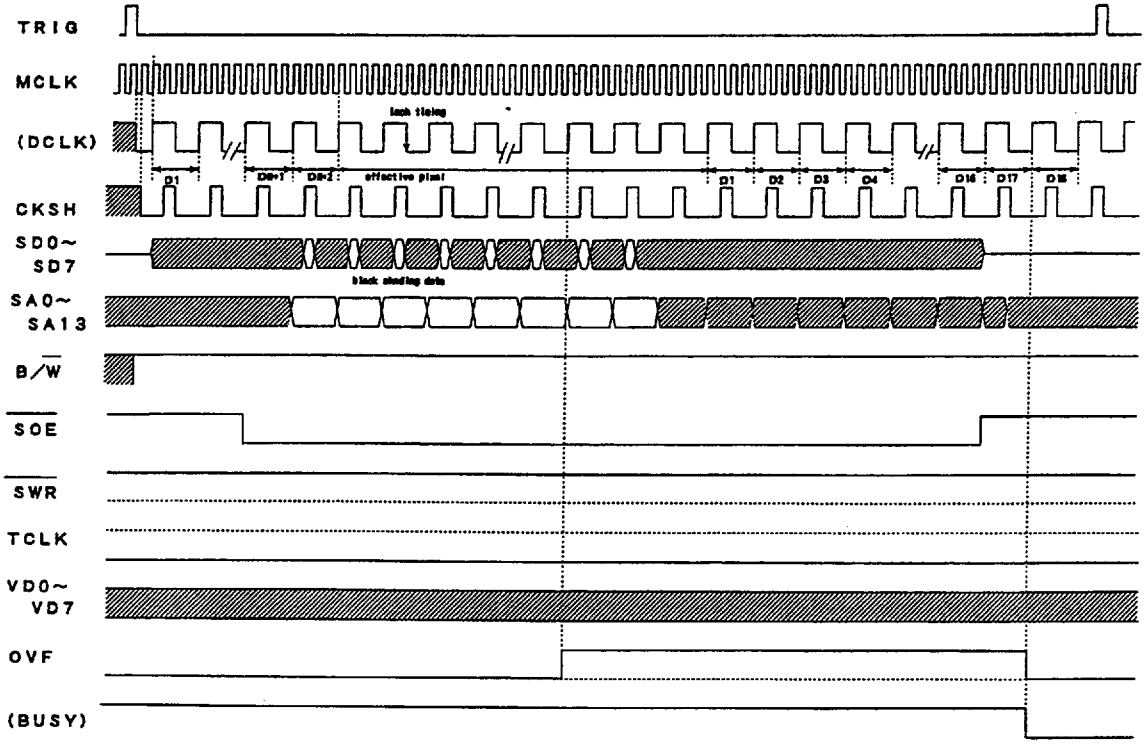


FIG 5 Peak detect mode(pixel to pixel type black shading correction)

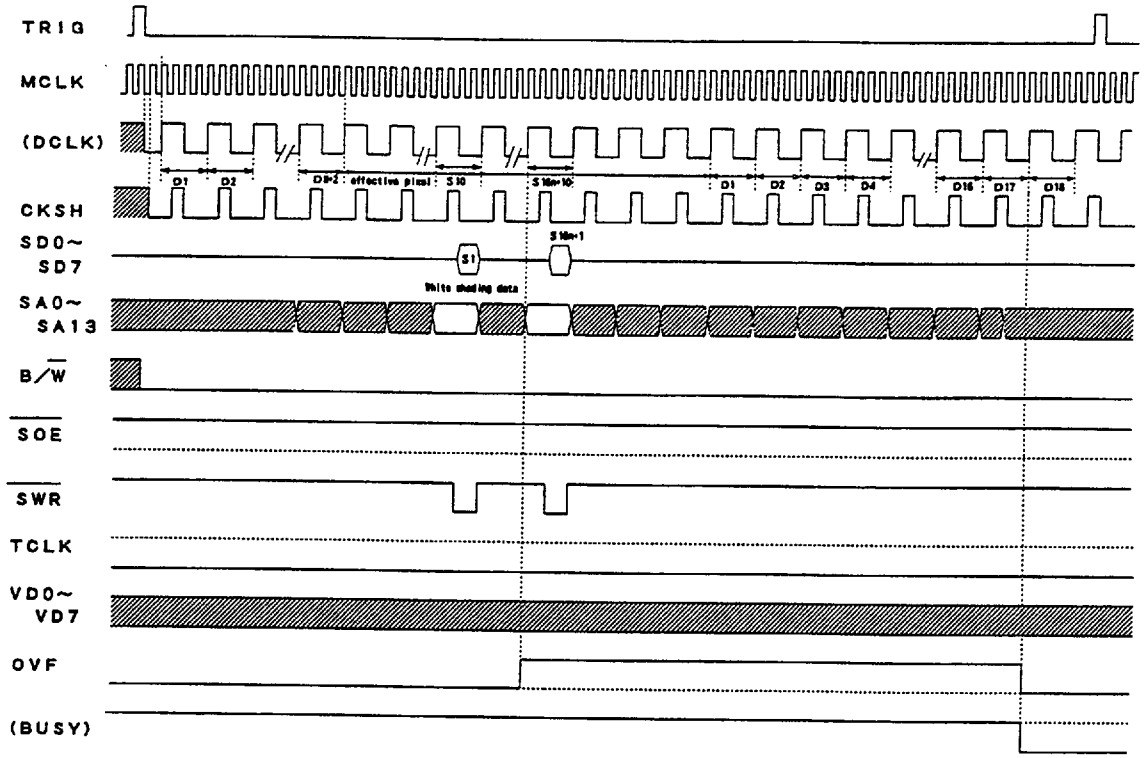


FIG 6 White shading detect mode(odd/even balance type black correction)

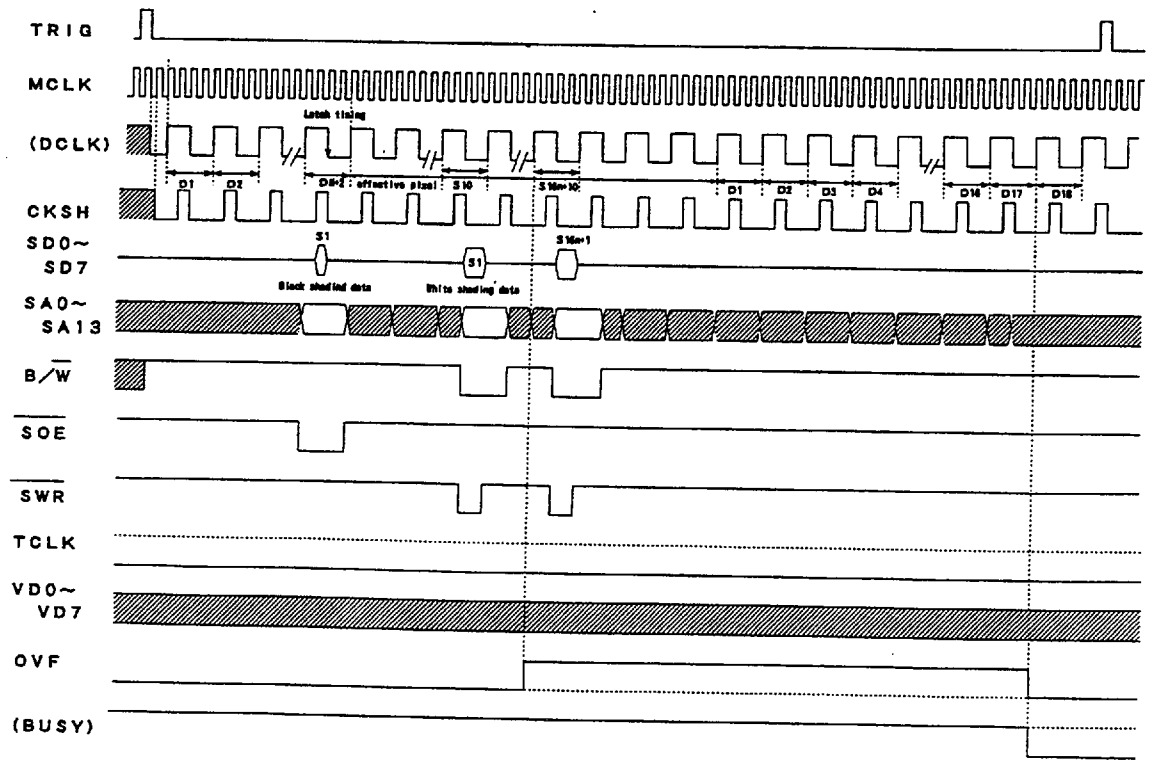


FIG 7 White shading detect mode(pixel to pixel type black shading correction)

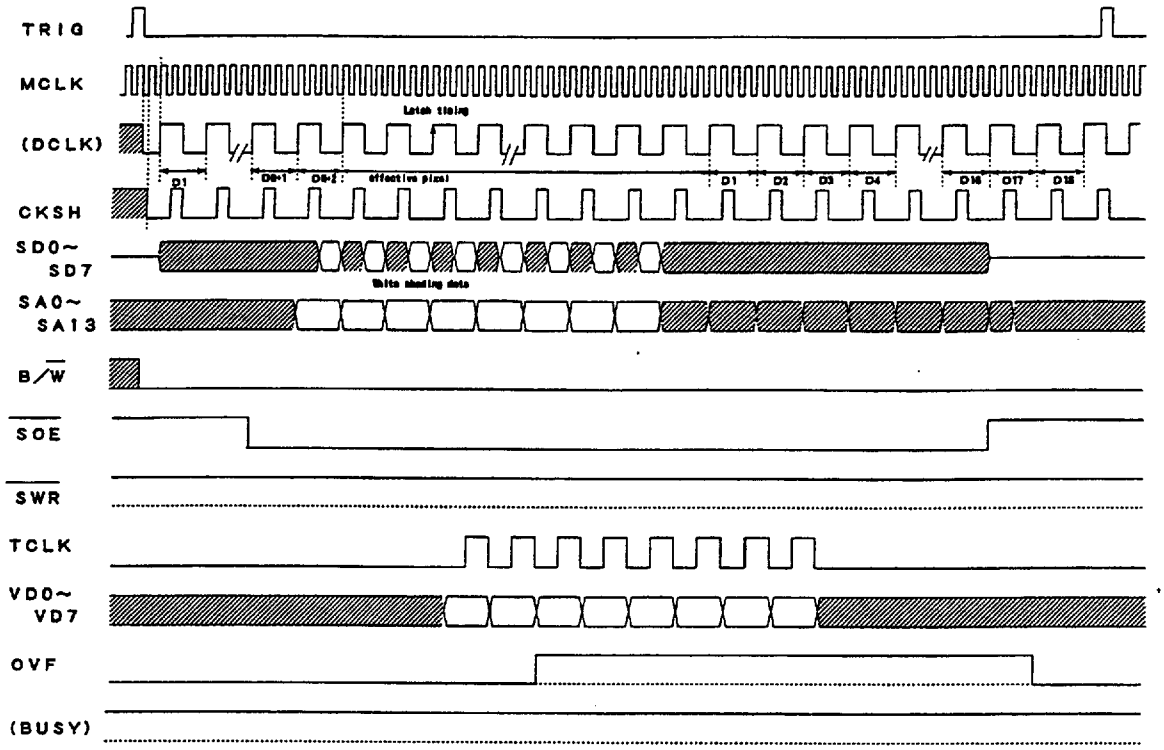


FIG 8 Document read mode(odd/even balance type black correction)

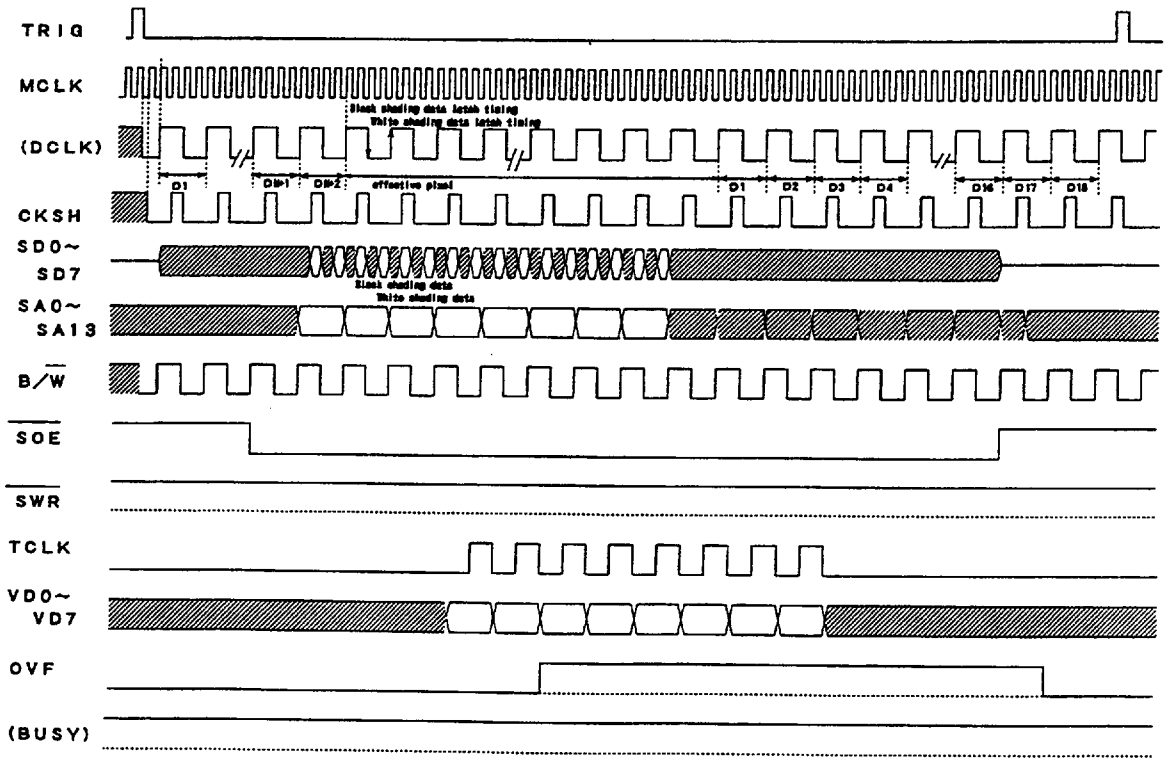


FIG 9 Document read mode(pixel to pixel type black shading correction)

Absolute maximum rating

Parameters	Syn.	min.	max.	Unit	Remarks
Supply voltage Digital Analog	 VD VA	 -0.3 -0.3	 6.7 6.7	 V V	
Digital applied voltage	V_{TD}	-0.3	VD+0.3	V	
Analog applied voltage	V_{TA}	-0.3	VA+0.3	V	
Operating temp.	T_a	0	70	℃	
Storage temp.	T_{stg}	-55	125	℃	
Soldering temp. and time	T_{SOL}	260℃, 10sec		—	

All voltage defined to their corresponding ground, AVSS or DVSS = 0V

Recommended operating Conditions

Parameters	Symbol	min.	typ.	max.	Unit	Remarks
Supply voltage Digital Analog	 VD VA	 4.75 4.75	 5.0 5.0	 5.25 5.25	 V V	
Operating temperature	Ta	0		70	℃	

All voltage defined to their corresponding ground, AVSS or DVSS = 0V

Electronic Specifications

■DC characteristics

Unless otherwise specified, VD, VA = 5V ± 5%, T_a = 0~70°C

Parameters	Sym.	Pins	min.	typ.	max.	Unit	Conditions
Supply current Digital Analog	 ID IA				 5 80	 mA mA	 MCLK=20MHz No load
HIGH level input voltage	V_{IH}	D0~D7, $\overline{CS}$, $\overline{WR}$, $\overline{RD}$, TRIG, RA0~RA3, SD0~SD7, MCLK, $\overline{TEST}$, $\overline{RESET}$	2.4	–	–	V	
LOW level input voltage	V_{IL}		–	–	0.8	V	
HIGH level output voltage	V_{OH}	D0~D7, SA0~SA12, SD0~SD7, $\overline{SOE}$, $\overline{SWR}$, B/$\overline{W}$, OVF, VD0~VD7, TCLK	3.0			V	I_{OH} = -400μA
LOW level output voltage	V_{OL}				0.4	V	I_{OL} = 1.6mA
Leakage current	I_{LI}	$\overline{CS}$, $\overline{RD}$, $\overline{WR}$, RA0~RA3, $\overline{RESET}$, TRIG, MCLK	-10		10	μA	V_I = DVDD V_I = DVSS
	I_{LIO}	D0~D7, SD0~SD7	-10		10	μA	V_I = DVDD V_I = DVSS
	I_{LPU}	$\overline{TEST}$	-10		10	μA	

■Analog specifications

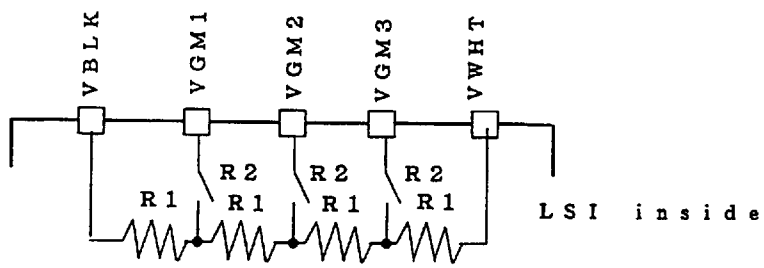
Unless otherwise specified, VD, VA = 5V ± 5%, T_a = 0 ~ 70℃

Parameters	min.	typ.	max.	Unit	Remarks
Analog input					
Maximum signal input level	1.15	1.25	1.35	V_{p-p}	AIN pin
Sampling rate			5	$M_{pix/s}$	AIN pin
Input capacitance		20		pF	AIN pin
Input registance		10		MΩ	AIN pin
Black shading detect/correction circuit					
Detection/correction range			200	mV	
Resolution		±1		mV	
Voltage reference					
AGND voltage		2.75		V	VRO pin I_{OUT} = ±100μA AVDD=5V
VBREF voltage		2.45		V	VBREF pin I_{OUT} = ±100μA AVDD=5V
Peak detect/hold circuit					
Maximum detect/output voltage	1.15	1.25	1.35	V	
Resolution		±3		mV	
DACs for reference voltage generation of 8bit 2 step flash ADC					
Resolution		4		BIT	
Settling time			400	μS	CL=3.3μF, 0.1%
Clump circuit					
Switch ON registance			150	Ω	

■Analog specifications Unless otherwise specified, VD, VA = 5V ± 5%, T_a = 0~70℃

Parameters	min.	typ.	max.	Unit	Remarks
Sample and hold circuit					
Settling time			50	nS	0.1%
AIN pin discharge (line clump mode)			0.3 × Vin_{p-p} × pix counts	pC	AIN pin
White shading detect/correction circuit					
Resolution		8		bit	Vpk-0.5Vpk
Correction range			50	%Vpk	
Precision		± 1/2		LSB	
Flash ADC					
Resolution		8		bit	
INL		±1.5		LSB	VBLK-VWHT ≧0.250V w/o γ correct
DNL		±1.5		LSB	VBLK-VWHT ≧0.250V w/o γ correct
Radder registance between taps (R1)	300	400	500	Ω	NOTE 1
γ ref input pins analog switch ON registance(R2)	100			Ω	NOTE 1

(注1)



■Digital AC characteristics

Unless otherwise specified, VD, VA=5V±5%, Ta=0～70° C

NO	Parameters	Pins	min.	typ.	max.	Unit	Cond.
1	MCLK cycle time (T) NOTE 1	MCLK	50			nS	
2	MCLK HIGH level width	MCLK	40%		60%	T	
3	MCLK LOW level width	MCLK	40%		60%	T	
4	TRIG setup time (to MCLK↑)	TRIG	20			nS	
5	TRIG hold time (to MCLK↑)	TRIG	20			nS	
6	CKSH delay time (to MCLK↑)	CKSH			25	nS	C_L=20pF
7	CKSH cycle time	CKSH		4		T	
8	CKSH HIGH level width	CKSH		1		T	
9	CKSH LOW level width	CKSH		3		T	
10	CKCL(A) delay time (to CKSH↓)	CKCL	T−15	T	T+15	nS	C_L=20pF
11	CKCL cycle time	CKCL		4		T	
12	CKCL(A) HIGH level width	CKCL		1		T	
13	CKCL(A) LOW level width	CKCL		3		T	
14	CKCL(B) delay time (to MCLK↑)	CKCL			25	nS	C_L=20pF
15	CKCL(B) HIGH level width	CKCL		1		T	
16	CKCL(B) LOW level width	CKCL		3		T	
17	CKCL(C) delay time (to CKSH↓)	CKCL	1.5T−15	1.5T	1.5T+15	nS	C_L=20pF
18	CKCL(C) HIGH level width	CKCL		0.5		T	
19	CKCL(C) LOW level width	CKCL		3.5		T	
20	CKSH, CKCL reset delay time (to MCLK↑)	CKSH CKCL			25	nS	CL=20pF
21	SA0～SA12, B/$\overline{W}$ setup time (to $\overline{SWR}$↓)	SA0～SA12 B/W		2		nS	C_L=20pF
22	SA0～SA12, B/$\overline{W}$ hold time (to $\overline{SWR}$↓)	SA0～SA12 B/W		2		nS	C_L=20pF
23	$\overline{SWR}$ pulse width	$\overline{SWR}$	2			T	
24	SD0～SD7 setup time (to $\overline{SWR}$↑)	SD0～SD7			2T−30	nS	CL=20pF
25	SD0～SD7 hold time (to $\overline{SWR}$↑)	SD0～SD7	0			nS	CL=20pF

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Unless otherwize specified, VDD=5v±5%, Ta=0～70°C

NO	Parameters	Pins	min.	typ.	max.	Unit	Cond.
26	SD0～SD7 acceptable delay time(to SA0～SA12, B/$\overline{W}$)	SD0～SD7			2T－50	nS	C_L=20pF
27	SA0～SA12, B/$\overline{W}$ hold time (to MCLK↑)	SA0～SA12 B/$\overline{W}$			70	nS	C_L=20pF
28	SD0～SD7 hold time (to MCLK↑)	SD0～SD7	20			nS	C_L=20pF
29	SD0～SD7 acceptable delay time (to $\overline{SOE}$↓)	SD0～SD7			2T－40	nS	CL=20pF
30	SA0～SA12 hold time (to $\overline{SOE}$↑)	SA0～SA12	0			nS	CL=20pF
31	SD0～SD7 hold time (to $\overline{SOE}$↑)	SD0～SD7	0			nS	C_L=20pF
32	SD0～SD7 acceptable delay time(to SA0～SA12, B/$\overline{W}$)	SD0～SD7			4T－50	nS	CL=20pF
33	$\overline{RD}$ pulse width	$\overline{RD}$	100			nS	
34	$\overline{SOE}$ delay time (to $\overline{RD}$)	$\overline{SOE}$			35	nS	C_L=20pF
35	D0～D7 floating delay time (to $\overline{RD}$↑)	D0～D7	0			nS	CL=20pF
36	D0～D7 delay time (to SD0～SD7)	D0～D7			35	nS	C_L=20pF
37	$\overline{WR}$ pulse width	$\overline{WR}$	100			nS	
38	$\overline{SWR}$ delay time (to $\overline{WR}$)	$\overline{SWR}$			50	nS	C_L=50pF
39	SA0～SA12 delay time (to $\overline{RD}$↑, $\overline{WR}$↑)	SA0～SA12			85	nS	C_L=50pF
40	SD0～SD7 delay time (to $\overline{SWE}$↓)	SD0～SD7			30	nS	C_L=50pF
41	SD0～SD7 floating delay time (to $\overline{SWE}$↑)	SD0～SD7	0			nS	C_L=50pF
42	SD0～SD7 delay time (to D0～D7)	SD0～SD7			40	nS	C_L=50pF
43	SA0～SA12 initialize delay time (to MCLK↑)	SA0～SA12			85	nS	C_L=50pF
44	VD0～VD7 delay time (to MCLK↑)	VD0～VD7			65	nS	C_L=50pF
45	TCLK delay time (to MCLK↑)	TCLK			45	nS	C_L=50pF
46	TCLK LOW level width	TCLK		2T		nS	
47	TCLK HIGH level width	TCLK		2T		nS	
48	OVF delay time (to MCLK↑)	OVF			45	nS	CL=50pF
49	RA0～RA3 setup time (to $\overline{RD}$↓, $\overline{WR}$↓)	RA0～RA3	20			nS	
50	RA0～RA3 hold time (to $\overline{RD}$↑, $\overline{WR}$↑)	RA0～RA3	0			nS	
51	$\overline{CS}$ setup time (to $\overline{RD}$↓, $\overline{WR}$↓)	$\overline{CS}$	20			nS	

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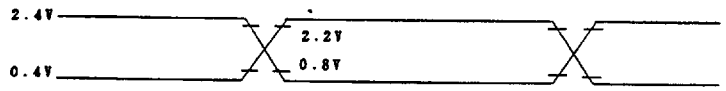
Unless otherwise specified, VDD=5V±5%, Ta=0~70° C

NO	Parameters	Pins	min.	typ.	max.	Unit	Cond.
52	$\overline{CS}$ hold time (to $\overline{RD}$↑)	$\overline{CS}$	0			nS	
53	D0~D7 delay time (対 $\overline{RD}$↓)	D0~D7			55	nS	C_L=50pF
54	D0~D7 floating delay time (to $\overline{RD}$↑)	D0~D7	0			nS	C_L=50pF
55	D0~D7 setup time (to $\overline{WR}$↑)	D0~D7	20			nS	
56	D0~D7 hold time (to $\overline{WR}$↑)	D0~D7	0			nS	
57	$\overline{RESET}$ pulse width	$\overline{RESET}$	20			nS	
58	AIN setup time (to CKSH↑)	AIN	0			nS	
59	AIN hold time (to CKSH↓)	AIN	0			nS	
60	SD0~SD7 setup time (to MCLK↓)	SD0~SD7	20			nS	C_L=20pF

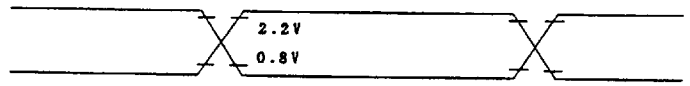
(Note)Necessary access time for the shading memory depends that black shading correction type is odd/even balance one or pixel to pixel one.(Refer to AC timing specifications of NO26, NO32).

■Measurement conditions

AC test input

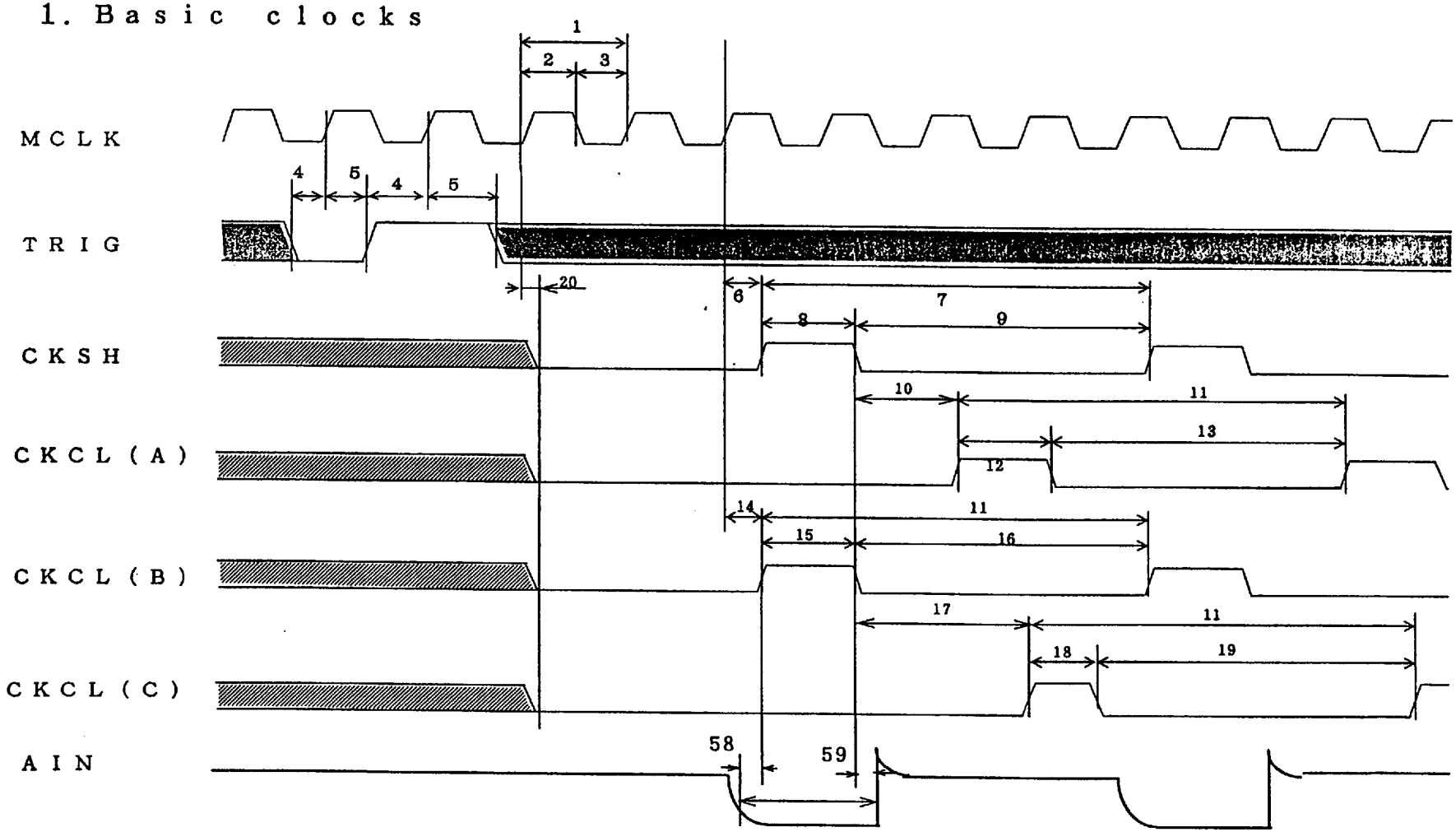


AC test output



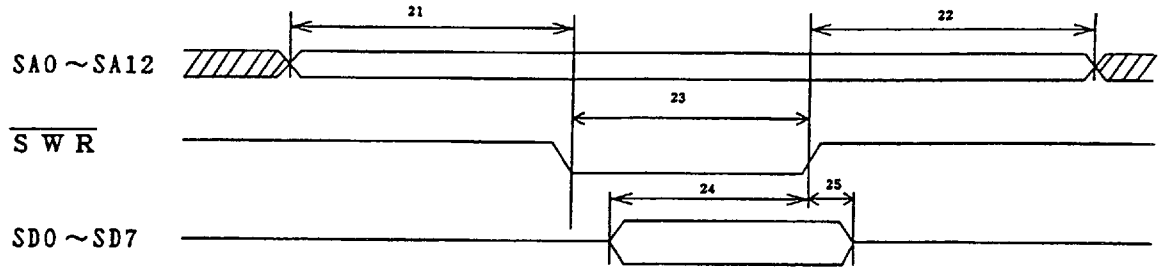
■ Timing specifications

1. Basic clocks



2. Memory access related timings in the each operation mode

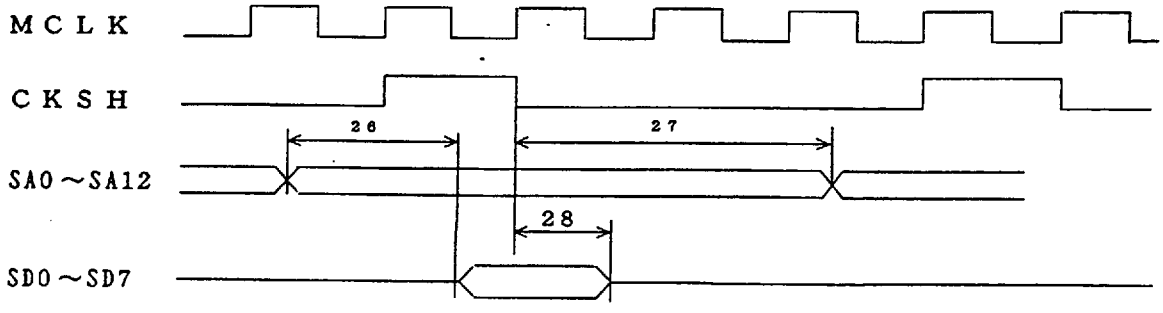
2 – 1. Black shading detection mode(pixel to pixel type)



Black correction data

(NOTE)B/$\overline{W}$,$\overline{SOE}$ are HIGH state.

2 – 2. Peak detect mode(pixel to pixel type black shading correction

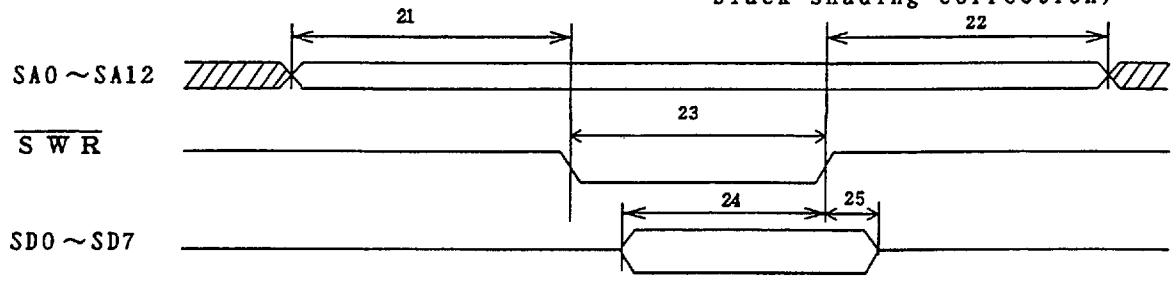


Black correction data

(NOTE)B/$\overline{W}$,$\overline{SWR}$ are H state,$\overline{SOE}$ is L state.

2 − 3 .White shading detect mode(odd/even balance type

black shading correction)

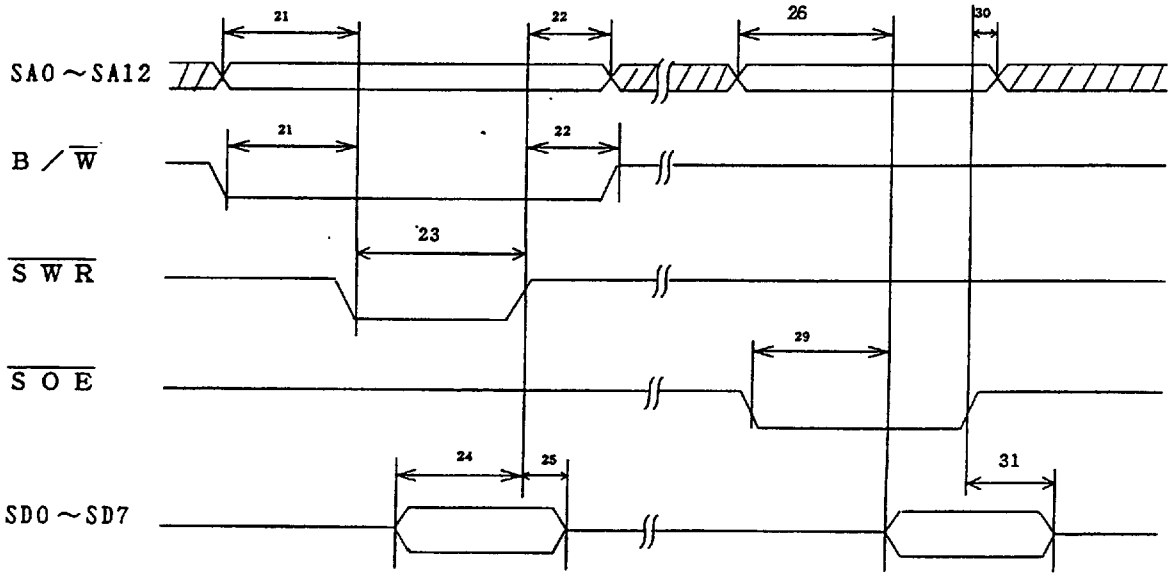


White shading correcrion data

(NOTE)B/$\overline{W}$ is L state,$\overline{SOE}$ are H state.

2 − 4 . White shading detect mode(pixel to pixel type

black shading correction).



White shading correcrion data

Black shading correcrion data

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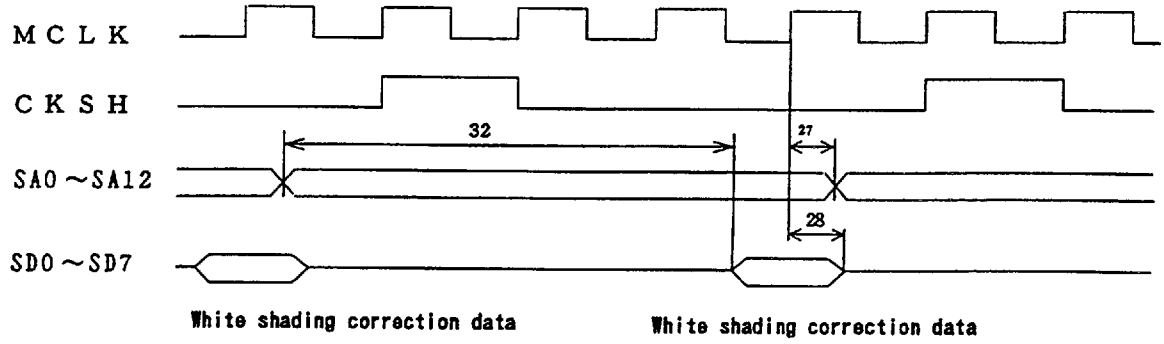
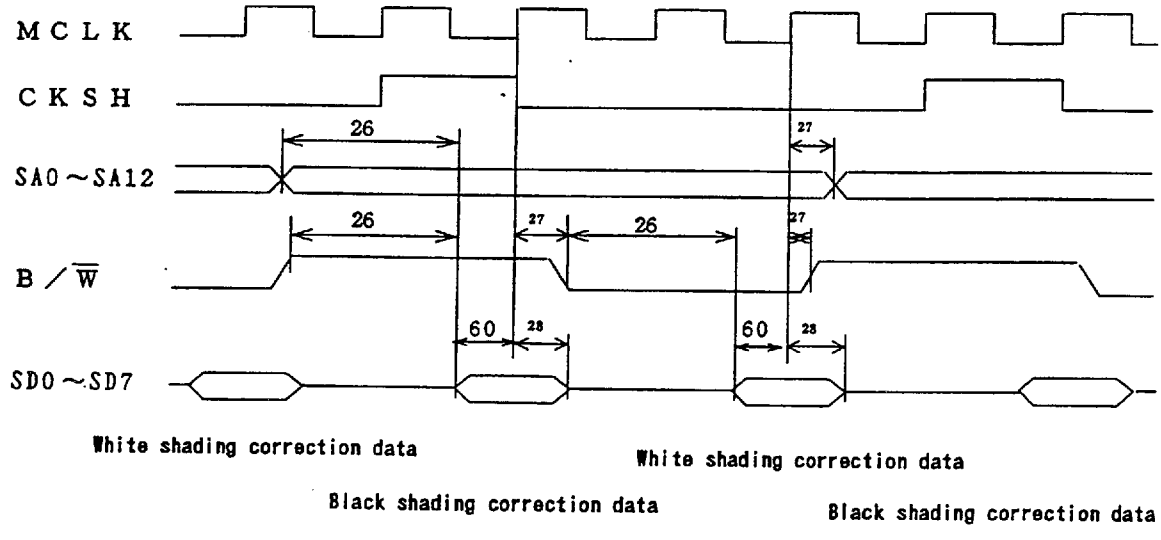
2 – 5. Document read mode(odd/even balance type black shading correction)



(NOTE) B/$\overline{W}$, $\overline{SOE}$ are L state, $\overline{SWR}$ is H state

2 – 6. Document read mode(pixel to pixel type black shading correction)



(NOTE) $\overline{SOE}$ is L state, $\overline{SWR}$ is H state

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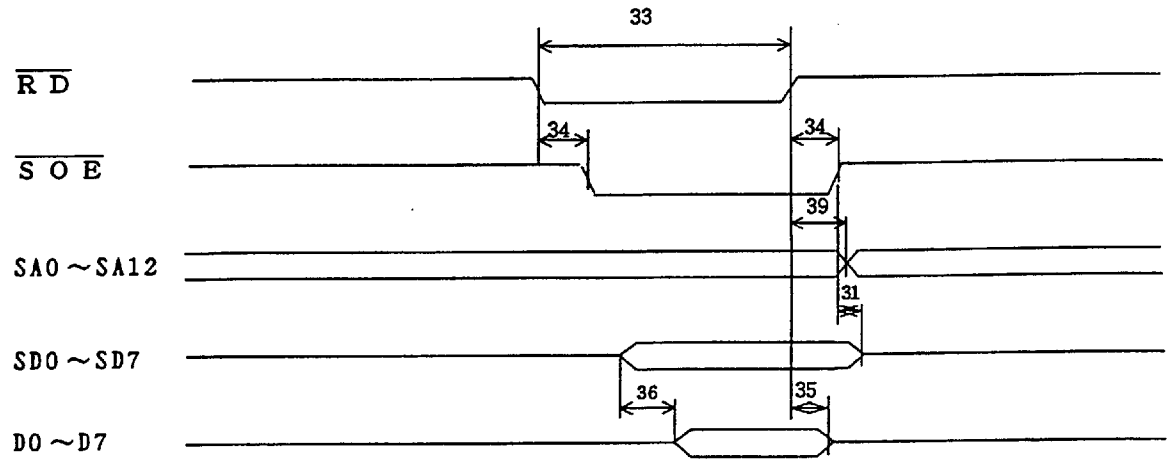
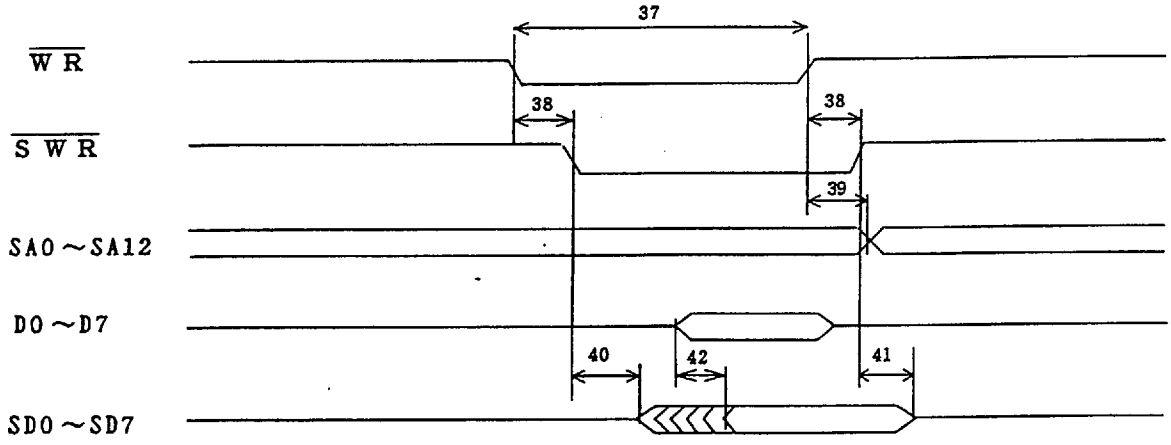
3. Shading memory access mode

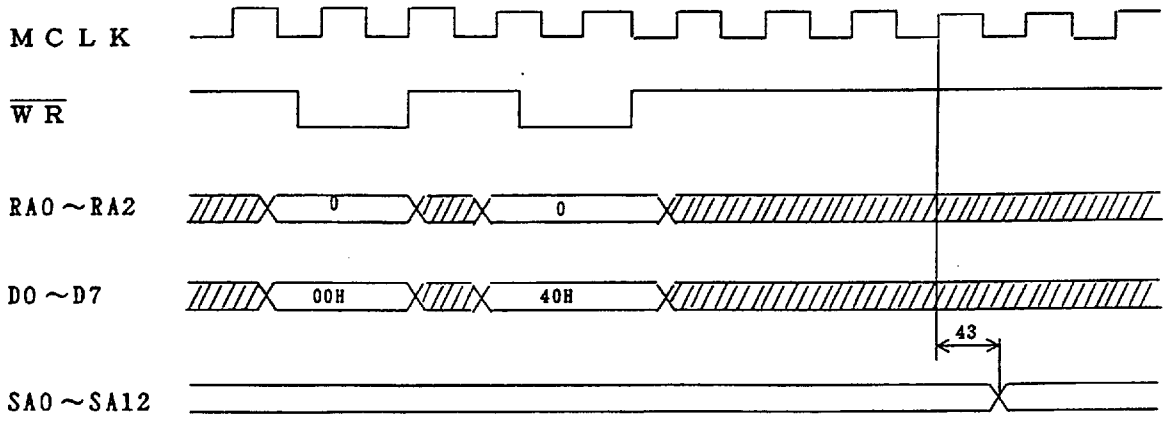
3 – 1. Read



3 – 2. Write



3 – 3. Address counter initialize



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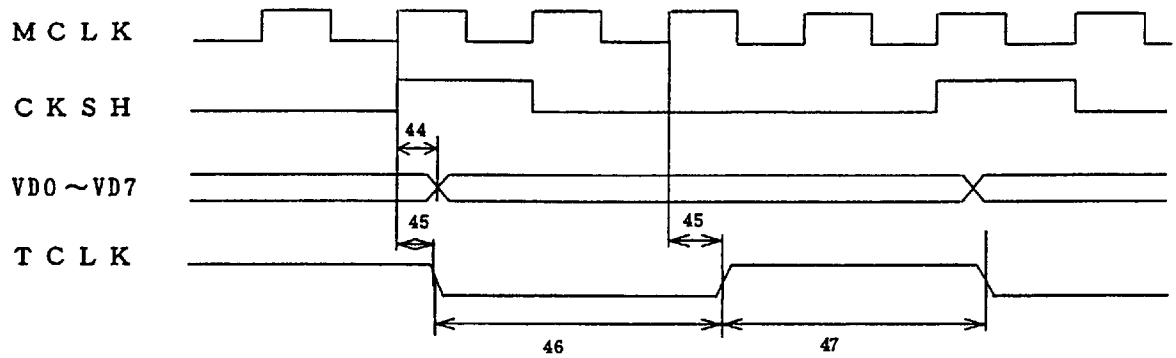
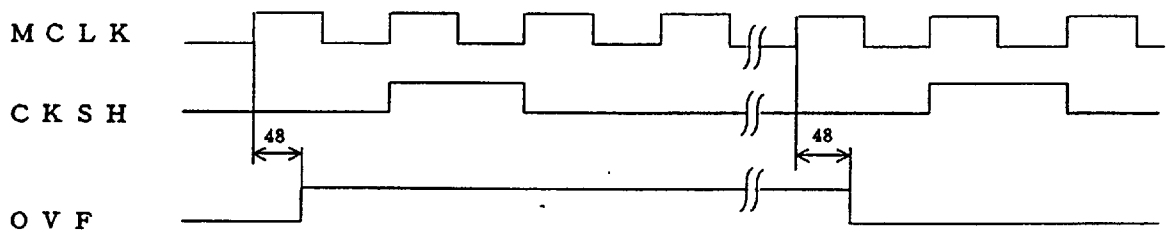
4. Video data output



5. OVF output



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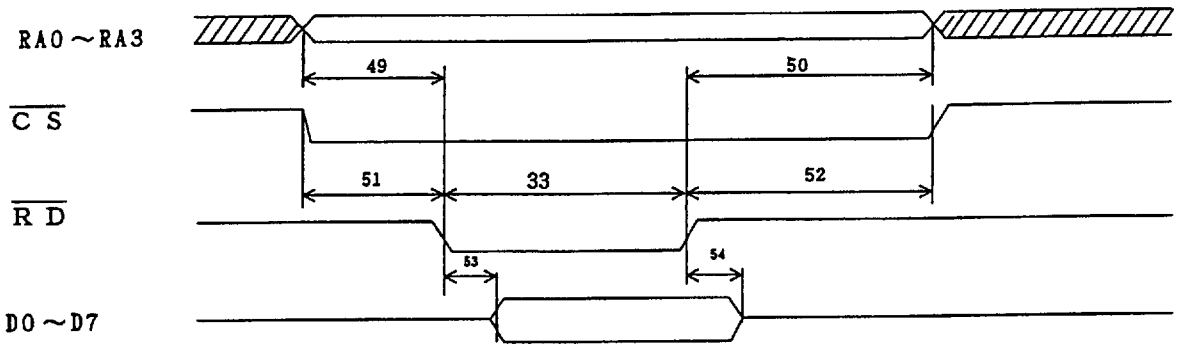
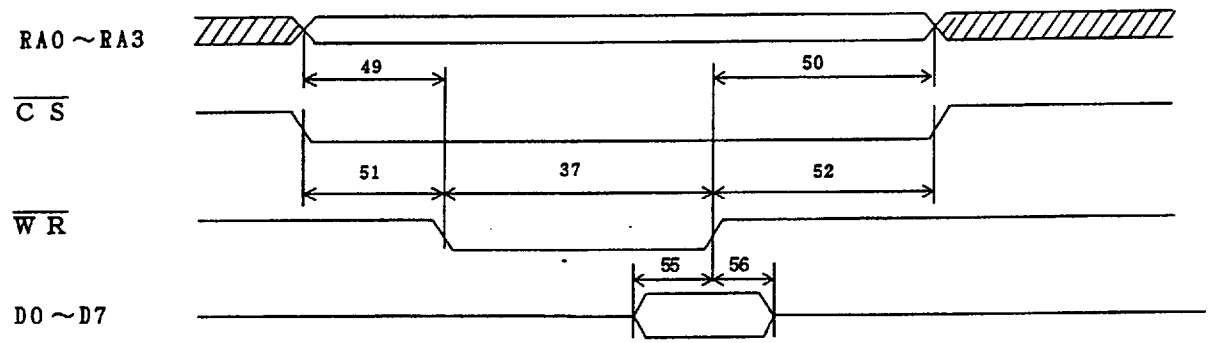
6. System bus interface

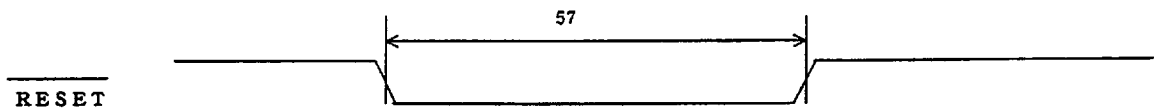
6 - 1. Read



6 - 2. Write



6 - 3. Reset



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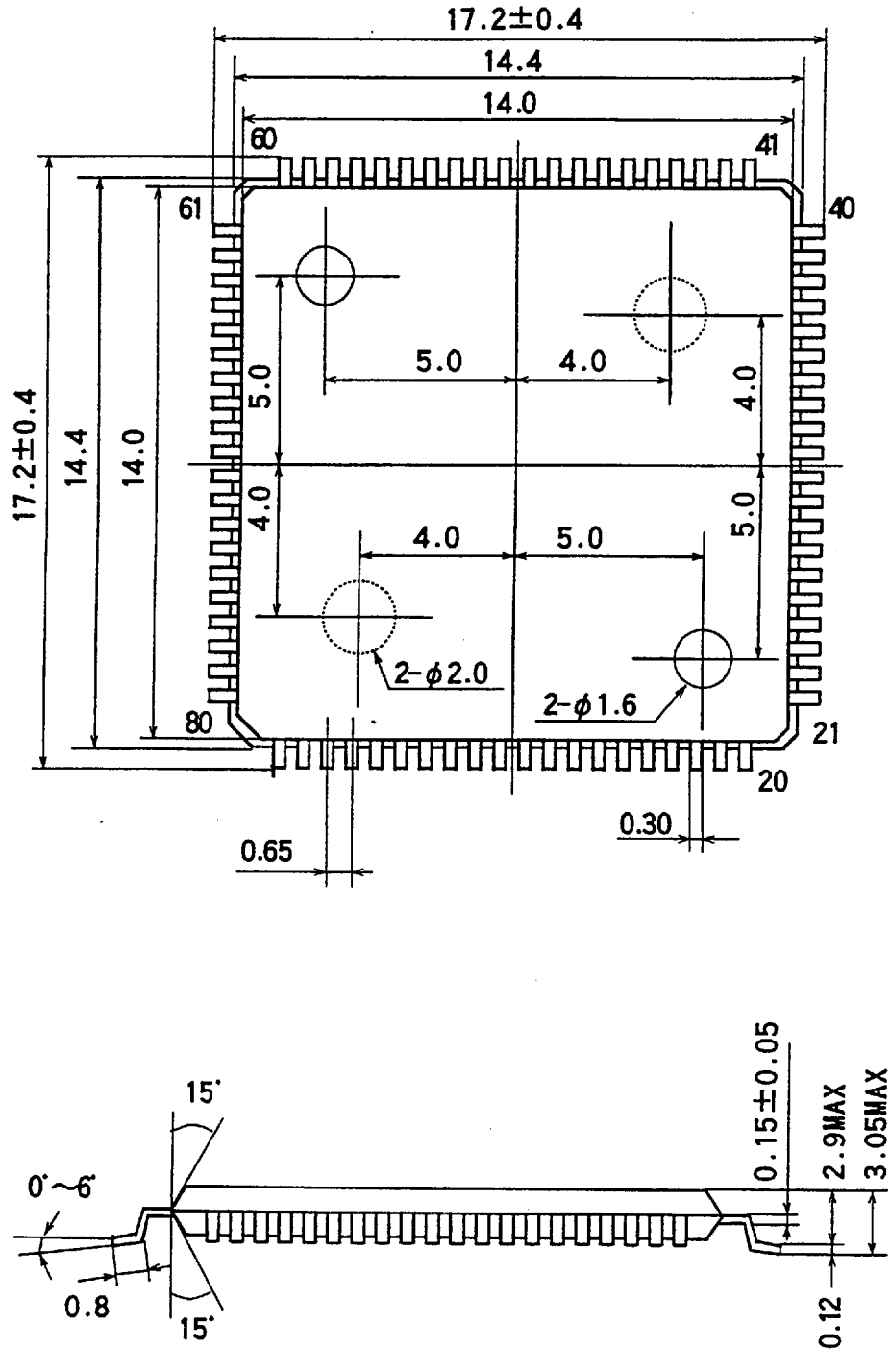
Package



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