100MSPS 12-Bit Track and Hold Amplifier

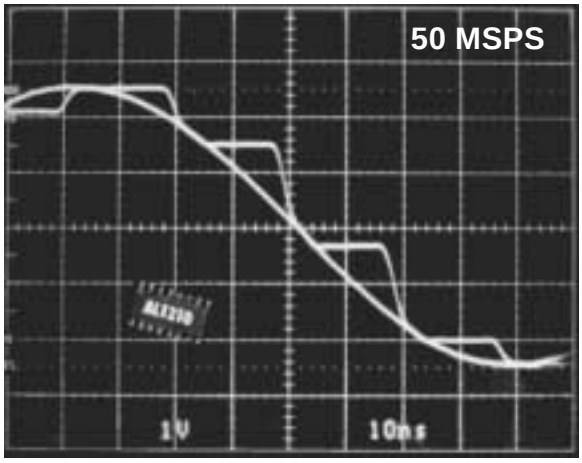
AL1210

FEATURES

- 100MSPS Sampling Rate (8-Bit)
- 50MSPS Sampling Rate (12-Bit)
- 5ns Acquisition Time (8-Bit)
- 4ns Output Settling Time (8-Bit)
- 0.018% Nonlinearity
- 5μV/°C Hold Offset
- 1ps Aperture Jitter
- 400MHz Small Signal Bandwidth
- Low Power (400mW Max.)
- Small Footprint Package (SOIC)

APPLICATIONS

- Flash A/D Driving
- CCD Imaging Systems
- Radar and IF Processors
- Data Acquisition Systems
- Deglitching



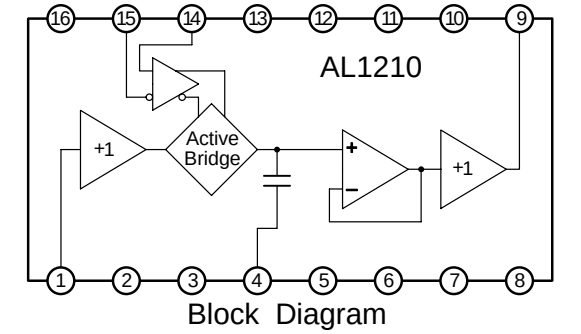
GENERAL DESCRIPTION

The AL1210 is an extremely fast and accurate monolithic track and hold amplifier. Even at input frequencies of up to **20MHz**, and sampling rates of **50MSPS**, its outstanding performance allows full 12-bit linearity to be maintained. Under these extremely fast conditions, the **TOTAL** harmonic distortion introduced by the AL1210 is still only **-70dBc**.

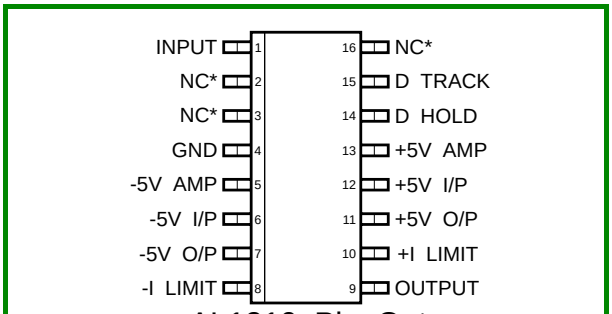
Its primary application is as a track and hold with the new generation high speed flash A/D converters. By using the AL1210 with these converters, it is now possible to obtain meaningful 10-bit performance at input frequencies of up to **40MHz** and sampling rates of up to **75MSPS**. If the AL1210 were not used, the meaningful resolution would drop down to 6 bits or less. **At 50MHz the TOTAL harmonic distortion is only -59dBc**.

The noise that a track and hold circuit generates must be significantly below the resolution or noise of the A/D converter in order not to limit the dynamic range of the system. The causes of noise in a track and hold are quite complex and come from several sources. In the AL1210 these noise sources are kept very low, for example, an aperture jitter of only **1ps** and a total output noise of only 50μV.

To obtain this remarkable performance, **innovative circuit design** and careful layout have been used. It is fabricated in a very fast complementary bipolar process. The AL1210 is packaged in a 16-pin SOIC in order to keep the pin inductances and capacitances to a minimum.



Block Diagram



AL1210 Pin Out

*It is reccomended that the unconnected pins be grounded

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Electrical Characteristics (VCC=5V, VEE=-5V, RL=1k, CL=20pF, unless otherwise specified)

Parameter	Units	Temp	Test Level	AL1210S Min	AL1210S Typ	AL1210S Max	AL1210A Min	AL1210A Typ	AL1210A Max	AL1210J Min	AL1210J Typ	AL1210J Max
DC ACCURACY												
Track Offset	mV	+25°C	I	-15	-8	0	-15	-8	0	-15	-8	0
	mV	Full	VI	-20		5	-20		5	-20		5
Track temperature coefficient[1]	µV/°C	Full	IV		20	40		20	40		20	40
Hold temperature coefficient[1,2]	µV/°C	Full	IV		2	20		2	20		2	20
Track Gain (no load)	V/V	+25°C	I	0.990	0.993	1.000	0.990	0.993	1.000	0.990	0.993	1.000
	V/V	Full	VI	0.980	0.990	1.000	0.980	0.990	1.000	0.980	0.990	1.000
temperature coefficient[1]	ppm/°C	Full	IV		20	30		20	30		20	30
Hold Gain (no load)[2]	V/V	+25°C	I	0.990	0.995	1.000	0.990	0.995	1.000	0.990	0.995	1.000
	V/V	Full	VI	0.990	0.995	1.000	0.990	0.995	1.000	0.990	0.995	1.000
temperature coefficient[1]	ppm/°C	Full	IV		15	30		15	30		15	30
Track Nonlinearity[3]	%	+25°C	I		0.018	0.030		0.018	0.030		0.018	0.030
	%	Full	VI			0.035			0.030			0.030
Hold Nonlinearity[2,3]	%	+25°C	I		0.015	0.030		0.015	0.030		0.015	0.030
	%	Full	VI			0.030			0.030			0.030
Output resistance[4]	Ω	+25°C	IV	6	8	10	6	8	10	6	8	10
	Ω	Full	IV	6		11	6		11	6		11
Output drive capability	mA	+25°C	IV	20		45	20		45	20		45
	mA	Full	VI	15		50	15		50	15		50
without short circuit protection	mA	Full	IV	50			50			50		
PSRR	mV/V	+25°C	I			4			4			4
	mV/V	Full	VI			6			6			6
ANALOG INPUT												
Voltage range[5]	V	Full	IV	-2.5		2.5	-2.6		2.6	-2.7		2.7
Bias current	µA	+25°C	I	-65	-15	10	-65	-15	10	-65	-15	10
	µA	Full	VI	-90		20	-75		15	-65		15
Resistance	kΩ	+25°C	I	170	300		170	300		170	300	
	kΩ	Full	VI	110			140			170		
Capacitance	pF	Full	IV			2			2			2
DIGITAL INPUTS												
Voltage range	V	Full	IV	-2.9		1.9	-3.0		2.0	-3.1		2.1
differential	V	Full	IV	0.4		5	0.4		5	0.4		5
Bias current high	µA	+25°C	I		10	25		10	25		10	25
	µA	Full	IV			50			40			35
Bias current low	µA	+25°C	I	-85	-40		-85	-40		-85	-40	
	µA	Full	IV	-170			-130			-110		
TRACK MODE DYNAMICS												
Bandwidth to output (-3dB)	MHz	+25°C	IV	300	400		300	400		300	400	
	MHz	Full	IV	300			300			300		
Bandwidth to hold cap. (-3dB)	MHz	+25°C	IV	350	400		350	400		350	400	
	MHz	Full	IV	350			350			350		
Total noise at output	µVrms	+25°C	IV		45	55		45	55		45	55
	µVrms	Full	IV			65			65			65
Output noise density	nV/√Hz	+25°C	IV		5	5.5		5	5.5		5	5.5
	nV/√Hz	Full	IV			6.5			6			6
Input current noise	pA/√Hz	+25°C	IV		3.5	5.5		3.5	5.5		3.5	5.5
	pA/√Hz	Full	IV			7			6.5			6
Capacitor slew rate	V/µs	+25°C	V		700			700			700	
	V/µs	Full	IV	550			550			550		
Output slew rate	V/µs	+25°C	V		550			550			550	
	V/µs	Full	IV	475			475			475		
Total Harmonic Distortion												
20MHz 0.5Vpp	dBc	+25°C	V		-74			-74			-74	
	dBc	Full	IV			-68			-68			-68
50MHz 0.5Vpp	dBc	+25°C	V		-54			-54			-54	
	dBc	Full	IV			-48			-48			-48
PSRR to hold cap. (20MHz)	dB	+25°C	V		-34			-34			-34	
	dB	Full	IV			-32			-32			-32
PSRR to output (20MHz)	dB	+25°C	V		-26			-26			-26	
	dB	Full	IV			-24			-24			-24

Parameter	Units	Temp	Test Level	AL1210S Min	AL1210S Typ	AL1210S Max	AL1210A Min	AL1210A Typ	AL1210A Max	AL1210J Min	AL1210J Typ	AL1210J Max
HOLD MODE DYNAMICS												
Feedthrough (10MHz, 2Vpp)	dB	+25°C	IV		-80	-75		-80	-75		-80	-75
	dB	Full	IV			-75			-75			-75
Droop rate[6]	mV/µs	+25°C	I		2.5	5		2.5	5		2.5	5
	mV/µs	Full	VI			15			10			15
time constant[7]	ms	+25°C	IV	0.5	2		0.5	2		0.5	2	
	ms	Full	IV	0.2			0.5			0.5		
Hold noise[8]	mV√s	+25°C	V		50			50			50	
	mV√s	Full	IV			150			150			150
PSRR (20MHz)	dB	Full	IV	18	21		18	21		18	21	
TRACK TO HOLD SWITCHING												
Effective aperture delay[9]	ps	Full	IV	-500	-250	0	-500	-250	0	-500	-250	0
Aperture jitter	ps rms	Full	IV		1	2		1	2		1	2
Pedestal offset	mV	+25°C	I		5	15		5	15		5	15
	mV	Full	VI			20			20			20
temperature coefficient[1]	µV/°C	Full	IV		20	40		20	40		20	40
sensitivity to supply voltage	mV/V	+25°C	IV		0.5	1		0.5	1		0.5	1
	mV/V	Full	IV			2			2			2
Transient amplitude peak-peak[10]	mV	+25°C	V		20			20			20	
	mV	Full	IV			50			50			50
Glitch impulse[10]	pVs	+25°C	V		20			20			20	
	pVs	Full	IV			50			50			50
Settling time to 4mV[11]	ns	+25°C	V		4			4			4	
	ns	Full	IV			6			6			6
Settling time to 0.5mV[11]	ns	+25°C	V		8			8			8	
	ns	Full	IV			12			12			12
Total sampled noise (50MSPS)[12]	µV	+25°C	V		50			50			50	
	µV	Full	IV			100			100			100
HOLD TO TRACK SWITCHING												
Acquisition time[11,13]												
1% 2V step	ns	+25°C	IV		6	8		6	8		6	8
	ns	Full	IV									
0.1% 2V step	ns	+25°C	IV		7.5	9		7.5	9		7.5	9
	ns	Full	IV									
0.01% 2V step	ns	+25°C	IV		12	14		12	14		12	14
	ns	Full	IV									
1% 200mV step	ns	+25°C	IV		4	6		4	6		4	6
	ns	Full	IV									
0.1% 200mV step	ns	+25°C	IV		6.5	7		6.5	7		6.5	7
	ns	Full	IV									
Output overshoot 2V step	mV	+25°C	IV		10	20		10	20		10	20
THROUGHPUT DISTORTION												
Total harmonics 0dBm, 50MSPS[14]												
18.75MHz	dBc	Full	IV		-70	-64		-70	-64		-70	-64
43.75MHz[15]	dBc	Full	IV		-59	-53		-59	-53		-59	-53
POWER REQUIREMENTS												
Total supply current	mA	Full	VI	30	36	40	30	36	40	30	36	40
Supply voltages												
positive	V	Full	V	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25
negative	V	Full	V	–5.25	–5	–4.75	–5.25	–5	–4.75	–5.25	–5	–4.75
Power dissipation	W	Full	VI	0.3	0.36	0.4	0.3	0.36	0.4	0.3	0.36	0.4

NOTES
1. End point average
2. Hold mode values include track mode and pedestal errors
3. End point over ±2V
4. Measured at 5mA output current
5. Voltage range which the output is guaranteed to cover
6. Rate of voltage change in hold mode
7. Decay time constant of the voltage on the hold capacitor
8. Noise accumulated during hold, e.g. at 50mV√s, holding for 10ns will accumulate a 5µVrms error
9. The delay in the analog signal path is greater than the delay in the digital signal path; therefore the effective aperture delay is negative
10. Excluding pedestal
11. Specified from the time of the digital command
12. Includes all sources of noise above 10kHz in the track and hold, driven from a 50-ohm source, excluding aperture jitter
13. Time for which the track and hold must be kept in track mode to acquire to within the specified precision
14. Includes all sources of distortion in the track and hold, measured by FFT analysis
15. This signal is under sampled, and therefore aliased, which does not present a problem in specifying the distortion

Pin Name	Pin No.	Pin Description
INPUT	1	Analog input to the track and hold.
NC	2,3,16	These pins have no internal connection, but do perform an important function. They should be grounded to obtain good isolation between the adjacent pins in the lead frame.
GND	4	Ground connection for the hold capacitor. This should be connected to a ground plane with the minimum inductance possible.
–5V AMP	5	Negative power supply for the amplifier following the hold capacitor. This should be connected to -5V. In order to achieve good isolation from the digital signals and the analog input, it may be desirable to isolate this supply from the input supply.
–5V I/P	6	Negative power supply for the input stages of the track and hold should be connected to -5V. This supply is connected to the internal substrate of the circuit, and therefore no pin should be significantly more negative than this one. Since the current drawn from this supply charges the storage capacitor, it has substantial transients during high slew rates, such as acquisition. It is important for optimum operation that these currents do not induce high speed voltage changes, and this pin therefore should be well decoupled to ground. Series resistance on the power supply side of the decoupling capacitor also can be used to prevent any remaining transients from disturbing the other supplies.
–5V O/P	7	Negative power supply for the output devices. The nature of the current drawn by this pin is dependent on the load presented to the track and hold output. If the -I LIMIT pin is well decoupled, then the currents drawn will not be subject to large high speed transients. However if a 50-ohm load is driven, then the current drawn by this pin may be correspondingly large.
–I LIMIT	8	In normal operation this pin should be decoupled to ground, and will supply transient currents required by the load. The internal output current limit is between this pin and the -5V O/P pin, and therefore these transients will not cause current limiting. If this pin is left unconnected, the current limit will be fast acting, and the -5V O/P should be well decoupled. A large transient of output current will cause current limiting, and consequent serious degradation of output settling time. If current limiting is not required, this pin may be connected to -5V O/P and the pair well decoupled. An output short circuit under these conditions will destroy the device.
OUTPUT	9	Output of the track and hold. This pin is capable of directly driving highly capacitive loads, such as flash A/D converters, or 50-ohm line. If it is required to drive more than 20mA continuously, the current limit should be disabled. No more than 50mA should be drawn.
+I LIMIT	10	See - I LIMIT, except with respect to +5V O/P.
+5V O/P	11	See -5V O/P, except positive supply.
+5V I/P	12	See -5V I/P, except positive supply.
+5V AMP	13	See -5V AMP, except positive supply.
DHOLD	14	One of the digital input pins. It is recommended that these be driven by high speed ECL in a complementary fashion. Particular care should be taken in deriving these signals to keep the edge position jitter to a minimum. This track and hold has very good aperture jitter performance, but can be no better than the jitter on signals presented to the device. High slew rate and fast settling also are desirable attributes for these signals.
DTRACK	15	Complementary signal to DHOLD. When DTRACK is higher than DHOLD, the device is in track mode; and when lower, it is in hold mode. Although for optimum performance, high speed ECL is recommended; it is possible to use other levels, subject to the limitations of the common mode and differential voltages in the specification.

RECOMMENDED OPERATING CONDITIONS

Supply voltages	.....		± 5V
Ambient temperature range	.....	AL1210S	-55 to +125°C
	.....	AL1210A	-25 to +85°C
	.....	AL1210J	0 to +70°C
Analog input range	.....		± 2V
Digital inputs	.....		Balanced ECL

EXPLANATION OF TEST LEVELS

I 100% production tested
II 100% production tested at +25°C; sample tested at temperature extremes
III Sample tested only
IV Parameter is guaranteed by design and characterization
V Parameter is a typical value only
VI 100% production tested at +25°C; military parts 100% tested at temperature extremes

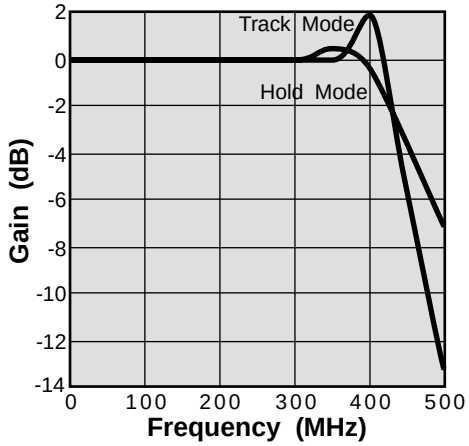
ABSOLUTE MAXIMUM RATINGS

-0.5V	<	(+5V I/P) - (-5V I/P)	<	12.5V
-3V	<	INPUT	<	3V
-5V	<	(D TRACK) - (D HOLD)	<	5V
(-5V I/P) - 0.5V	<	(Any Pin)	<	(+5V I/P) + 0.5V
-55°C	<	Ambient temperature	<	125°C
-65°C	<	Storage temperature	<	150°C
		Lead temperature (10s)	<	300°C
-50mA	<	Continuous output current	<	50mA

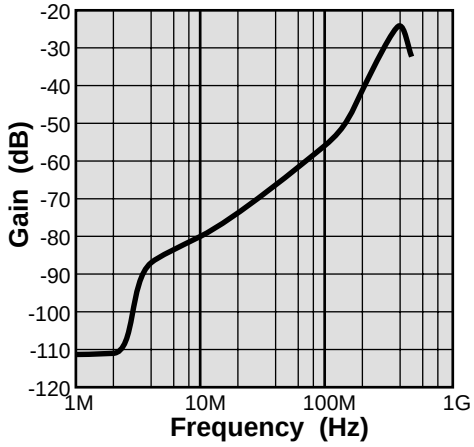
Operation of the device beyond these limits may impair performance permanently

TYPICAL PERFORMANCE CHARACTERISTICS

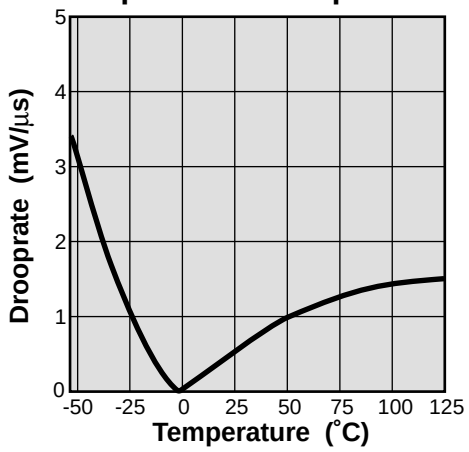
Gain vs Frequency



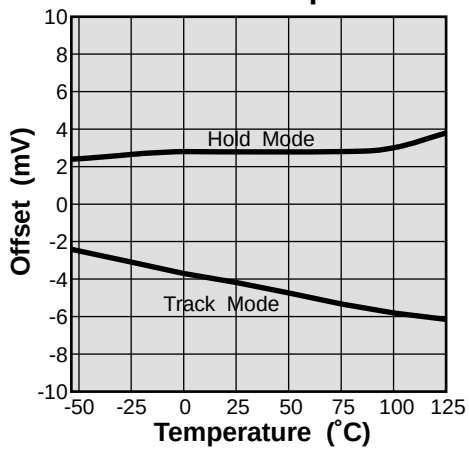
Feedthrough vs Frequency



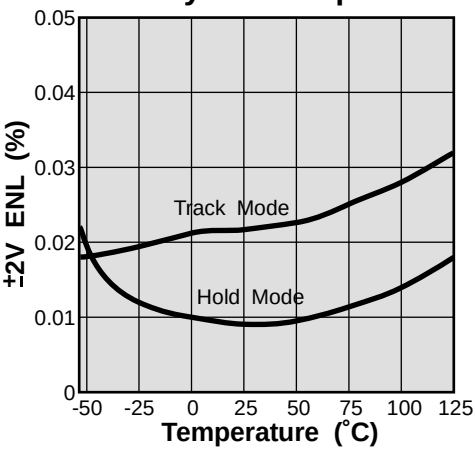
Drooprate vs Temperature



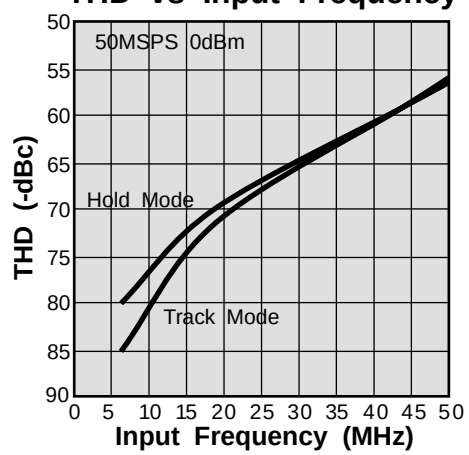
Offset vs Temperature

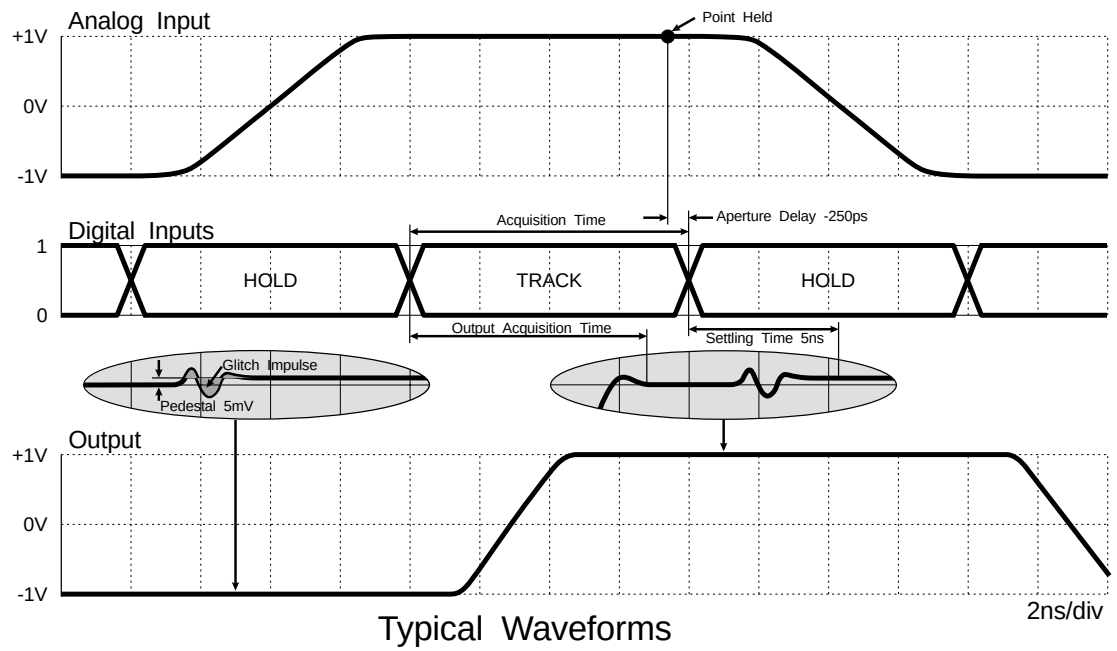


Linearity vs Temperature



THD vs Input Frequency





Typical Waveforms

GLOSSARY OF TRACK AND HOLD TERMINOLOGY

Acquisition Time is the time for which the device has to be switched into track mode in order to acquire the new voltage within a specified percentage of the specified change in voltage.

Aperture Delay is the time delay between the hold command input and the point at which the input is sampled. This can be either positive or negative, depending on the relative delays in the analog and digital signal paths. The exact value is rarely important, but matching between multiple track and holds in a system can be. In some vendors' specifications this figure is excluded from settling time, in which case its magnitude does become significant.

Aperture Jitter is the random variation in aperture delay from sample to sample, expressed as an rms time. Aperture jitter will cause an increase in noise in the presence of high slew rate input waveforms. The extra voltage noise on a sample will be the product of the input slew rate and the aperture jitter.

Delays are included in the acquisition and settling times, and therefore are not specified.

Droop Rate is the rate at which the output voltage changes while the device is in hold mode. For short hold times this is not significant, but over long hold intervals it can cause errors. The estimation of these errors is discussed elsewhere in this data sheet.

Feedthrough is the effect that a change in the analog input voltage has upon the output voltage when the device is in hold mode. Feedthrough is usually worse at higher frequencies.

Output Acquisition Time is the time from when the device is switched into track mode, to when the output has settled to within a specified percentage of the specified change in voltage. Some vendors' specifications call this the acquisition time.

Output Settling Time is the time from when the device is switched into hold mode, to when the output has settled to within a specified voltage of its final value.

Pedestal Offset is the voltage step on the output as the device switches into hold mode, and may be treated as an offset. If it is nonlinear with respect to the input voltage or the slew rate, it will introduce distortion. The pedestal offset of the AL1210 is very linear and stable, and the linearity specification includes pedestal error.

Throughput Cycle Time is the total throughput capability of the device while the output is settling to a given level of accuracy.

Track to Hold Transient is the glitch on the output voltage when the device is switched into hold mode. This is specified in four ways: 1) peak-to-peak magnitude; 2) glitch impulse, which is the area contained within the glitch in Volt-seconds; 3) pedestal offset, which is where it finally settles; and 4) output settling time.

GENERAL DISCUSSION OF TRACK AND HOLD PERFORMANCE

Noise Considerations

There are various sources of noise present in any electronic circuit. The AL1210 has been characterized for its noise performance, but many contributions to noise are dependent on the circuit in which it is used. The various sources of noise are uncorrelated, and the total voltage noise is therefore the rms sum of the noise contributions.

Low drive impedance is desirable to prevent input current noise from developing extra voltage noise at the input. The contribution to noise will be the product of the input current noise and the driving impedance. The resistive part of the source impedance also will generate thermal noise.

Any noise present at the input obviously is included in the sampled signal, and therefore should be minimized. Attention should be given to the bandwidth of the noise source. If the noise density on the input is sufficiently low, then the high bandwidth of the AL1210 will not present a problem; on the other hand, if reduction of amplitude response variation with frequency is important, it will be undesirable to limit the bandwidth.

Hold noise is a result of random charges accumulating on the hold capacitor. Voltage error will accumulate in proportion to the square root of the hold time, and normally will not be significant, although it is specified for the AL1210.

Noise on the power supplies will couple into the signal path, reduced by the power supply rejection ratio. This noise can be minimized by effective decoupling of the supplies at the pins.

Aperture jitter will cause an increase in noise in the presence of high slew rate input waveforms. The extra voltage noise on a sample will be the product of the input slew rate and the aperture jitter.

Aperture jitter of 1ps rms is difficult to maintain. The use of balanced high-speed low-impedance logic helps to minimize jitter degradation. Single-ended TTL driving, although convenient, will degrade this aspect of performance.

Nonlinearity Considerations

Nonlinearity can arise in a variety of ways and is normally measured either as a proportion of the voltage range used (the usual low frequency measurement), or as the harmonic distortion introduced to a sine wave (the usual high frequency measurement). Some caution should be taken in comparing harmonic distortion specifications. Often harmonic distortion will be specified as the ratio of the largest harmonic to the fundamental. Furthermore with track and hold circuits, it is commonly specified in track mode only. While these are useful specifications other factors are significant, in particular:

1) The total harmonic distortion is often of interest, and is sometimes specified as a signal-to-noise ratio, which includes the noise contribution. In systems where data from the converter is subject to digital signal processing, it is necessary to know the contributions to error separately. Distortion and noise integrate differently because distortion is correlated to the signal whereas noise is uncorrelated.

2) A distortion specified in track mode does not include errors introduced by the sampling process. The hold-to-track and track-to-hold settling times place limits on the distortion, but the figures are not readily convertible.

There is a nonlinear DC transfer characteristic imposed upon the signal which causes distortion of the signal independent of frequency. This nonlinearity is usually specified as a percentage of the voltage range over which it is measured, either compared to a straight line joining the endpoints (endpoint nonlinearity or ENL), or to a best-fit straight line. The AL1210 specification is endpoint nonlinearity.

There is a dynamic contribution to nonlinearity during slew. While the signal is slewing, the output of any circuit will lag behind the change in the input. As the slewrate of the signal changes, this lag changes; and there is some nonlinearity in the change. Typically in flash A/D converters, this nonlinearity results in increased distortion as the input slew rate increases. The AL1210 is of great value in alleviating this problem. The level of dynamic distortion in the AL1210 is much lower than in flash A/D converters. The output of the AL1210 is not slewing when the flash A/D is sampling the signal, which results in the full accuracy of the converter being realized, even at high input frequencies. Thus the harmonic distortion performance of the system is improved dramatically.

Further dynamic distortion occurs in flash A/D converters because of a variation in aperture time with input voltage. The distortion associated with this aperture time change is removed when the AL1210 is used to drive the A/D. The output of the AL1210 is not slewing at the time the flash converter samples it; therefore the change in aperture time does not result in a voltage error.

The output stage of the AL1210 is capable of driving low impedance loads. While high currents are being drawn from the output, there is an additional contribution to nonlinearity. This does not affect the system performance driving a flash A/D with a high capacitance input. At the time the flash conversion occurs, the voltage on the output of the AL1210 is static, so no capacitive current is drawn. However if a low resistive impedance is presented to the output of the AL1210, the linearity will be reduced. The input resistance of a flash A/D is unlikely to be low enough to cause any significant degradation of linearity.

During hold mode, the leakage current to the hold capacitor will cause the voltage on the capacitor to drift. As a result, an offset will develop during the hold interval prior to a flash A/D sampling the output. If this interval is not fixed, and if the hold interval and the signal are uncorrelated, this offset will manifest itself as noise. If the hold interval and signal are correlated, this offset will manifest itself as distortion. The most probable situation is that the flash A/D converter will sample the output of the track and hold at a fixed time after the signal is acquired. The drift will result in an offset error, which will have a temperature coefficient related to the temperature coefficient of the leakage current. If the leakage current contains a resistive component, the amplitude of the signal will change with hold time, thereby causing a gain error. However if the leakage current is nonlinear with voltage, a distortion will be introduced with hold time. In a flash A/D driving circuit, this distortion is unlikely to be significant.

Timing Considerations

Throughput is the key specification for the performance of a track and hold and is the rate at which the device can sample signals to a given level of accuracy. Unfortunately this is rarely specified, and therefore has to be estimated. The specifications that are given for track and hold devices vary, and the definitions of the same specification figure also vary. The definitions used for the AL1210 are given in the Glossary.

The AL1210 timing specifications are all measured from the time of the digital command, which is when the two input logic levels cross. This results in a relatively simple estimation of cycle time as the sum of the acquisition time to the required accuracy; the output settling time to the required accuracy; and any interval for which the output is to be held stable for the benefit of subsequent circuitry. Some specifications do not measure from the digital command, but add delay specifications and then specify times from when the output begins to change. This is not a very satisfactory specification because “begins to change” is not a well-defined point, and the output will probably have a transient upon it at the time the logic levels on the digital input change. This may be satisfactory if the interval is a pure delay, but this is not the case if the output has a transient at the logic switching time. Few designers will be prepared to sample the output of the track and hold during this interval; and therefore this delay adds to the useful acquisition and output settling times and reduces the total throughput.

Analog delay is the propagation time for a signal from the input to the output. In some specifications this is excluded from settling time figures; if it is included in settling time, it is of little significance.

From a designer’s viewpoint, the most useful specification is the throughput rate for the required accuracy, which is usually not specified directly in the data sheet. It is a difficult parameter to test in production, and depends to some extent upon the circuit in which it is used. The AL1210 has a specified throughput harmonic distortion (sometimes called hold mode distortion).

Sampling Below Nyquist

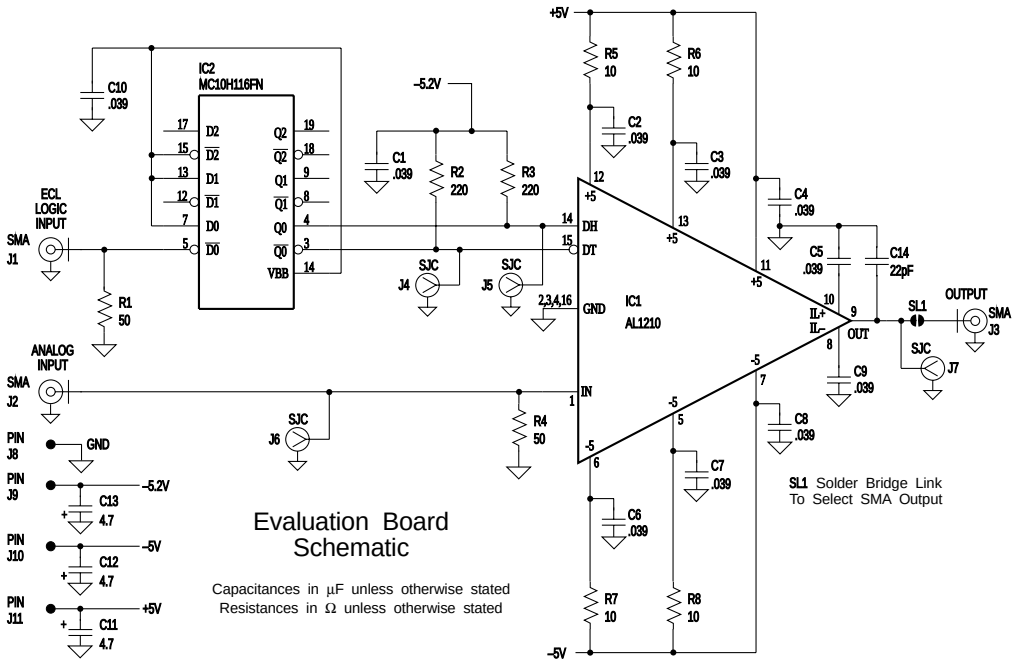
The AL1210 is quite capable of sampling signals of higher frequencies than can be resolved by the sampling rate unambiguously, subject to the available bandwidth. However it should be recognized that distortion of the input signal is primarily a result of slew rate: the higher the amplitude of a high frequency sine wave, the higher the distortion. The AL1210 has a distortion specification for a 1Vpp 50MHz input. The effect of aperture jitter at high slew rates also will increase the noise level.

Circuit Techniques

The AL1210 is capable of driving typical capacitive loads with relatively little lengthening of output settling time; however resonant loads can cause more significant settling time increases. The most common way of presenting a resonant load is as a capacitive load at the far end of a length of line. Even a few centimeters of line can be very significant. The AL1210 therefore should be mounted very close to the load it is driving. If this is not possible, then a resistor in series with the output can help to damp the ringing that occurs, and can keep the output settling time reasonably short.

The power supplies of the AL1210 are brought out of the package separately. This minimizes the mutual coupling that would occur as a result of the inductance of the package pin. In order to preserve isolation, the tracks from these pins should be kept separate until they are decoupled to ground, which should be as close as possible to the package. Series resistors in the power supplies, as shown in the evaluation board schematic, can help to preserve this isolation.

The AL1210 contains current limiting circuitry to prevent destruction of the device under short circuit output conditions. Decoupling the -I limit and +I limit pins will allow larger output currents to flow for short periods. Connecting -I limit to -5V O/P and +I limit to +5V O/P will disable completely the current limiting function.



LAYOUT CONSIDERATIONS

As with any high speed precision circuit, good printed circuit board layout is necessary. A small package and the use of surface mounting help to reduce the parasitic inductances associated with the pins.

The package inductance of pin 4 to ground is already the limiting factor for both acquisition time and output settling time. Therefore pin 4 should be connected directly to an extensive ground plane. Pins 2, 3 and 16 should be grounded; this will minimize capacitive coupling between digital and analog inputs which would otherwise degrade performance.

Ground return paths for the input, digital inputs, output and power supply decoupling should not intersect within the ground plane as this would cause mutual coupling of these signals.

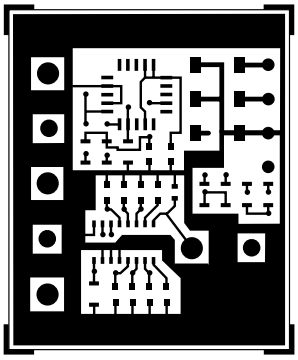
The input and digital control lines should be transmitted via properly terminated transmission lines, such as microstrip or stripline, if they are longer than 20 or 30mm. The output path should either be kept very short or be properly terminated. The part is capable of driving 50-ohm line, although doing so will reduce the linearity. Unterminated line on the output will adversely affect output settling time. The capacitive load presented by typical flash A/D converters does not present a linearity problem, in spite of its very nonlinear nature, because the output voltage is settled at the time the flash converter is fired.

Correct power supply decoupling is very important; typically 0.01µF surface-mounted multilayer capacitors should be placed as close as possible to the power supply pins of the AL1210. Further isolation of the supplies may be achieved by the use of small series resistors, as in the evaluation board. These resistors and capacitors prevent the high speed transient currents from the track and hold causing voltage transients on the supplies; and also prevent external high frequency transients from reaching the device supplies. It is important that the supplies are stable and contain no lower frequency transients; therefore sharing a supply with logic is not recommended unless thorough supply filtering is employed.

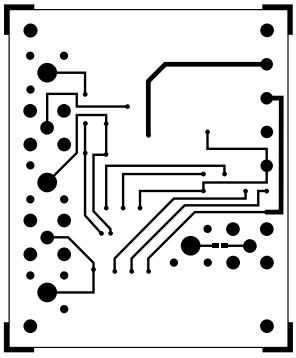
The use of sockets is not recommended because of the associated increase in stray inductances.

The layout of the evaluation board (AL1210-EVAL) is shown above, and fulfills all of the layout requirements satisfactorily. The schematic of the board is shown above, and illustrates how the part may be used. When the device forms part of a larger circuit, considerable benefit can be gained through the use of a multilayer board. The evaluation board is available to assist the designer in assessing the capabilites of the AL1210 without having to arrange a test fixture.

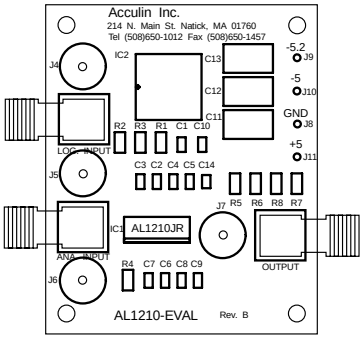
The evaluation board includes an ECL line receiver (IC2) as a convenience to provide balanced logic to the AL1210; other balanced logic sources may be used. In a larger circuit, it may be preferable to terminate the ECL in 50 ohms to -2V depending upon the logic transmission environment.



Component Side Metal



Back Side Metal



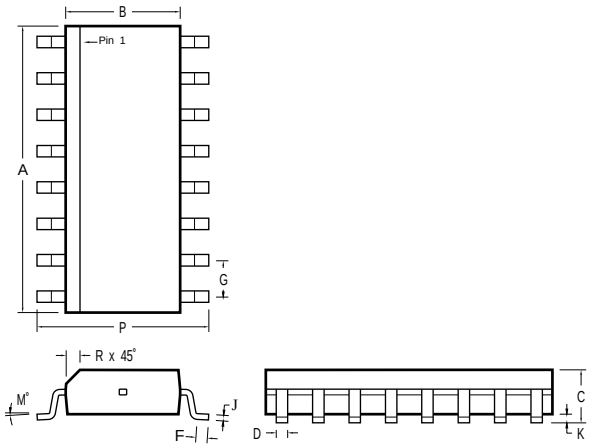
Component Layout

Evaluation Board Layout

ORDERING INFORMATION

Model	Temp Range	Package
AL1210JR	0 to +70°C	16-pin SOIC
AL1210AR	-25 to +85°C	16-pin SOIC
AL1210SE	-55 to +125°C	20-terminal LCC
AL1210SJ/2	-55 to 125°C	20 J-Lead Ceramic
AL1210-DIE	Various	Unpackaged
AL1210-EVAL	Evaluation Board	PCB

PACKAGE DIMENSIONS

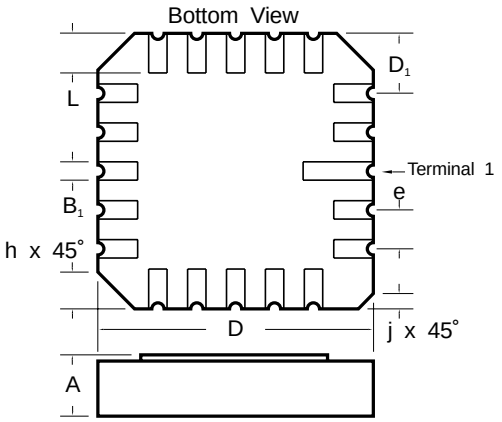


SOIC-16 PACKAGE (R SUFFIX)

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

NOTES:
1. CONTROLLING DIMENSION: MILLIMETER
2. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION
3. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE

LCC-20 PACKAGE (E SUFFIX)

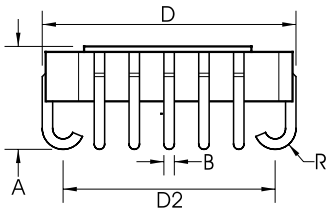


	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	1.63	2.54	0.064	0.100
B_1	0.56	0.71	0.022	0.028
D	8.69	9.09	0.342	0.358
D_1	1.91 REF		0.075 REF	
e	1.27 BSC		0.050 BSC	
j	0.51 REF		0.020 REF	
h	1.02 REF		0.040 REF	
L	1.14	1.40	0.045	0.055

NOTES:
1. CONTROLLING DIMENSION: INCH
2. DIMENSION A IS OVERALL PACKAGE THICKNESS
3. DIMENSION D APPLIES TO ALL FOUR SIDES

20 J-LEADED CERAMIC (J/2 SUFFIX)

package as LCC-20 with leads attached



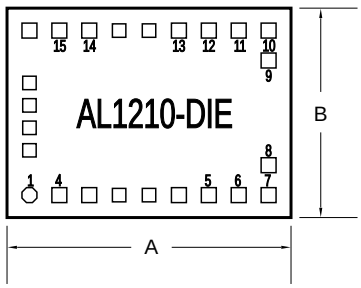
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	2.54	5.08	0.100	0.200
B	0.31	0.46	0.012	0.018
D	8.69	9.34	0.342	0.368
D2	7.16	7.82	0.282	0.308
R	0.64	0.89	0.025	0.035

NOTES:
1. CONTROLLING DIMENSION: INCH
2. DIMENSIONS D AND D2 APPLY TO ALL FOUR SIDES

Conversion Table

16-Pin SOIC	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
20-Term Ceramic	2	3	4	5	7	8	9	10	12	13	14	15	17	18	19	20

UNPACKAGED DIE (-DIE SUFFIX)



	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	1.93	2.18	0.076	0.086
B	1.27	1.52	0.050	0.060
C	0.28	0.43	0.011	0.017

NOTES:
1. CONTROLLING DIMENSION: MILLIMETER
2. DIMENSION C IS OVERALL DIE THICKNESS
3. NUMBERS BY BONDPADS REFER TO SOIC PINS

November 2000