# QUAD MICROPOWER RAIL TO RAIL CMOS OPERATIONAL AMPLIFIER

## GENERAL DESCRIPTION

The ALD 4701 is a quad monolithic CMOS micropower high slew-rate operational amplifier intended for a broad range of analog applications using ±1V to ±6V dual power supply systems, as well as +2V to +12V battery operated systems. All device characteristics are specified for +5V single supply or ±2.5V dual supply systems. Total supply current for four operational amplifiers is 1mA maximum at 5V supply voltage. It is manufactured with Advanced Linear Devices' enhanced A CMOS silicon gate CMOS process.

The ALD 4701 is designed to offer a tradeoff of performance parameters providing a wide range of desired specifications. It offers the popular industry pin configuration of LM324 and ICL 7641 types.

The ALD 4701 has been developed specifically for the +5V single supply or ±1V to ±6V dual supply user. Several important characteristics of the device make application easier to implement at these voltages. First, each operational amplifier can operate with rail to rail input and output voltages. This means the signal input voltage and output voltage can be equal to or near to the positive and negative supply voltages. This feature allows numerous analog serial stages and flexibility in input signal bias levels. Secondly, each device was designed to accommodate mixed applications where digital and analog circuits may operate off the same power supply or battery. Thirdly, the output stage can typically drive up to 50 pF capacitive and 10 KΩ resistive loads. These features, combined with extremely low input currents, high open loop voltage gain of 100V/mV, useful bandwidth of 700 KHz, a slew rate of 0.7V/µs, low power dissipation of 5mW, low offset voltage and temperature drift, make the ALD 4701 a versatile, micropower quad operational amplifier.

The ALD 4701, designed and fabricated with silicon gate CMOS technology, offers 1 pA typical input bias current. Due to low voltage and low power operation, reliability and operating characteristics, such as input bias currents and warm up time, are greatly improved.

## ORDERING INFORMATION

| | Operating Temperature Range | | |
|---|---|---|---|
| | -55°C to +125°C | 0°C to +70°C | 0°C to +70°C |
| +25°C $V_{os}$ (mV) | 14-Pin CERDIP Package | 24-Pin Small Outline Package (SOIC) | 14-Pin Plastic Dip Package |
| 2.0 | ALD 4701A DB | ALD 4701A SF | ALD 4701A PB |
| 5.0 | ALD 4701B DB | ALD 4701B SF | ALD 4701B PB |
| 10.0 | ALD 4701 DB | ALD 4701 SF | ALD 4701 PB |



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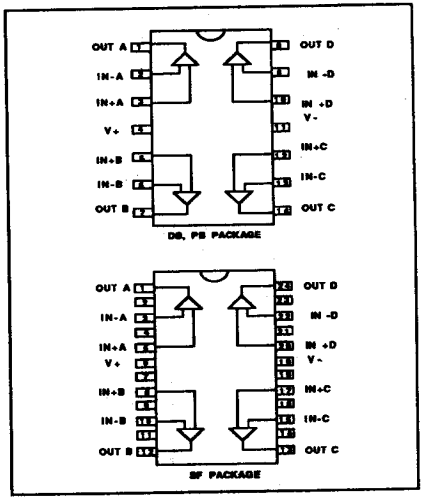
## PIN CONFIGURATION




## FEATURES

- All parameters specified for + 5 V single supply or ± 2.5V dual supply systems
- Rail to rail input and output voltage ranges
- Unity gain stable
- Extremely low input bias currents – 1.0 pA
- High source impedance applications
- Dual power supply ±1.0 V to ±6.0 V
- Single power supply +2 V to +12 V
- High voltage gain
- Output short circuit protected
- Unity gain bandwidth of 0.7 MHz
- Slew rate of 0.7 V/µs
- Low power dissipation
- Symmetrical output drive

## APPLICATIONS

- Voltage follower/buffer/amplifier
- Charge integrator
- Photodiode amplifier
- Data acquisition systems
- High performance portable instruments
- Signal conditioning circuits
- Sensor and transducer amplifiers
- Low leakage amplifiers
- Active filters
- Sample/Hold amplifier
- Picoammeter
- Current to voltage converter

## ABSOLUTE MAXIMUM RATINGS

| | | |
|---|---|---|
| Supply voltage, $V_{DD}$ | | 12V |
| Differential input voltage range | | -0.3V to $V_{DD}$ +0.3V |
| Power dissipation | | 600 mW |
| Operating temperature range | 4701XPB/4701XSF | 0°C to +70°C |
| | 4701XDB | -55°C to +125°C |
| Storage temperature range | | -65°C to +150°C |
| Lead temperature, 10 seconds | | +300°C |

## DC AND OPERATING ELECTRICAL CHARACTERISTICS

**$T_A$ = 25°C $V_{DD}$ = 5.0V ($V_S$ = ±2.5V in dual supply operation) unless otherwise specified**

| Parameter | Symbol | 4701A Min | 4701A Typ | 4701A Max | 4701B Min | 4701B Typ | 4701B Max | 4701 Min | 4701 Typ | 4701 Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Supply Voltage | $V_S$ | ±1.0 | | ±6.0 | ±1.0 | | ±6.0 | ±1.0 | | ±6.0 | V | Dual Supply |
| | $V_{DD}$ | 2.0 | | 12.0 | 2.0 | | 12.0 | 2.0 | | 12.0 | V | Single Supply |
| Input Offset Voltage | $V_{OS}$ | | | 2.0 | | | 5.0 | | | 10.0 | mV | $R_S$≤100KΩ |
| | | | | 2.8 | | | 5.8 | | | 11.0 | mV | 0°C≤$T_A$≤+70°C |
| Input Offset Current | $I_{OS}$ | | 1.0 | 25 | | 1.0 | 25 | | 1.0 | 25 | pA | $T_A$ = 25°C |
| | | | | 240 | | | 240 | | | 240 | pA | 0°C≤$T_A$≤+70°C |
| Input Bias Current | $I_B$ | | 1.0 | 30 | | 1.0 | 30 | | 1.0 | 30 | pA | $T_A$=25°C |
| | | | | 300 | | | 300 | | | 300 | pA | 0°C≤$T_A$≤+70°C |
| Input Voltage Range | $V_{IR}$ | 0.0 | | 5.0 | 0.0 | | 5.0 | 0.0 | | 5.0 | V | $V_{DD}$ = +5V |
| | | -2.5 | | +2.5 | -2.5 | | +2.5 | -2.5 | | +2.5 | V | $V_S$ = ±2.5V |
| Input Resistance | $R_{IN}$ | | $10^{12}$ | | | $10^{12}$ | | | $10^{12}$ | | Ω | |
| Input Offset Voltage Drift | $TCV_{OS}$ | | 5 | | | 5 | | | 7 | | µV/°C | $R_S$≤100KΩ |
| Power Supply Rejection Ratio | PSRR | 65 | 80 | | 65 | 80 | | 60 | 80 | | dB | $R_S$≤100KΩ |
| | | 65 | 80 | | 65 | 80 | | 60 | 80 | | dB | 0°C≤$T_A$≤+70°C |
| Common Mode Rejection Ratio | CMRR | 65 | 83 | | 65 | 83 | | 60 | 83 | | dB | $R_S$≤100KΩ |
| | | 65 | 83 | | 65 | 83 | | 60 | 83 | | dB | 0°C≤$T_A$≤+70°C |
| Large Signal Voltage Gain | $A_V$ | 15 | 100 | | 15 | 100 | | 10 | 80 | | V/mV | $R_L$=100KΩ |
| | | | 300 | | | 300 | | | 300 | | V/mV | $R_L$≥1MΩ |
| | | 10 | | | 10 | | | 7 | | | V/mV | $R_L$=100KΩ 0°C≤$T_A$≤+70°C |
| Output Voltage | $V_O$ low | | 0.02 | 0.10 | | 0.02 | 0.10 | | 0.02 | 0.10 | V | $R_L$=100KΩ$V_{DD}$=5V |
| | $V_O$ high | 4.90 | 4.98 | | 4.90 | 4.98 | | 4.90 | 4.98 | | V | 0°C≤$T_A$≤+70°C |
| Range | $V_O$ low | | -2.48 | -2.40 | | -2.48 | -2.40 | | -2.48 | -2.40 | V | $R_L$=100KΩ$V_S$=±2.5V |
| | $V_O$ high | 2.40 | 2.48 | | 2.40 | 2.48 | | 2.40 | 2.48 | | V | 0°C≤$T_A$≤+70°C |
| Output Short Circuit Current | $I_{SC}$ | | 1 | | | 1 | | | 1 | | mA | |
| Supply Current | $I_S$ | | 480 | 1000 | | 480 | 1000 | | 480 | 1000 | µA | $V_{IN}$ =0V No Load |
| Power Dissipation | $P_D$ | | | 5.0 | | | 5.0 | | | 5.0 | mW | All amplifiers $V_S$=±2.5V |

**DC AND OPERATING ELECTRICAL CHARACTERISTICS (cont'd)**
**$T_A$ = 25°C $V_S$ = ±2.5V unless otherwise specified**

| Parameter | Symbol | 4701A | | | 4701B | | | 4701 | | | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | | |
| Input Capacitance | $C_{IN}$ | | 1 | | | 1 | | | 1 | | pF | |
| Bandwidth | $B_W$ | | 700 | | | 700 | | | 700 | | KHz | |
| Slew Rate | $S_R$ | | 0.7 | | | 0.7 | | | 0.7 | | V/µS | $A_V$=+1 $R_L$=100KΩ |
| Rise time | $t_r$ | | 0.2 | | | 0.2 | | | 0.2 | | µS | $R_L$=100KΩ |
| Overshoot Factor | | | 20 | | | 20 | | | 20 | | % | $R_L$=100KΩ $C_L$=50pF |
| Settling Time $R_L$=100KΩ | $t_s$ | | 10.0 | | | 10.0 | | | 10.0 | | µs | 0.1% $A_V$=-1 $C_L$=50pF |
| Channel Separation | cs | | 120 | | | 120 | | | 120 | | dB | $A_V$=100 |

**$T_A$ = 25°C $V_S$ = ±5.0V unless otherwise specified**

| Parameter | Symbol | 4701A | | | 4701B | | | 4701 | | | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | | |
| Power Supply Rejection Ratio | PSRR | | 83 | | | 83 | | | 83 | | dB | $R_S$≤100KΩ |
| Common Mode Rejection Ratio | CMRR | | 83 | | | 83 | | | 83 | | dB | $R_S$≤100KΩ |
| Large Signal Voltage Gain | $A_V$ | | 250 | | | 250 | | | 250 | | V/mV | $R_L$=100KΩ |
| Output Voltage Range | $V_O$ low<br>$V_O$ high | 4.90 | -4.98<br>4.98 | -4.90 | 4.90 | -4.98<br>4.98 | -4.90 | 4.90 | -4.98<br>4.98 | -4.90 | V<br>V | $R_L$=100KΩ |
| Bandwidth | $B_W$ | | 1.0 | | | 1.0 | | | 1.0 | | MHz | |
| Slew Rate | $S_R$ | | 1.0 | | | 1.0 | | | 1.0 | | V/µS | $A_V$=+1 $C_L$=50pF |

**$V_S$ = ±2.5V –55°C ≤ $T_A$ ≤ +125°C unless otherwise specified**

| Parameter | Symbol | 4701A DB | | | 4701B DB | | | 4701 DB | | | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | | |
| Input Offset Voltage | $V_{OS}$ | | | 3.0 | | | 6.0 | | | 15.0 | mV | $R_S$≤100KΩ |
| Input Offset Current | $I_{OS}$ | | | 8.0 | | | 8.0 | | | 8.0 | nA | |
| Input Bias Current | $I_B$ | | | 10.0 | | | 10.0 | | | 10.0 | nA | |
| Power Supply Rejection Ratio | PSRR | 60 | 75 | | 60 | 75 | | 60 | 75 | | dB | $R_S$≤100KΩ |
| Common Mode Rejection Ratio | CMRR | 60 | 83 | | 60 | 83 | | 60 | 83 | | dB | $R_S$≤100KΩ |
| Large Signal Voltage Gain | $A_V$ | 10 | 50 | | 10 | 50 | | 7 | 50 | | V/mV | $R_L$=100KΩ |
| Output Voltage Range | $V_O$low<br>$V_O$high | 2.35 | -2.47<br>2.45 | -2.40 | 2.35 | -2.47<br>2.45 | -2.40 | 2.35 | -2.47<br>2.45 | -2.40 | V<br>V | $R_L$=100KΩ |

## Design & Operating Notes:

1. The ALD 4701 CMOS operational amplifier uses a 3 gain stage architecture and an improved frequency compensation scheme to achieve large voltage gain, high output driving capability, and better frequency stability. In a conventional CMOS operational amplifier design, compensation is achieved with a pole splitting capacitor together with a nulling resistor. This method is, however, very bias dependent and thus cannot accomodate the large range of supply voltage operation as is required from a stand alone CMOS operational amplifier. The ALD 4701 is internally compensated for unity gain stability using a novel scheme that does not use a nulling resistor. This scheme produces a clean single pole roll off in the gain characteristics while providing for more than 70 degrees of phase margin at the unity gain frequency.

2. The ALD 4701 has complementary p-channel and n-channel input differential stages connected in parallel to accomplish rail to rail input common mode voltage range. This means that with the ranges of common mode input voltage close to the power supplies, one of the two differential stages is switched off internally. To maintain compatibility with other operational amplifiers, this switching point has been selected to be about 1.5 V below the positive supply voltage. Since offset voltage trimming on the 4701 is made when the input voltage is symmetrical to the supply voltages, this internal switching does not affect a large variety of applications such as an inverting amplifier or non-inverting amplifier with a gain larger than 2.5 (5V operation), where the common mode voltage does not make excursions above this switching point. The user should however, be aware that this switching does take place if the operational amplifier is connected as a unity gain buffer and should make provision in his design to allow for input offset voltage variations.

3. The input bias and offset currents are essentially input protection diode reverse bias leakage currents, and are typically less than 1pA at room temperature. This low input bias current assures that the analog signal from the source will not be distorted by input bias currents. Normally, this extremely high input impedance of greater than $10^{12}\ \Omega$ would not be a problem as the source impedance would limit the node impedance. However, for applications where source impedance is very high, it may be necessary to limit noise and hum pickup through proper shielding.

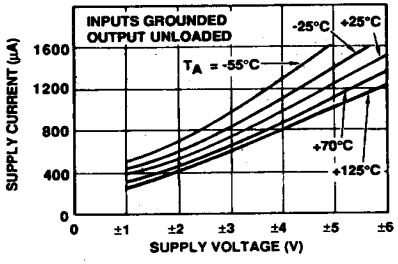
4. The output stage consists of class AB complementary output drivers, capable of driving a low resistance load. The output voltage swing is limited by the drain to source on-resistance of the output transistors as determined by the bias circuitry, and the value of the load resistor. When connected in the voltage follower configuration, the oscillation resistant feature, combined with the rail to rail input and output feature, makes an effective analog signal buffer for medium to high source impedance sensors, transducers, and other circuit networks.

5. The ALD 4701 operational amplifier has been designed to provide full static discharge protection. Internally, the design has been carefully implemented to minimize latch up. However, care must be exercised when handling the device to avoid strong static fields that may degrade a diode junction, causing increased input leakage currents. In using the operational amplifier, the user is advised to power up the circuit before, or simultaneously with, any input voltages applied and to limit input voltages to not exceed 0.3V of the power supply voltage levels.

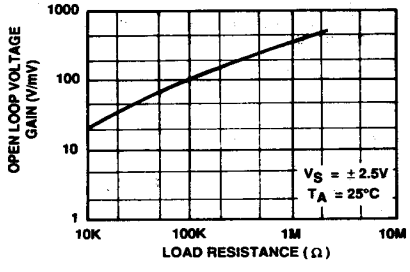
6. The ALD 4701, with its micropower operation, offers numerous benefits in reduced power supply requirements, less noise coupling and current spikes, less thermally induced drift, better overall reliability due to lower self heating, and lower input bias current. It requires practically no warm up time as the chip junction heats up to only 0.4° C above ambient temperature under most operating conditions.

## TYPICAL PERFORMANCE CHARACTERISTICS

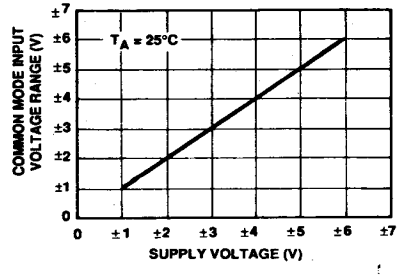
SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



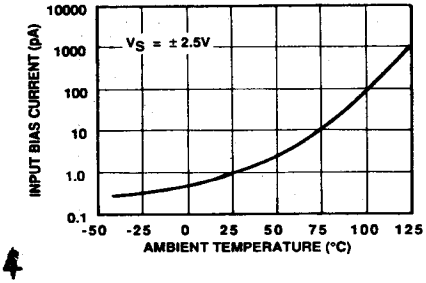

OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF LOAD RESISTANCE




COMMON MODE INPUT VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE

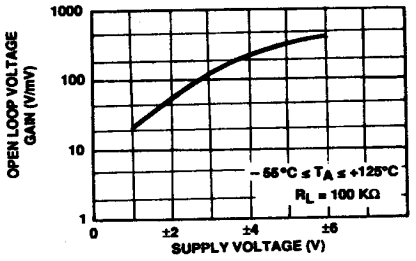



INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

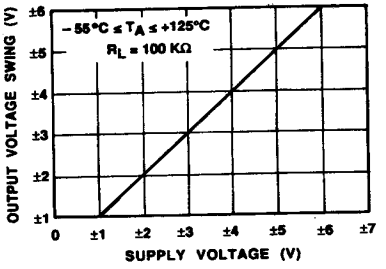


## TYPICAL PERFORMANCE CHARACTERISTICS

OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE AND TEMPERATURE

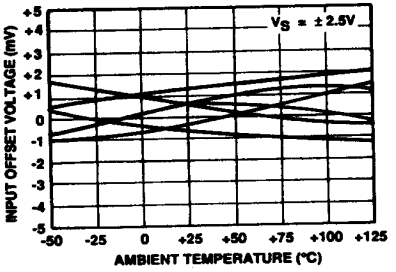



OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE

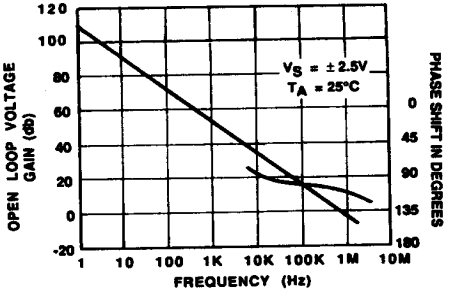



INPUT OFFSET VOLTAGE AS A FUNCTION OF AMBIENT TEMPERATURE

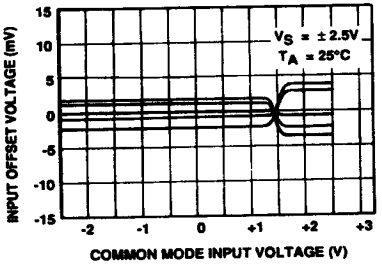
REPRESENTATIVE UNITS



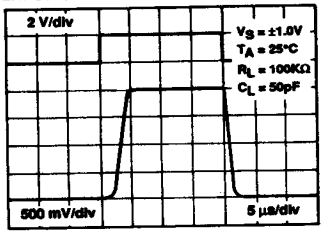

OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



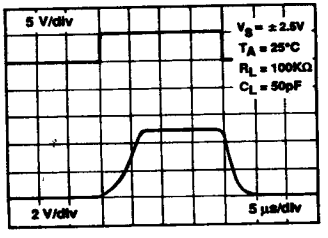

INPUT OFFSET VOLTAGE AS A FUNCTION OF COMMON MODE INPUT VOLTAGE



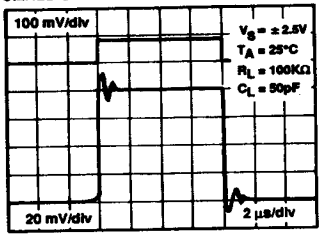

LARGE-SIGNAL TRANSIENT RESPONSE




LARGE-SIGNAL TRANSIENT RESPONSE

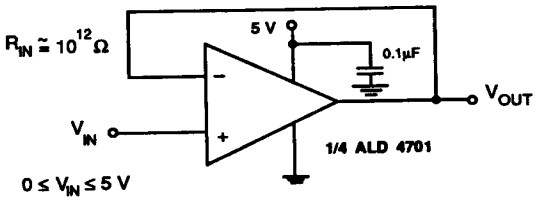



SMALL-SIGNAL TRANSIENT RESPONSE

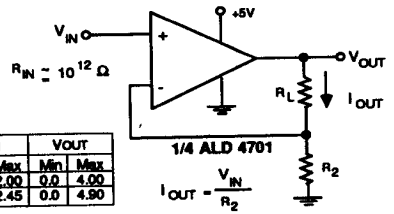


## TYPICAL APPLICATIONS

### RAIL TO RAIL VOLTAGE FOLLOWER/BUFFER

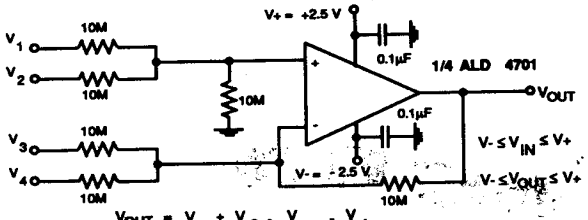



### TRANSCONDUCTANCE AMPLIFIER




| RL = R2 | VIN | | VOUT | |
|---|---|---|---|---|
| | Min | Max | Min | Max |
| 1K | 0.0 | 2.00 | 0.0 | 4.00 |
| 10K | 0.0 | 2.45 | 0.0 | 4.90 |

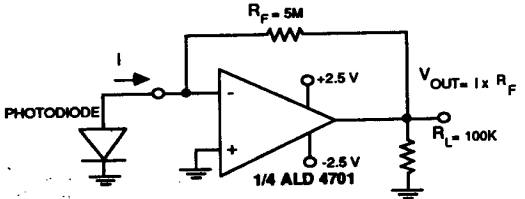
### HIGH INPUT IMPEDANCE RAIL TO RAIL PRECISION DC SUMMING AMPLIFIER



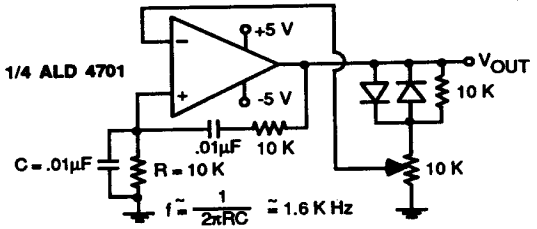

$V_{OUT} = V_1 + V_2 - V_3 - V_4$

$R_{IN}$ = 10 MΩ Accuracy limited by resistor tolerances and input offset voltage

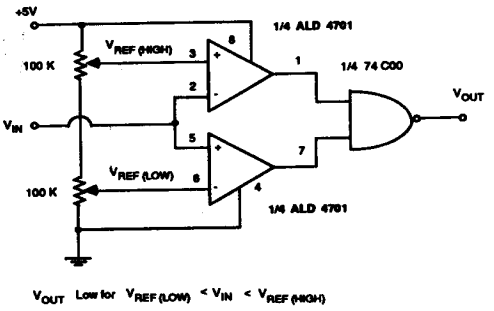
### PHOTO DETECTOR CURRENT TO VOLTAGE CONVERTER




### WIEN BRIDGE OSCILLATOR (RAIL TO RAIL) SINE WAVE GENERATOR

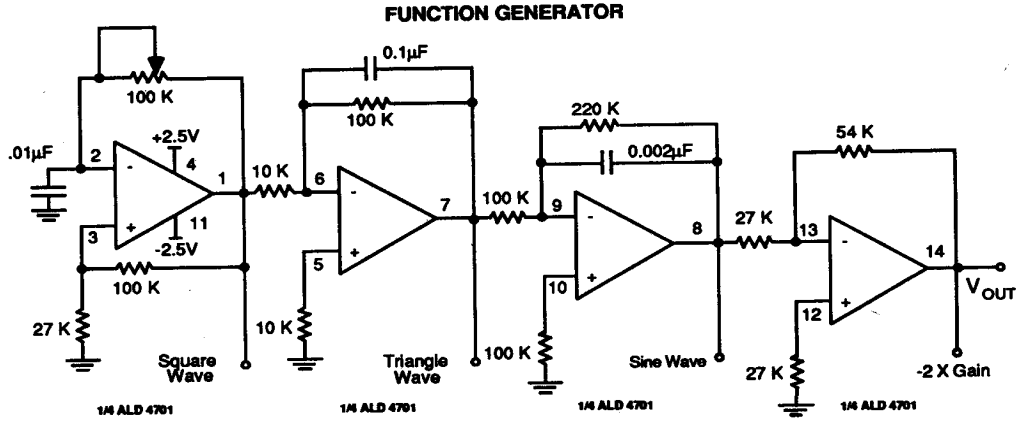



### RAIL TO RAIL WINDOW COMPARATOR




$V_{OUT}$ Low for $V_{REF (LOW)} < V_{IN} < V_{REF (HIGH)}$

### FUNCTION GENERATOR



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