Am2168/Am2169

4096 X 4 Static R/W Random-Access Memory

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- High speed — access times as fast as 40 ns
- Fully static storage and interface circuitry
- No clocks or timing signals required
- Automatic power down when deselected (Am2168)
- Power dissipation
  - Am2168: 660 mW active, 165 mW standby
    Am2169: 660 mW
- Standard 20-pin, .300 inch dual-in-line package
- Standard 20-pin rectangular ceramic leadless chip carrier
- High output drive
  - Up to seven standard TTL loads or six Schottky TTL loads
- TTL-compatible interface levels

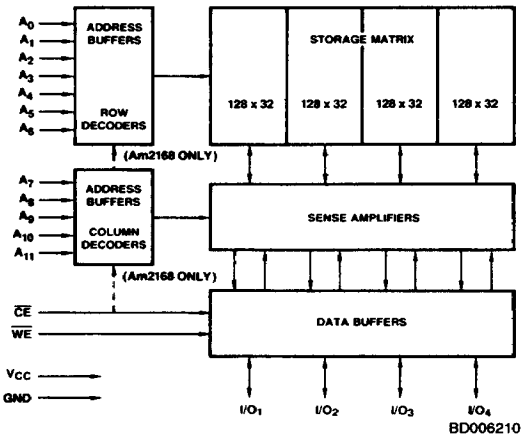
GENERAL DESCRIPTION

The Am2168 and Am2169 are high-performance, static, N-channel, read/write, random-access memories organized as 4096 words of 4 bits. Operation is from a single 5 V supply, and all input/output levels are identical to standard TTL specifications. The Am2168 and Am2169 are the same except that the Am2168 offers an automatic Chip Enable ($\overline{CE}$) power-down feature.

The Am2168 remains in a low-power standby mode as long as $\overline{CE}$ remains HIGH, thus reducing its power requirements from 660 mW to 165 mW maximum.

The data read out is not destructive and has the same polarity as the input data. The device is packaged in either a .300 slim DIP or 20-pin leadless chip carrier. The outputs of similar devices can be OR-tied and easy selection obtained by use of the $\overline{CE}$.

BLOCK DIAGRAM



PRODUCT SELECTOR GUIDE

Part Number		Am2168-35	Am2168-45	Am2169-40	Am2168-55	Am2169-50	Am2168-70	Am2169-70
Maximum Access Time (ns)		35	45	40	55	50	70	70
0 to +70°C	I_{CC} (mA)	120	120	120	120	120	120	120
	I_{SB}* (mA)	30	30	N/A	30	N/A	30	N/A
−55 to +125°C	I_{CC} (mA)	N/A	160	N/A	160	160	160	160
	I_{SB}* (mA)	N/A	30	N/A	30	N/A	30	N/A

*Am2168

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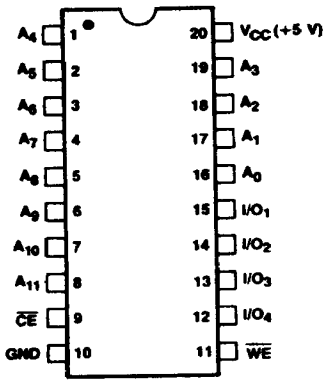
Publication #	Rev.	Amendment
04568	C	/0

Issue Date: January 1989

CONNECTION DIAGRAMS
Top View

DIPs



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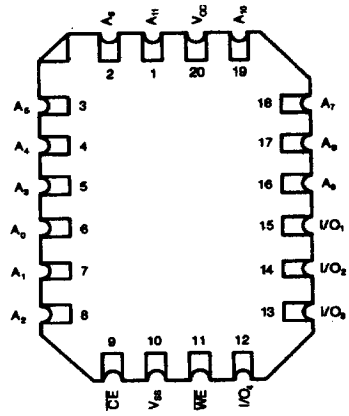
LCC



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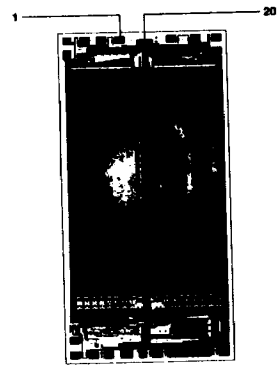
Note: Pin 1 is marked for orientation.

METALLIZATION AND PAD LAYOUT

Address Designators	
External	Internal
A_0	A_0
A_1	A_1
A_2	A_2
A_3	A_3
A_4	A_4
A_5	A_5
A_6	A_6
A_7	A_7
A_8	A_8
A_9	A_{11}
A_{10}	A_{10}
A_{11}	A_9

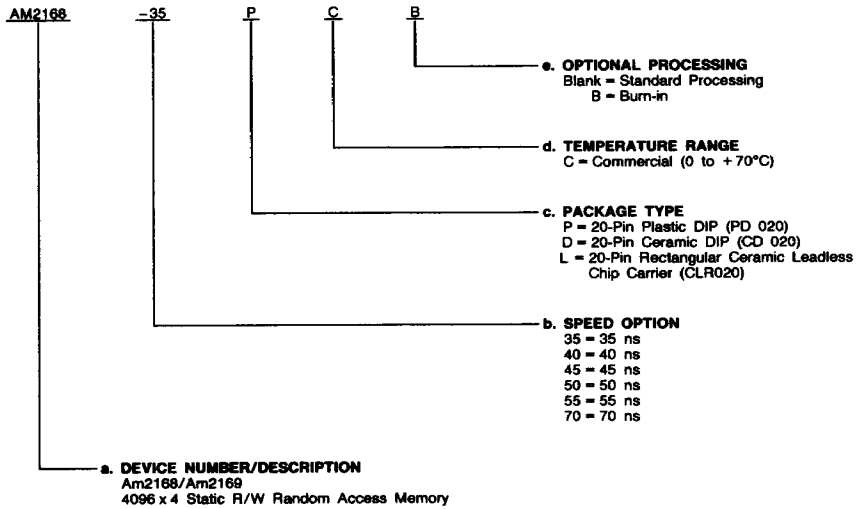


Die Size: 0.123" x 0.252"

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **a. Device Number**
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing



Valid Combinations	
AM2168-35	PC, PCB, DC, DCB, LC, LCB
AM2169-40	
AM2168-45	PC, PCB, DC, DCB
AM2168-55	
AM2169-50	
AM2168-70	
AM2169-70	

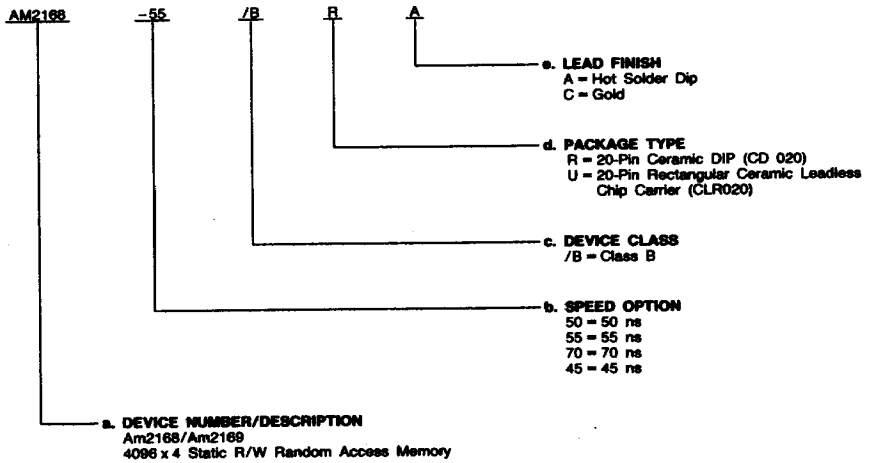
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

MILITARY ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) is formed by a combination of: **a. Device Number**
b. Speed Option (if applicable)
c. Device Class
d. Package Type
e. Lead Finish



Valid Combinations	
AM2168-45	/BRA, /BUA
AM2168-55	
AM2169-50	
AM2168-70	
AM2169-70	
AM2168-45	
AM2168-55	
AM2169-50	
AM2168-70	
AM2169-70	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

PIN DESCRIPTION

$A_0 - A_{11}$ Address Inputs (Inputs)
The address input lines select the RAM location to be read or written.

$\overline{CE}$ Chip Enable (Input, Active LOW)
The Chip Enable selects the memory device.

$\overline{WE}$ Write Enable (Input, Active LOW)
When Write Enable is LOW and Chip Enable is also LOW, data is written into the location specified on the address pins.

$I/O_1 - I/O_4$ Data In/Out Bus (Bidirectional Active HIGH)
These I/O lines provide the path for data to be read from or written to the selected memory location.

V_{CC} Power Supply

V_{SS} Ground

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage ..... −0.5 V to +7.0 V
All Signal Voltages ..... −3.5 V to +7.0 V
DC Output Current ..... 20 mA
Power Dissipation
  Cerdip & Leadless Packages ..... 1.2 W
  Plastic Packages ..... 0.7 W
Ambient Temperature with Power Applied
  Cerdip & Leadless Packages ..... −55 to +125°C
  Plastic Packages ..... −10 to +85°C
Storage Temperature
  Cerdip & Leadless Packages ..... −65 to +150°C
  Plastic Packages ..... −55 to +150°C

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

*Maximum ratings are for system design reference; parameters given may not be 100% tested.

OPERATING RANGES (Note 4)

Commercial (C) Devices
  Ambient Temperature (T_A) ..... 0 to +70°C
  Supply Voltage (V_{CC}) ..... 4.5 V to +5.5 V

Military (M) Devices
  Ambient Temperature (T_A) ..... −55 to +125°C
  Supply Voltage (V_{CC}) ..... +4.5 to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating ranges unless otherwise specified (for APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted) (Note 4)

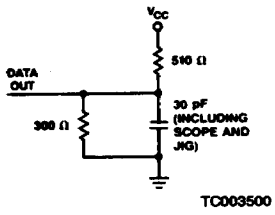
Parameter Symbol	Parameter Description	Test Conditions		Am2168-35, -45, & -40 Min.	Am2168-35, -45, & -40 Max.	Am2168-55 & -70 Am2169-50 & -70 Min.	Am2168-55 & -70 Am2169-50 & -70 Max.	Unit
I_{OH}	Output HIGH Current	V_{OH} = 2.4 V	V_{CC} = 4.5 V	−4		−4		mA
I_{OL}	Output LOW Current	V_{OL} = 0.4 V	COM'L	8		8		mA
			MIL	8		8		
V_{IH}	Input HIGH Voltage			2.2	6.0	2.2	6.0	V
V_{IL}	Input LOW Voltage	Note 3		−0.5	0.8	−0.5	0.8	V
I_{IX}	Input Load Current	$GND \leq V_I \leq V_{CC}$		−10	10	−10	10	μA
I_{OZ}	Output Leakage Current	$GND \leq V_O \leq V_{CC}$ Output Disabled		−50	50	−50	50	μA
C_I	Input Capacitance	Test Frequency = 1.0 MHz T_A = 25°C, All Pins at 0 V, V_{CC} = 5 V (Note 5)			5		5	pF
$C_{I/O}$	Input/Output Capacitance				7		7	
I_{CC}	V_{CC} Operating Supply Current	Max. V_{CC}, $CE \leq V_{IL}$ Output Open	COM'L		120		120	mA
			MIL		N/A		160	
I_{SB}	Automatic $\overline{CE}$ Power Down Current (Am2168 Only)	Max. V_{CC}, ($CE \geq V_{IH}$)	COM'L		30		30	mA
			MIL		N/A		30	

Notes:
1. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V and output loading of the specified I_{OL}/I_{OH} and 30 pF load capacitance. Output timing reference is 1.5 V.
2. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
3. V_{IL} voltages of less than −0.5 V on the I/O pins will cause the output current to exceed the maximum rating and thus should not exceed 30 seconds in duration.
4. For test and correlation purposes, ambient temperature is defined as the "Instant-on" case temperature.
5. At any given temperature and voltage condition, t_{HZ} is less than t_{LZ} and t_{WZ} is less than t_{OW} for all devices. Transition is measured at 1.5 V on the input to V_{OH} −500 mV and V_{OL} +500 mV on the outputs using the load shown in B. under Switching Test Circuits. C_L = 5 pF.
6. Not 100% tested parameter; parameter guaranteed by characterization.

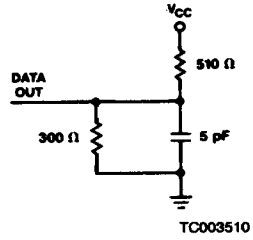
SWITCHING CHARACTERISTICS over operating ranges unless otherwise specified (for APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted) (Note 1)

No.	Parameter Symbol	Parameter Description			Am2168-35 Min.	Am2168-35 Max.	Am2168-45, Am2169-40 Min.	Am2168-45, Am2169-40 Max.	Am2168-55, Am2169-50 Min.	Am2168-55, Am2169-50 Max.	Am2168-70, Am2169-70 Min.	Am2168-70, Am2169-70 Max.	Unit
READ CYCLE													
1	t_{RC}	Address Valid to Address Do Not Care Time (Read Cycle Time)			35		40		50		70		ns
2	t_{AA}	Address Valid to Data Out Valid Delay (Address Access Time)				35		40		50		70	ns
3	t_{ACS}	Chip Enable LOW to Data Out Valid (Chip Enable Access Time)	Am2168			35		45		55		70	ns
			Am2169					20		25		30	
4	t_{LZ}	Chip Enable LOW to Data Out On	Am2168	(Notes 4, 5)	5		5		5		5		
			Am2169				2		2		2		
5	t_{HZ}	Chip Enable HIGH to Data Out Off		(Notes 4, 5)	0	20	0	20	0	25	0	30	ns
6	t_{OH}	Output hold time from address change	COM'L		3		3		3		3		
			MIL				1		1		1		
7	t_{PD}	Chip Enable HIGH to Power-Down Delay	Am2168	(Note 5)		35		45		55		70	ns
8	t_{PU}	Chip Enable LOW to Power-Up Delay	Am2168	(Note 5)	0		0		0		0		ns
WRITE CYCLE													
9	t_{WC}	Address Valid to Address Do Not Care (Write Cycle Time)			35		40		50		70		ns
10	t_{WP}	Write Enable LOW to Write Enable HIGH		(Note 2)	30		35		45		65		ns
11	t_{WR}	Write Enable HIGH to Address Do Not Care			0		0		0		0		ns
12	t_{WZ}	Write Enable LOW to Output in Hi-Z		(Notes 4, 5)	0	15	0	15	0	20	0	25	ns
13	t_{DW}	Data In Valid to Write Enable HIGH			20		20		25		35		ns
14	t_{DH}	Data Hold Time			5		5		5		5		ns
15	t_{AS}	Address Valid to Write Enable LOW			0		0		0		0		ns
16	t_{CW}	Chip Enable LOW to Write Enable HIGH		(Note 2)	30		35		45		65		ns
17	t_{OW}	Write Enable HIGH to Output in Low-Z		(Notes 4, 5)	0		0		0		0		ns
18	t_{AW}	Address Valid to End of Write			30		35		45		65		ns

SWITCHING TEST CIRCUITS



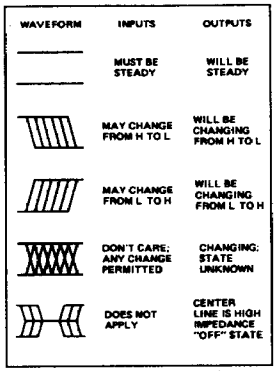
A. Output Load



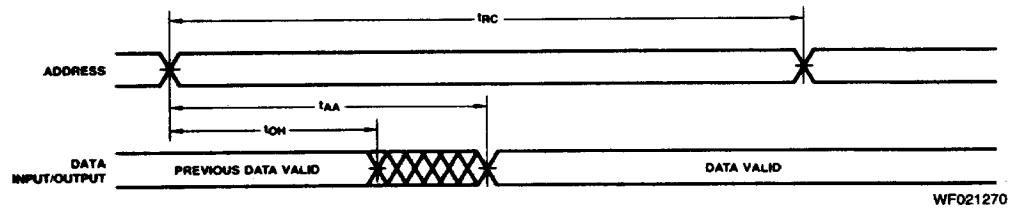
B. Output Load for t_{HZ}, t_{LZ}, t_{OW}, t_{WZ}

SWITCHING WAVEFORMS

KEY TO SWITCHING WAVEFORMS

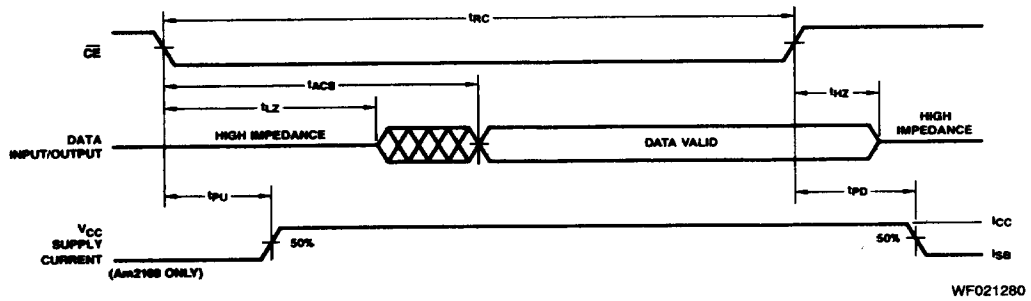


KS000010



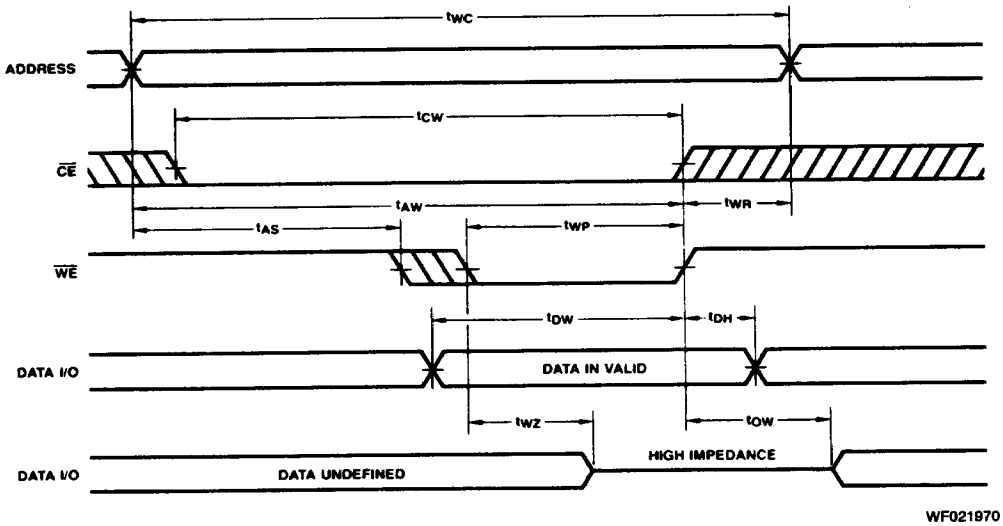
WF021270

Read Cycle No. 1 ($\overline{WE}$ HIGH, $\overline{CE}$ LOW)

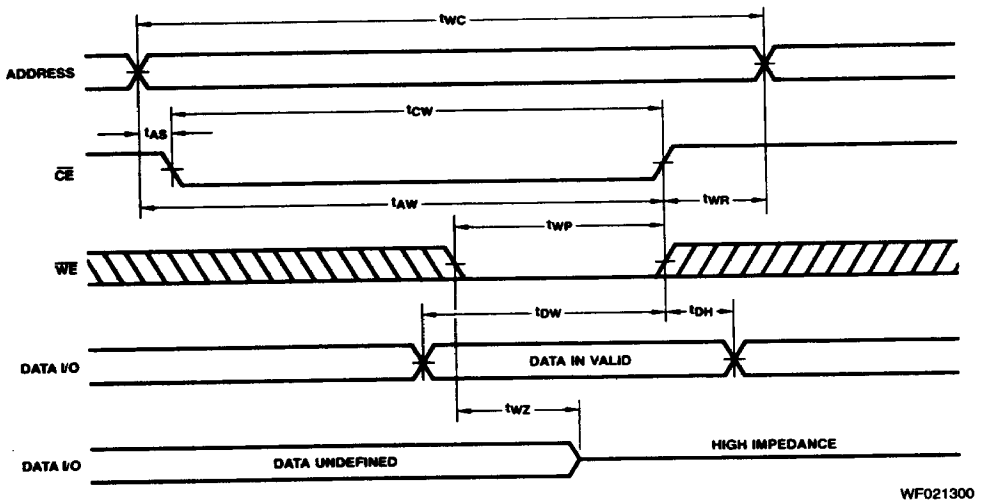


WF021280

Read Cycle No. 2 ($\overline{WE}$ HIGH, Address Valid Prior to $\overline{CE}$ Transition to LOW)



Write Cycle No. 1 ($\overline{WE}$ Controlled)

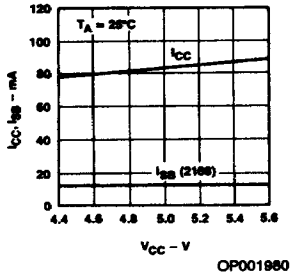


Write Cycle No. 2 ($\overline{CE}$ Controlled)

Note: If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

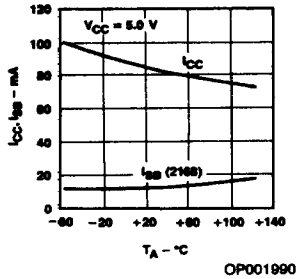
TYPICAL PERFORMANCE CURVES

Supply Current versus Supply Voltage



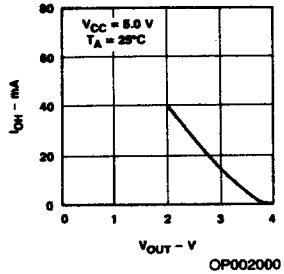
OP001980

Supply Current versus Ambient Temperature



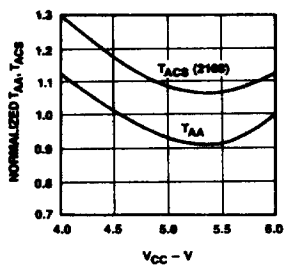
OP001990

Output Source Current versus Output Voltage



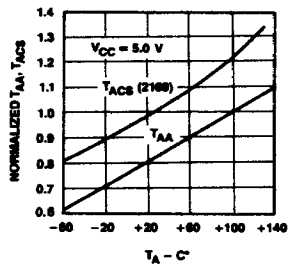
OP002000

Normalized Access Time versus Supply Voltage



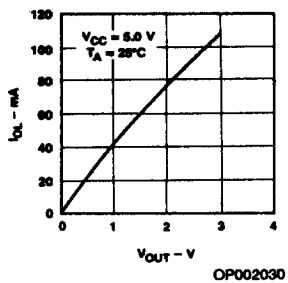
OP002010

Normalized Access Time versus Ambient Temperature



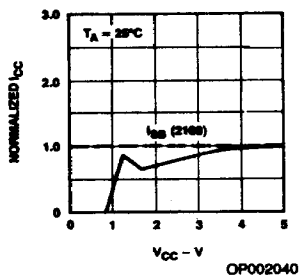
OP002020

Output Sink Current versus Output Voltage



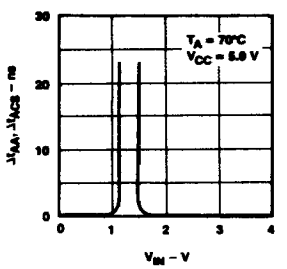
OP002030

Typical Power-On Current versus Power Supply



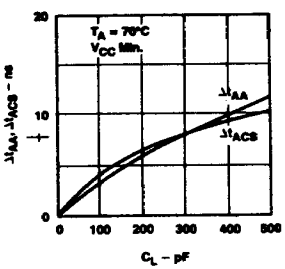
OP002040

Access Time Change versus Input Voltage



OP002050

Access Time Change versus Output Loading



OP002060

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