Am2147/Am21L47

4096x1 Static RAM

DISTINCTIVE CHARACTERISTICS

- High speed — access times down to 35 ns maximum
- Automatic power-down when deselected
- Low power dissipation
- High output drive
- TTL compatible interface levels
- No power-on current surge

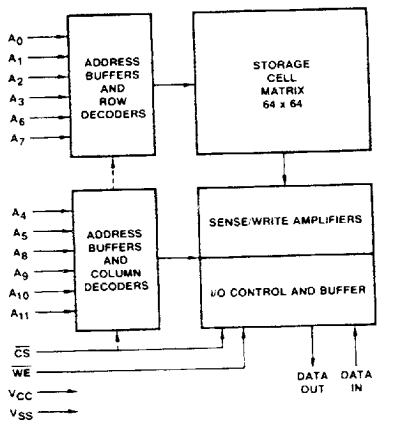
GENERAL DESCRIPTION

The Am2147/Am21L47 Series are high-performance, 4096 x 1-bit, static, read/write, random-access memories. It is organized as 4096 words by one bit per word. All interface signal levels are identical to TTL specifications, providing good noise immunity and simplified system design. All inputs are purely capacitive MOS loads. The outputs will drive up to seven standard TTL loads or up to six Schottky TTL loads.

Only a single +5-volt power supply is required. When deselected ($\overline{CS} \geq V_{IH}$), the Am2147 automatically enters a power-down mode which reduces power dissipation by more than 85%. When selected, the chip powers up again with no access time penalty.

Data In and Data Out use separate pins on the standard 18-pin package. Data Out is the same polarity as Data In. Data Out is a three-state signal allowing wired-or operation of several chips. Data In and Data Out may be connected together for operation in a common data bus environment.

BLOCK DIAGRAM



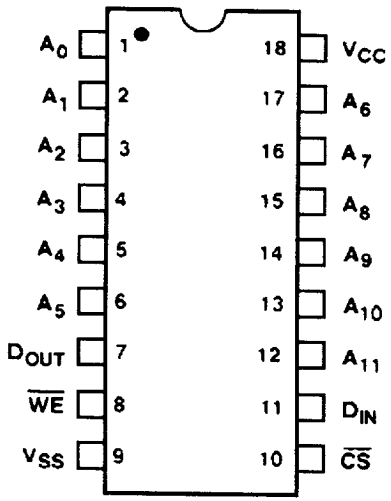
BD000051

PRODUCT SELECTOR GUIDE

Part Number	Am2147-35	Am2147-45	Am21L47-45	Am2147-55	Am21L47-55	Am2147-70	Am21L47-70
Maximum Access time (ns)	35	45	45	55	55	70	70
Maximum Active Current (mA)	180	180	125	180	125	160 (180 mil)	125
Maximum Standby Current (mA)	30	30	15	30	15	20 (30 mil)	15
Full Military Operating Range Version		Yes		Yes		Yes	

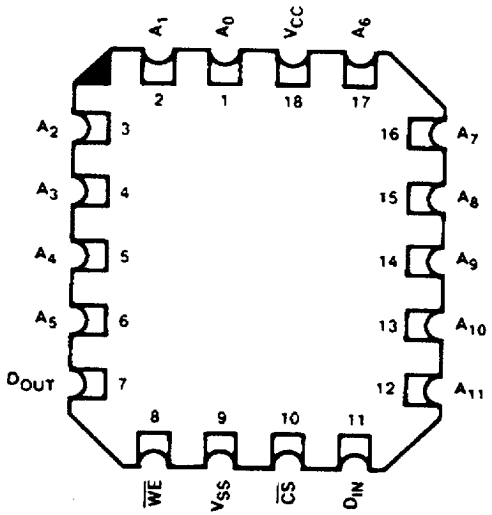
CONNECTION DIAGRAMS
Top View

DIPs*



CD000091

LCC



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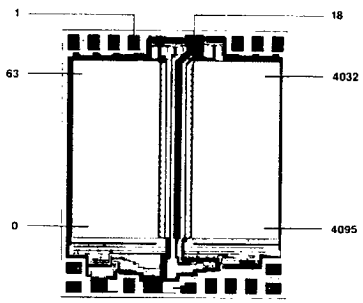
*Also available for military customers in an 18-Pin Ceramic Flatpack. Pinout is identical to DIPs.

Note: Pin 1 is marked for orientation.

BIT MAP

Address Designators	
External	Internal
A_0	A_2
A_1	A_5
A_2	A_4
A_3	A_3
A_4	A_8
A_5	A_7
A_6	A_1
A_7	A_0
A_8	A_{11}
A_9	A_9
A_{10}	A_{10}
A_{11}	A_6

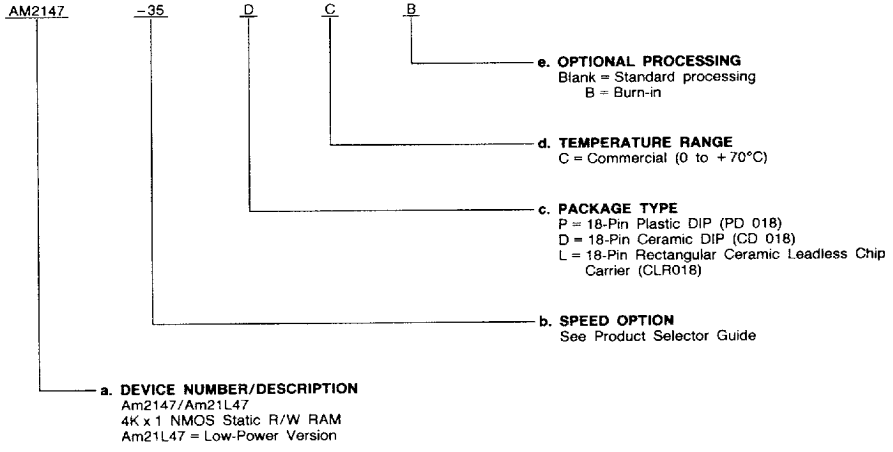


Die Size: 0.130 x 0.106

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **a. Device Number**
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing



Valid Combinations	
AM2147-35	PC, PCB, DC, DCB, LC, LCB
AM2147-45	
AM2147-55	
AM2147-70	
AM21L47-45	
AM21L47-55	
AM21L47-70	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult MSIS sales department to confirm availability of specific valid combinations, and to obtain additional data on MSIS's standard military grade products.

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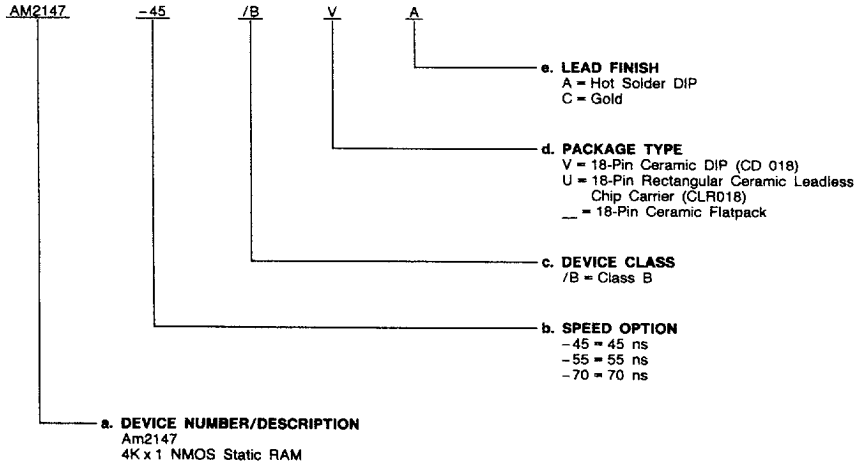
MILITARY ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) is formed by a combination of: **a. Device Number**
b. Speed Option (if applicable)
c. Device Class
d. Package Type
e. Lead Finish



Valid Combinations	
AM2147-45	/BVA
AM2147-55	
AM2147-70	
AM2147-45	/BUC
AM2147-55	
AM2147-70	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult MSIS sales department to confirm availability of specific valid combinations, and to obtain additional data on MSIS's standard military grade products.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

PIN DESCRIPTION

$A_0 - A_{11}$ Address Inputs
The address input lines select the RAM location to be read or written.

$\overline{CS}$ Chip Select (Input, Active LOW)
The Chip Select selects the memory device.

$\overline{WE}$ Write Enable (Input, Active LOW)
When $\overline{WE}$ is LOW and $\overline{CS}$ is also LOW, data is written into the location specified on the address pins.

D_{IN} Data In (Input)
This pin is used for entering data during write operations.

D_{OUT} Data Out (Output, Three-State)
This pin is three state during write operations. It becomes active when $\overline{CS}$ is LOW and $\overline{WE}$ is HIGH.

V_{CC} Power Supply

V_{SS} Ground

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Ambient Temperature with
Power Applied ..... −55 to +125°C
Supply Voltage ..... −0.5 V to +7.0 V
Signal Voltages with
respect to ground ..... −3.5 V to +7.0 V
Power Dissipation ..... 1.2 W
DC Output Current ..... 20. mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Absolute Maximum Ratings are for system-design reference; parameters given are not 100% tested.

OPERATING RANGES

Commercial (C) Devices
Ambient Temperature (T_A) ..... 0 to +70°C
Supply Voltage (V_{CC}) ..... +4.5 V to +5.5 V

Military (M) Devices
Ambient Temperature (T_A)* ..... −55 to +125°C
Supply Voltage V_{CC} ..... +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

*T_A is defined as the "instant on" case temperature.

DC CHARACTERISTICS over operating ranges unless otherwise specified (for APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions		Am2147-35 Am2147-45 Am2147-55		Am21L47-45 Am21L47-55 Am21L47-70		Am2147-70		Unit
				Min.	Max.	Min.	Max.	Min.	Max.	
I_{OH}	Output High Current	V_{OH} = 2.4 V	V_{CC} = 4.5 V	−4		−4		−4		mA
I_{OL}	Output Low Current	V_{OL} = 0.4 V	T_A = 70°C	12		12		12		mA
			T_A = 125°C	8		N/A		8		
V_{IH}	Input High Voltage			2.0	6.0	2.0	6.0	2.0	6.0	V
V_{IL}	Input Low Voltage			−2.5	0.8	−2.5	0.8	−2.5	0.8	V
I_{IX}	Input Load Current	$V_{SS} \leq V_I \leq V_{CC}$		−10	10	−10	10	−10	10	μA
I_{OZ}	Output Leakage Current	$GND \leq V_O \leq V_{CC}$ Output Disables	T_A = −55 to+ 125°C	−50	50	−50	50	−50	50	μA
C_I	Input Capacitance	Test Frequency = 1.0 MHz (Note 4) T_A = 25°C, All pins at 0 V, V_{CC} = 5 V			5		5		5	pF
C_O	Output Capacitance				6		6		6	
I_{CC}	V_{CC} Operating Supply Current	Max. V_{CC} $\overline{CS} \leq V_{IL}$ Output Open	T_A = 0 to 70°C		180		125		160	mA
			T_A = −55 to 125°C		180		N/A		180	
I_{SB}	Automatic $\overline{CS}$ Power Down Current	Max. V_{CC}, ($\overline{CS} \geq V_{IH}$) (Note 3)	T_A = 0 to 70°C		30		15		20	mA
			T_A = −55 to +125°C		30		N/A		30	

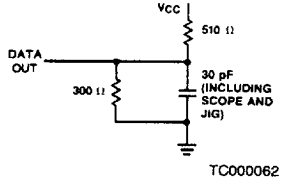
Notes:
1. Test conditions assume signal transition times of 10 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V and output loading of the specified I_{OL}/I_{OH} and 30 pF load capacitance. Output timing reference is 1.5 V.
2. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{WE}$ LOW. Both signals must be low to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
3. A pull-up resistor to V_{CC} on the $\overline{CS}$ input is required to keep the device deselected during V_{CC} power up. Otherwise I_{SB} will exceed values given.
4. These parameters are not 100% tested, but guaranteed by characterization.
5. Chip deselected greater than 55 ns prior to selection.
6. Chip deselected less than 55 ns prior to selection.
7. Transition is measured at 1.5 V on the input to V_{OH} − 500 mV and V_{OL} + 500 mV on the outputs using the load shown in Figure B under Switching Test Circuit.
8. $\overline{WE}$ is HIGH for read cycle.
9. Device is continuously selected, $\overline{CS} = V_{IL}$.
10. Address valid prior to or coincident with $\overline{CS}$ transition LOW.

SWITCHING CHARACTERISTICS over operating ranges unless otherwise specified (Note 1) (for APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted)

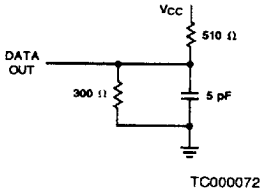
No.	Parameter Symbol	Parameter Description		Am2147-35		Am2147-45 Am21L47-45		Am2147-55 Am21L47-55		Am2147-70 Am21L47-70		Unit
				Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE												
1	t_{RC}	Address Valid to Address Do Not Care Time (Read Cycle Time)		35		45		55		70		ns
2	t_{AA}	Address Valid to Data Out Valid Delay (Address Access Time)			35		45		55		70	ns
3	t_{ACS1}	Chip Select LOW to Data Out Valid	(Note 5)		35		45		55		70	ns
4	t_{ACS2}		(Note 6)		35		45		65		80	
5	t_{LZ}	Chip Select LOW to Data Out On (Notes 4 & 7)		5		5		5		5		ns
6	t_{HZ}	Chip Select HIGH to Data Out Off (Notes 4 & 7)		0	30	0	30	0	30	0	40	ns
7	t_{OH}	Output hold after address change		5		5		5		5		ns
8	t_{PD}	Chip Select HIGH Power Down Delay (Note 4)			20		20		20		30	ns
9	t_{PU}	Chip Select LOW to Power Up Delay (Note 4)		0		0		0		0		ns
WRITE CYCLE												
10	t_{WC}	Address Valid to Address Do Not Care (Write Cycle Time)		35		45		55		70		ns
11	t_{WP}	Write Enable LOW to Write Enable High (Note 2)		20		25		25		40		ns
12	t_{WR}	Write Enable HIGH to Address		0		0		10		15		ns
13	t_{WZ}	Write Enable LOW to Output in Hi Z (Notes 4 & 7)		0	20	0	25	0	25	0	35	ns
14	t_{DW}	Data In Valid to Write Enable HIGH		20		25		25		30		ns
15	t_{DH}	Data Hold Time		10		10		10		10		ns
16	t_{AS}	Address Valid to Write Enable LOW		0		0		0		0		ns
17	t_{CW}	Chip Select LOW to Write Enable HIGH (Note 2)		35		45		45		55		ns
18	t_{OW}	Write Enable HIGH to Output in Low Z (Notes 4 & 7)		0		0		0		0		ns
19	t_{AW}	Address Valid to End of Write		35		45		45		55		ns

Notes: See notes following DC Characteristics table.

SWITCHING TEST CIRCUITS



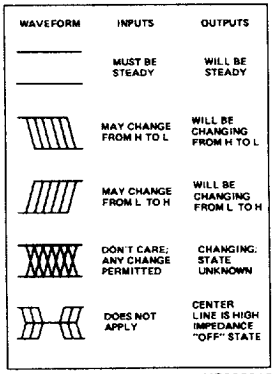
A. Output Load



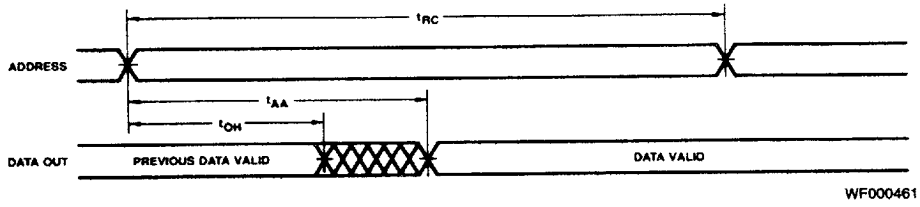
B. Output Load for t_{HZ}, t_{LZ}, t_{OW}, t_{WZ}

SWITCHING WAVEFORMS

KEY TO SWITCHING WAVEFORMS

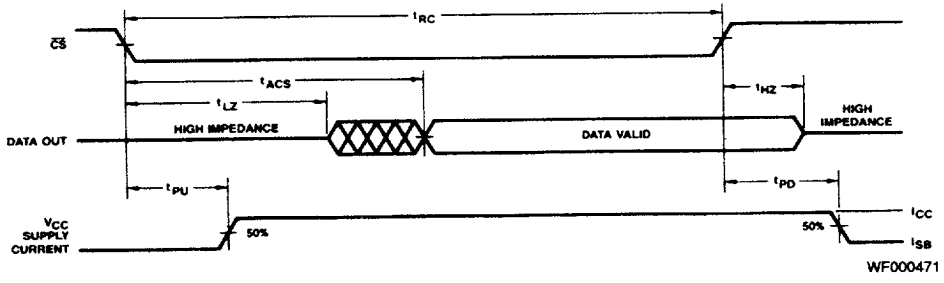


KS000010



WF000461

Read Cycle No. 1 (Notes 8, 9)

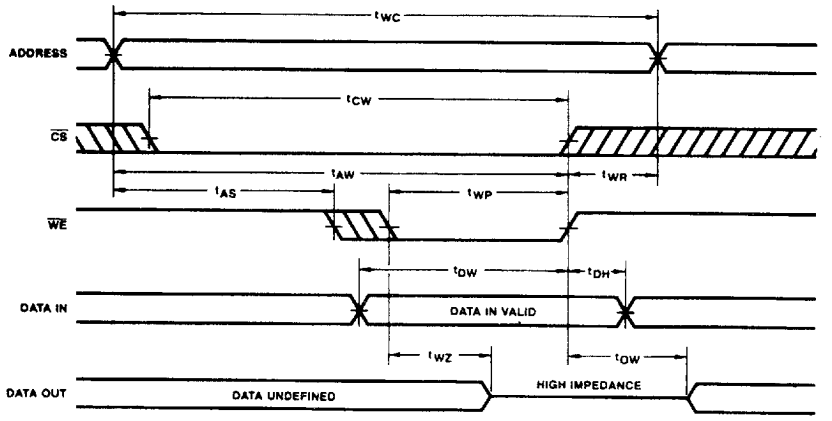


WF000471

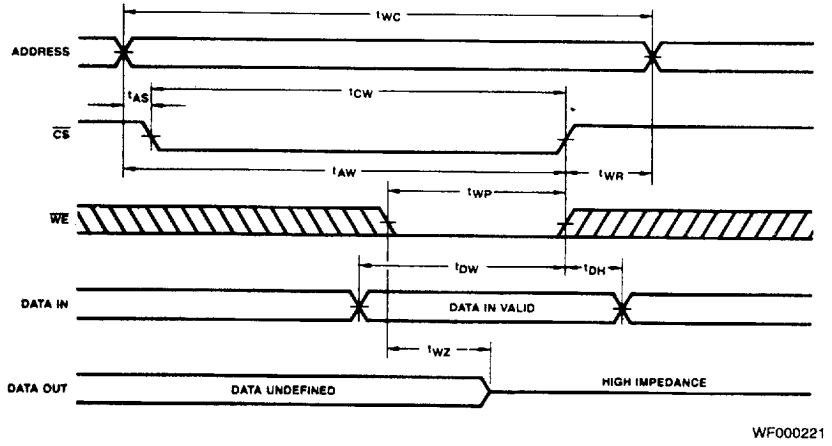
Read Cycle No. 2 (Notes 8, 10)

Notes: See notes following DC Characteristics table.

SWITCHING WAVEFORMS (Cont'd.)



Write Cycle No. 1 ($\overline{WE}$ Controlled)

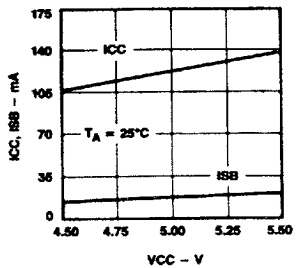


Write Cycle No. 2 ($\overline{CS}$ Controlled)

Note: If $\overline{CS}$ goes HIGH simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.

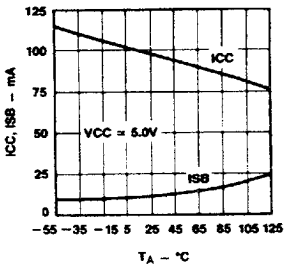
TYPICAL PERFORMANCE CURVES

Supply Current Versus Supply Voltage



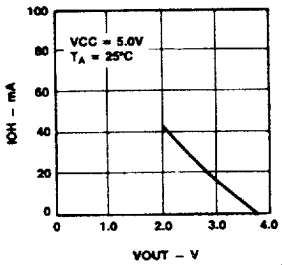
OP000430

Supply Current Versus Ambient Temperature



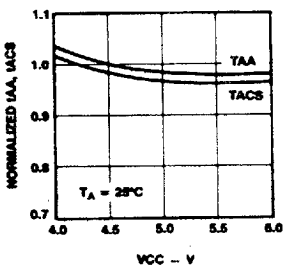
OP000440

Output Source Current Versus Output Voltage



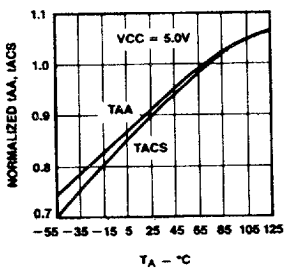
OP000220

Normalized Access Time Versus Supply Voltage



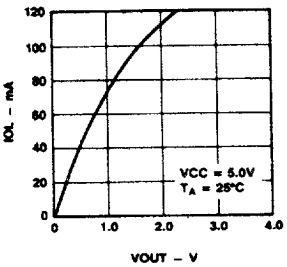
OP000760

Normalized Access Time Versus Ambient Temperature



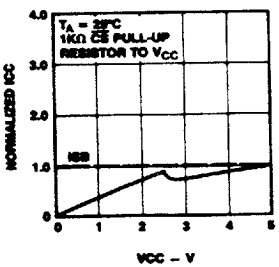
OP000230

Output Sink Current Versus Output Voltage



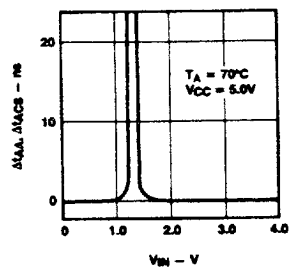
OP000240

Typical Power-On Current Versus Power Supply



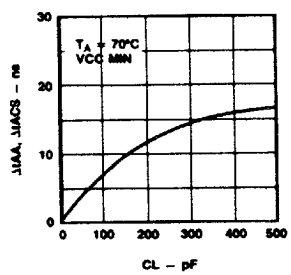
OP000870

Access Time Change Versus Input Voltage



OP000800

Access Time Change Versus Output Loading



OP000270

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