

Am2148/Am2149

Am21L48/Am21L49

1024x4 Static RAM



DISTINCTIVE CHARACTERISTICS

- High speed — access times as fast as 35 ns
- Fully static storage and interface circuitry
- Automatic power-down when deselected (Am2148)
- TTL-compatible interface levels
- Low power dissipation
 - Am2148: 990 mW active, 165 mW power down
 - Am21L48: 688 mW active, 110 mW power down
- High output drive
 - Up to seven standard TTL loads

GENERAL DESCRIPTION

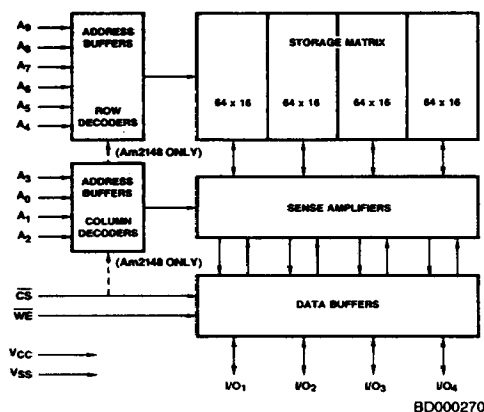
The Am2148 and Am2149 are high-performance, static, N-Channel, read/write, random-access memories, organized as 1024 x 4. Operation is from a single 5-V supply, and all input/output levels are identical to standard TTL specifications. The Am2148 and Am2149 are the same except that the Am2148 offers an automatic $\overline{CS}$ power-down feature.

The Am2148 remains in a low-power standby mode as long as $\overline{CS}$ remains HIGH, thus reducing its power requirements.

The Am2148 power decreases from 990 mW to 165 mW in the standby mode. The $\overline{CS}$ input does not affect the power dissipation of the Am2149.

Data readout is not destructive and has the same polarity as data input. $\overline{CS}$ provides for easy selection of an individual package when the outputs are OR-tied.

BLOCK DIAGRAM

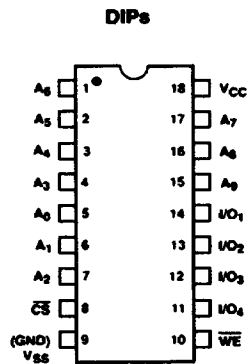


PRODUCT SELECTOR GUIDE

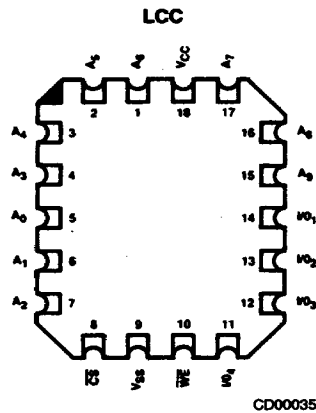
Part Number		Am2148/9 -35	Am2148/9 -45	Am21L48/9 -45	Am2148/9 -55	Am21L48/9 -55	Am2148/9 -70	Am21L48/9 -70
Maximum Access Time (ns)		35	45	45	55	55	70	70
I_{CC} Max. (mA)	0 to +70°C	180	180	125	180	125	180	125
I_{SB}^* Max. (mA)		30	30	20	30	20	30	20
I_{CC} Max. (mA)	-55 to +125°C	N/A	180	N/A	180	N/A	180	N/A
I_{SB}^* Max. (mA)		N/A	30	N/A	30	N/A	30	N/A

*Am2148 and Am21L48 only.

CONNECTION DIAGRAMS Top View



CD000171

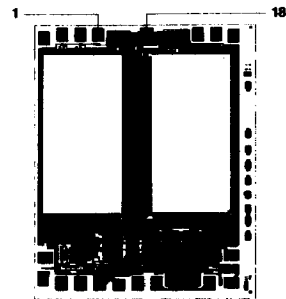


CD000350

Note: Pin 1 is marked for orientation.

METALLIZATION AND PAD LAYOUT

Address Designators	
External	Internal
A ₀	A ₇
A ₁	A ₈
A ₂	A ₉
A ₃	A ₆
A ₄	A ₅
A ₅	A ₄
A ₆	A ₃
A ₇	A ₂
A ₈	A ₁
A ₉	A ₀



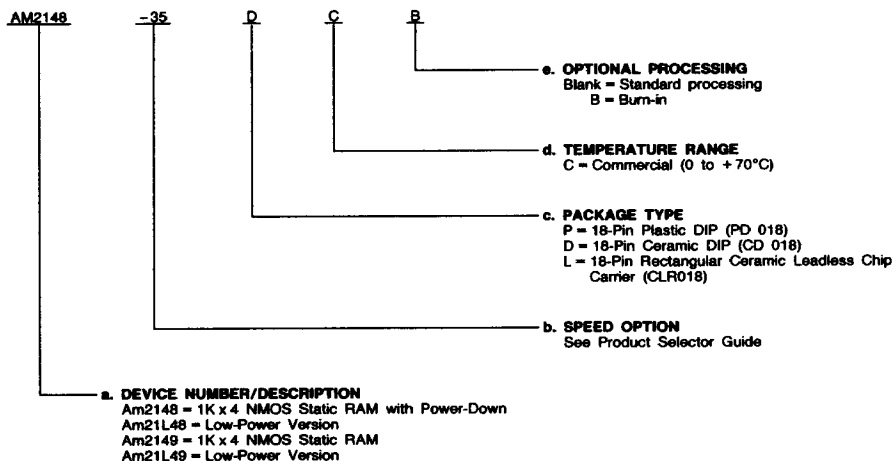
Die Size: 0.107" x 0.145"

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

- a. **Device Number**
- b. **Speed Option** (if applicable)
- c. **Package Type**
- d. **Temperature Range**
- e. **Optional Processing**



Valid Combinations	
AM2148-35	PC, PCB, DC, DCB, LC, LCB
AM2149-35	
AM21L48-45	
AM21L49-45	
AM21L48-55	
AM21L49-55	
AM21L48-70	
AM21L49-70	PC, PCB, DC, DCB, LC, LCB
AM2148-45	
AM2149-45	
AM2148-55	
AM2149-55	
AM2148-70	
AM2149-70	

Valid Combinations

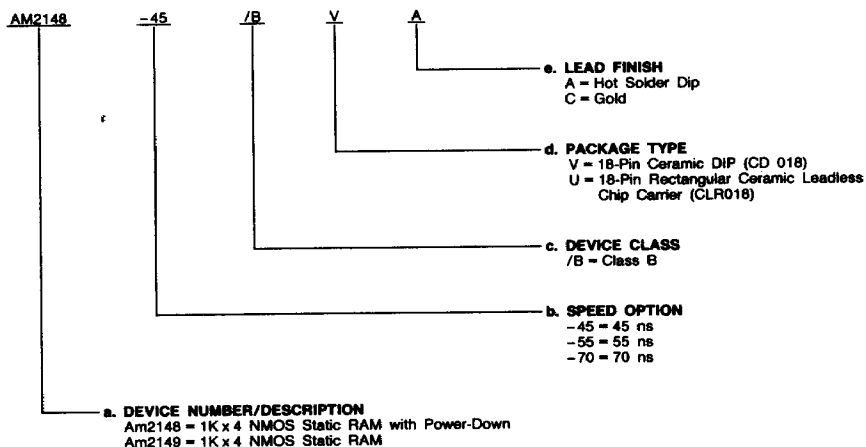
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released valid combinations, and to obtain additional data on AMD's standard military grade products.

MILITARY ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) is formed by a combination of:

- a. **Device Number**
- b. **Speed Option** (if applicable)
- c. **Device Class**
- d. **Package Type**
- e. **Lead Finish**



Valid Combinations	
AM2148-45	/BVA
AM2149-45	
AM2148-55	
AM2149-55	
AM2148-70	
AM2149-70	/BUC
AM2148-45	
AM2149-45	
AM2148-55	
AM2149-55	
AM2148-70	
AM2149-70	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

Group A Tests

Group A Tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

PIN DESCRIPTION

A₀ - A₉ Address Inputs

The address input lines select the RAM location to be read or written.

CS Chip Select (Input, Active LOW)

The Chip Select selects the memory device.

WE Write Enable (Input, Active LOW)

When WE is LOW and CS is also LOW, data is written into the location specified on the address pins.

I/O₁ - I/O₄ Data In/Out Bus (Bidirectional, Active HIGH)

These I/O lines provide the path for data to be read from or written to the selected memory location.

V_{CC} Power Supply

V_{SS} Ground

ABSOLUTE MAXIMUM RATINGS

Storage Temperature -65 to +150°C
 Ambient Temperature with
 Power Applied -55 to +125°C
 Supply Voltage -0.5 V to +7.0 V
 Signal Voltages with
 Respect to Ground -3.5 V to +7.0 V
 Power Dissipation 1.2 W
 DC Output Current 20 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Absolute Maximum Ratings are for system-design reference; parameters given are not 100% tested.

OPERATING RANGES

Commercial (C) Devices
 Ambient Temperature (T_A) 0 to +70°C
 Supply Voltage (V_{CC}) +4.5 V to +5.5 V
 Military (M) Devices
 Ambient Temperature (T_A) -55 to +125°C
 Supply Voltage (V_{CC}) +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

* T_A is defined as the "instant on" case temperature.

DC CHARACTERISTICS over operating ranges unless otherwise specified (for APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions		Standard		Low Power		Unit
				Min.	Max.	Min.	Max.	
I_{OH}	Output HIGH Current	$V_{OH} = 2.4 \text{ V}$	$V_{CC} = 4.5 \text{ V}$	-4		-4		mA
I_{OL}	Output LOW Current	$V_{OL} = 0.4 \text{ V}$	$T_A = 70^\circ\text{C}$	8		8		mA
			$T_A = 125^\circ\text{C}$	8		N/A		
V_{IH}	Input HIGH Voltage			2.0	6.0	2.0	6.0	V
V_{IL}	Input LOW Voltage			-0.5	0.8	-0.5	0.8	V
I_{IX}	Input Load Current	$V_{SS} < V_I < V_{CC}$		-10	10		10	μA
I_{OZ}	Output Leakage Current	$GND < V_O < V_{CC}$ Output Disabled	$T_A = -55 \text{ to} +125^\circ\text{C}$	-50	50	-50	50	μA
C_I	Input Capacitance	Test Frequency = 1.0 MHz $T_A = 25^\circ\text{C}$, All Pins at 0 V, $V_{CC} = 5 \text{ V}$ (Note 12)			5		5	pF
$C_{I/O}$	Input/Output Capacitance				7		7	
I_{CC}	V_{CC} Operating Supply Current	Max. V_{CC} , $\overline{CS} < V_{IL}$ Output Open	$T_A = 0 \text{ to} +70^\circ\text{C}$		180		125	mA
			$T_A = -55 \text{ to} +125^\circ\text{C}$		180		N/A	
I_{SB}	Automatic $\overline{CS}$ Power Down Current	Max. V_{CC} , ($\overline{CS} > V_{IH}$)	$T_A = 0 \text{ to} +70^\circ\text{C}$		30		20	mA
			$T_A = -55 \text{ to} +125^\circ\text{C}$		30		N/A	
I_{PO}	Peak Power-On Current	Max. V_{CC} , ($\overline{CS} > V_{IH}$) (Notes 3 & 12)	$T_A = 0 \text{ to} +70^\circ\text{C}$		50		30	mA
			$T_A = -55 \text{ to} +125^\circ\text{C}$		50		N/A	
I_{OS}	Output Short-Circuit Current	$GND < V_O < V_{CC}$ (Notes 11, 12)	$T_A = 0 \text{ to} +70^\circ\text{C}$		± 275		± 275	mA
			$T_A = -55 \text{ to} +125^\circ\text{C}$		± 350		± 350	

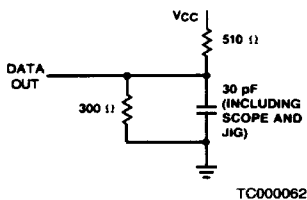
- Notes: 1. Test conditions assume signal transition times of 10 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V and output loading of the specified I_{OL}/I_{OH} and 30 pF load capacitance. Output timing reference is 1.5 V.
 2. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
 3. A pullup resistor to V_{CC} on the $\overline{CS}$ input is required to keep the device deselected during V_{CC} power up. Otherwise I_{PO} will exceed values given (Am2148 only).
 4. The operating ambient temperature is defined as the "instant-ON" case temperature.
 5. Chip deselected greater than 55 ns prior to selection.
 6. Chip deselected less than 55 ns prior to selection.
 7. Transition is measured $\pm 500 \text{ mV}$ from steady state voltage with specified loading in Figure B. These parameters are sampled and not 100% tested.
 8. $\overline{WE}$ is HIGH for read cycle.
 9. Device is continuously selected, $\overline{CS} = V_{IL}$.
 10. Address valid prior to or coincident with $\overline{CS}$ transition LOW.
 11. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.
 12. This parameter is sampled and not 100% tested, but guaranteed by characterization.

SWITCHING CHARACTERISTICS over operating range unless otherwise specified (Note 1) (for APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted)

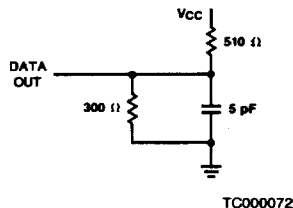
No.	Parameter Symbol	Parameter Description	Am2148/9-35		Am2148/9-45 Am21L48/9-45		Am2148/9-55 Am21L48/9-55		Am2148/9-70 Am21L48/9-70		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle											
1	t _{RC}	Address Valid to Address Do Not Care Time (Read Cycle Time)	35		45		55		70		ns
2	t _{AA}	Address Valid to Data Out Valid Delay (Address Access Time)		35		45		55		70	ns
3	t _{ACS1}	Chip Select LOW to Data Out Valid (Am2148 only)	(Note 5)	35		45		55		70	ns
4	t _{ACS2}	Chip Select LOW to Data Out Valid (Am2149 only)	(Note 6)	45		55		65		80	
5	t _{ACS}	Chip Select LOW to Data Out Valid (Am2149 only)		15		20		25		30	ns
6	t _{LZ}	Chip Select LOW to Data Out On (Notes 7 & 12)	Am2148 Am2149	10 5		10 5		10 5		10 5	ns
7	t _{HZ}	Chip Select HIGH to Data Out Off (Notes 7 & 12)		0	20	0	20	0	20	0	
8	t _{OH}	Output hold after address change		5		5		5		5	ns
9	t _{PD}	Chip Select HIGH to Power Down Delay (Note 12)	Am2148		30		30		30		ns
10	t _{PU}	Chip Select LOW to Power Up Delay (Note 12)	Am2148	0		0		0		0	ns
Write Cycle											
11	t _{WC}	Address Valid to Address Do Not Care (Write Cycle Time)	35		45		55		70		ns
12	t _{WP}	Write Enable LOW to Write Enable HIGH (Note 2)	30		35		40		50		ns
13	t _{WR}	Write Enable HIGH to Address	5		5		5		5		ns
14	t _{WZ}	Write Enable LOW to Output in High Z (Notes 7 & 12)	0	10	0	15	0	20	0	25	ns
15	t _{DW}	Data In Valid to Write Enable HIGH	20		20		20		25		ns
16	t _{DH}	Data Hold Time	0		0		0		0		ns
17	t _{AS}	Address Valid to Write Enable LOW	0		0		0		0		ns
18	t _{CW}	Chip Select LOW to Write Enable HIGH (Note 2)	30		40		50		65		ns
19	t _{OW}	Write Enable HIGH to Output in Low Z (Notes 7 & 12)	0		0		0		0		ns
20	t _{AW}	Address Valid to End of Write	30		40		50		65		ns

Notes: See notes following DC Characteristics table.

SWITCHING TEST CIRCUITS



A. Output Load



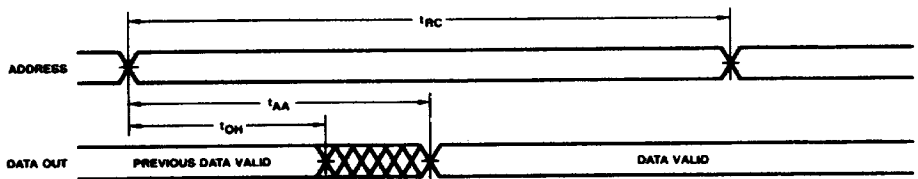
B. Output Load
for t_{HZ}, t_{LZ}, t_{OW}, t_{WZ}

SWITCHING WAVEFORMS

KEY TO SWITCHING WAVEFORMS

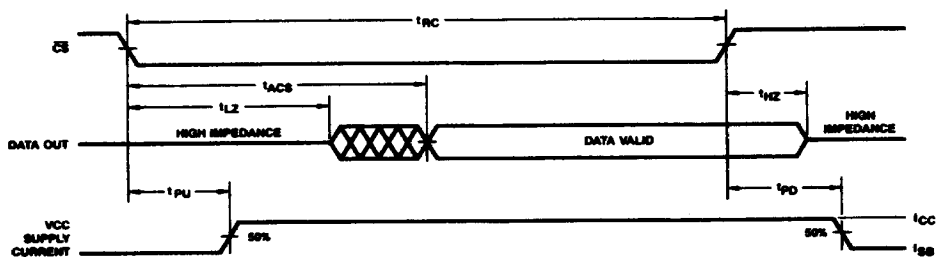
WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

KS000010



WF000461

Read Cycle No. 1 (Notes 8, 9)

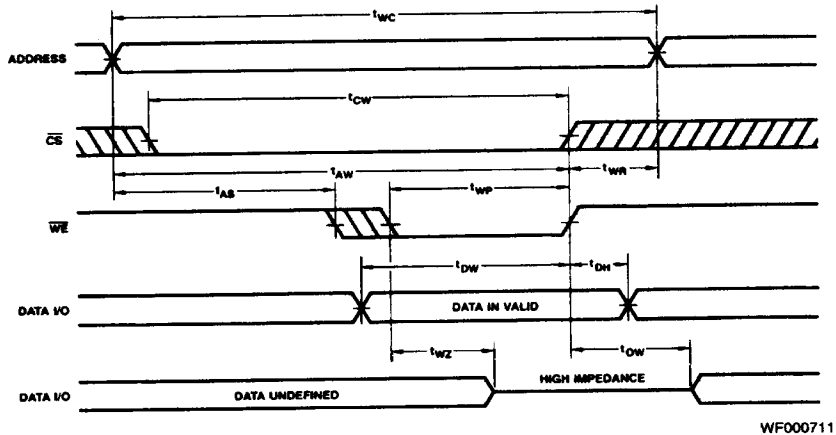


WF000241

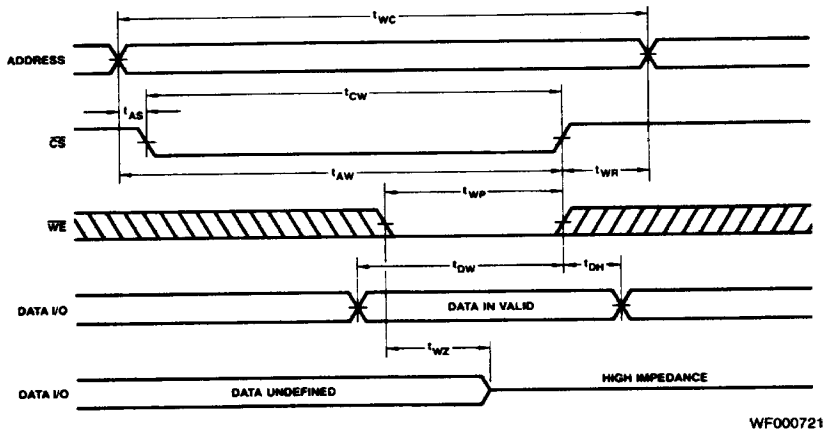
Read Cycle No. 2 (Notes 8, 10)

Notes: See notes following DC Characteristics table.

SWITCHING WAVEFORMS (Cont'd.)



Write Cycle No. 1 ($\overline{WE}$ Controlled)

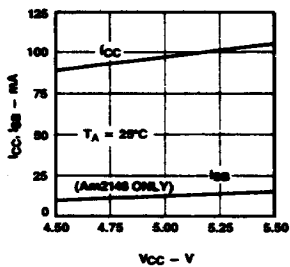


Write Cycle No. 2 ($\overline{CS}$ Controlled)

Note: If $\overline{CS}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

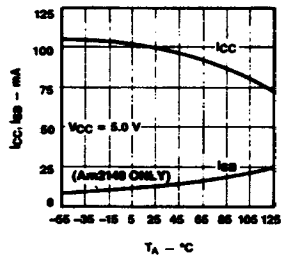
TYPICAL PERFORMANCE CURVES

Supply Current
Versus Supply Voltage



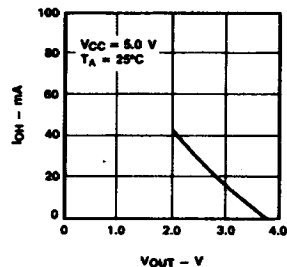
OP000730

Supply Current
Versus Ambient Temperature



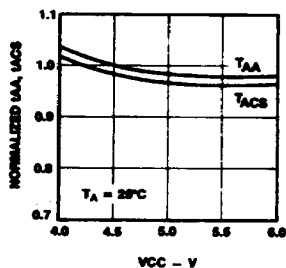
OP000741

Output Source Current
Versus Output Voltage



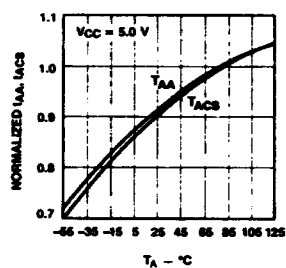
OP001081

Normalized Access Time
Versus Supply Voltage



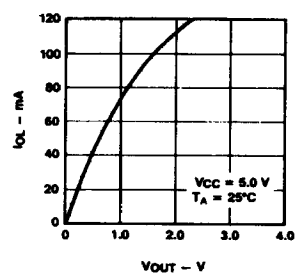
OP000761

Normalized Access Time
Versus Ambient Temperature



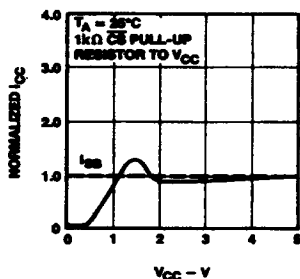
OP000771

Output Sink Current
Versus Output Voltage



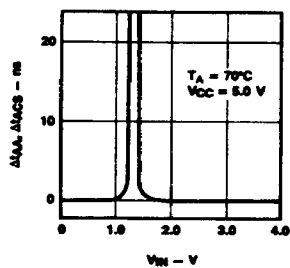
OP001091

Typical Power-On Current
Versus Power Supply



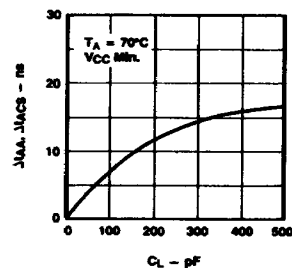
OP000781

Access Time Change
Versus Input Voltage



OP000801

Access Time Change
Versus Output Loading



OP001101