AM26LS31CC Quad Line Driver

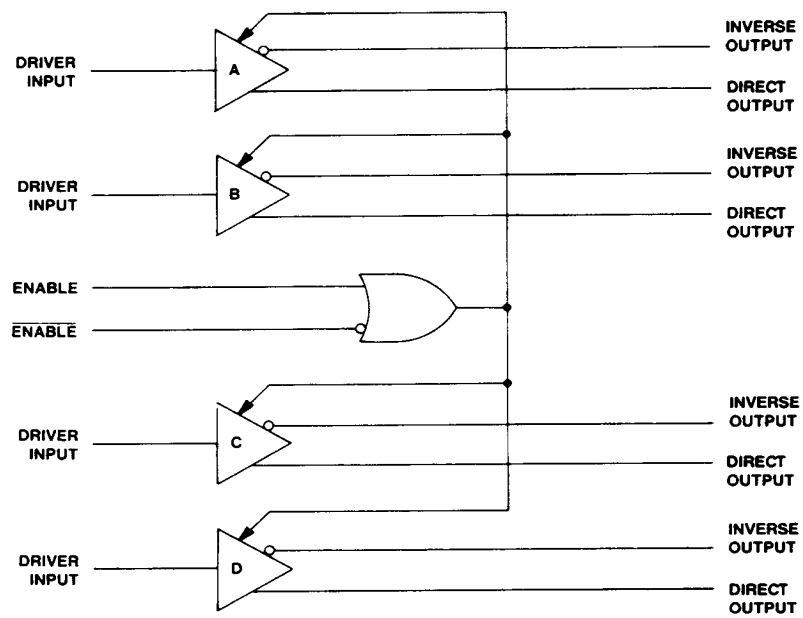
Description

The AM26LS31CC Quad Line Driver is an integrated circuit consisting of four independent line drivers with a common control for both ENABLE, $\overline{\text{ENABLE}}$. It provides high-speed differential drive to transmission lines having an impedance of at least 100 ohms. Each of the four drivers has a complementary 3-state output. The device requires only a 5 volt supply ($\pm$10%) for operation.

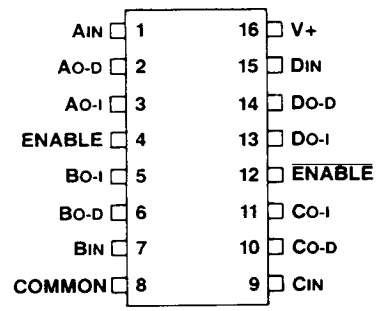
Features

- Propagation delay is less than 20 ns
- Power supply current is reduced to less than 40 mA when device is disabled
- ENABLE, $\overline{\text{ENABLE}}$ to output delay is less than 40 ns
- Direct replacement for industry-standard differential line drivers
- Meets EIA RS-422A requirements
- TTL-compatible ENABLE, $\overline{\text{ENABLE}}$ inputs
- Output skew (time delay between direct output and inverse output) is typically 2 ns
- Available in a 16-pin plastic DIP

Functional Diagram



Pin Diagram



Maximum Ratings

Rating	Value	Unit
Power Supply Voltage (V+)	7.0	V
Input Operating Voltages, V+, Driver Inputs, ENABLE, $\overline{\text{ENABLE}}$	5.5	V
Ambient Operating Temperature Range	0 to 70	°C
Storage Temperature Range	−40 to +125	°C
Driver Output Current	±35	mA
Pin Temperature (Soldering, 15 sec)	300	°C

Stresses in excess of those listed under "Maximum Ratings" may cause permanent damage to the device. This is an absolute stress rating only. Functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this data sheet is not implied. Exposure to maximum rating conditions for extended periods of time may adversely affect device reliability.

Pin Descriptions

Pin	Symbol	Name/Function
1	A_{IN}	TTL-Compatible Input, Line Driver A
2	A_{O-D}	Noninverting Line Driver Output, Driver A
3	A_{O-I}	Inverting Line Driver Output, Driver A
4	ENABLE	Logic HIGH Enable, TTL-Compatible Input (see Truth Table for logic programming of this pin)
5	B_{O-I}	Inverting Line Driver Output, Driver B
6	B_{O-D}	Noninverting Line Driver Output, Driver B
7	B_{IN}	TTL-Compatible Input, Line Driver B
8	COMMON	Circuit Common (not necessarily physical or system ground)
9	C_{IN}	TTL-Compatible Input, Line Driver C
10	C_{O-D}	Noninverting Line Driver Output, Driver C
11	C_{O-I}	Inverting Line Driver Output, Driver C
12	$\overline{\text{ENABLE}}$	Logic LOW Enable, TTL-Compatible Input (see Truth Table for logic programming of this pin)
13	D_{O-I}	Inverting Line Driver Output, Driver D
14	D_{O-D}	Noninverting Line Driver Output, Driver D
15	D_{IN}	TTL-Compatible Input, Line Driver D
16	V+	Connection for External Power Supply

Electrical Characteristics

T_A = 25°C, unless otherwise specified

Characteristic	Conditions		Min	Max	Unit
Power Supply Voltage, Operating (Figure 1)			4.5	5.5	V
Output Voltage (Figure 1)	$V+$ = 4.5 V, I_O = 20 mA, V_{IH} = 2.0 V, V_{IL} = 0.8 V	High	2.5	3.5	V
		Low	0.05	0.5	V
Input Clamp Voltage (Figure 2)	$V+$ = 4.5 V, I_{IN} = −18 mA		0	−1.5	V
Power Supply Current, No Load (Figure 3)	$V+$ = 5.5 V, V_{IN} = 0		45	90	mA
Power Supply Current, Disabled (Figure 3)	$V+$ = 5.5 V, V_{IN} = 2.0 V		20	40	mA
Output Current, Disabled (Figure 4)	V_O = 0.5 V or 2.5 V		—	±20	μA
Output Current, Power Off (Figure 5)	V_O = −0.25 or +6.0 V		—	±100	μA
Output Current, Short Circuit (Figure 6)	$V+$ = 5.5 V		—	−150	mA
Input Current, Low (Figure 7)	V_{IN} = 0.4 V		0	−0.36	mA
Input Current, High (Figure 7)	V_{IN} = 2.7 V		—	±20	μA
Input Current, Reverse (Figure 7)	V_{IN} = 7.0 V		0	0.1	mA

Timing Characteristics

Parameter	Min	Max	Unit
Transition Time; t_{THL}, t_{TLH} (Figure 10)	—	20	ns
Propogation Delay Time; t_{PHL}, t_{PLH} (Figure 9)	—	20	ns
V_{O-D} to V_{O-I} Time Difference, t_{skew} (Figure 9)	—	±6.0	ns
Overshoot, $\frac{Vpeak - V+}{V+}$ (Figure 10)	—	10	%
Output Enable Times*			
High Impedance to Output High; t_{ZH}	—	30	ns
High Impedance to Output Low; t_{ZL}	—	30	ns
Output $\overline{\text{Enable}}$ Times*			
Output High to High Impedance; t_{HZ}	—	40	ns
Output Low to High Impedance; t_{LZ}	—	40	ns

* The device is disabled when ENABLE = LOW and $\overline{\text{ENABLE}}$ = HIGH. All other conditions of ENABLE and $\overline{\text{ENABLE}}$ will allow the device to operate (see Truth Table in Applications section, page 7).

Test Circuits

Pin Allocation for Test Circuits (See Figures 1 through 8)

Driver	IN	OUT	$\overline{OUT}$
A	Pin 1	Pin 2	Pin 3
B	Pin 7	Pin 6	Pin 5
C	Pin 9	Pin 10	Pin 11
D	Pin 15	Pin 14	Pin 13

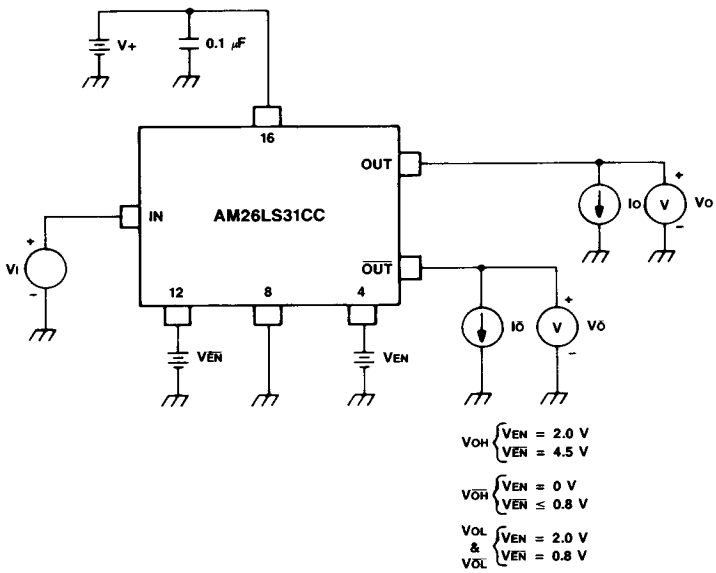


Figure 1. Output Voltages (High, Low)

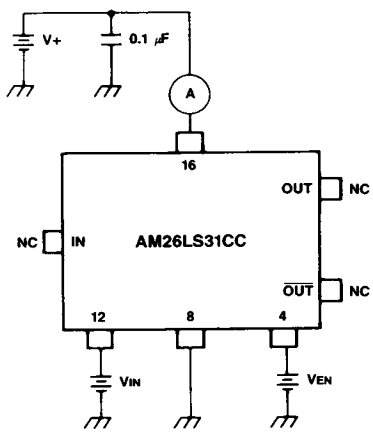


Figure 3. Power Supply Current, No Load & Disabled ($V_{EN} \leq 0.8$ V)

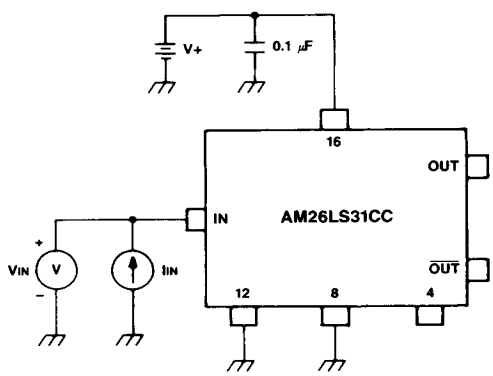


Figure 2. Input Clamp Voltage

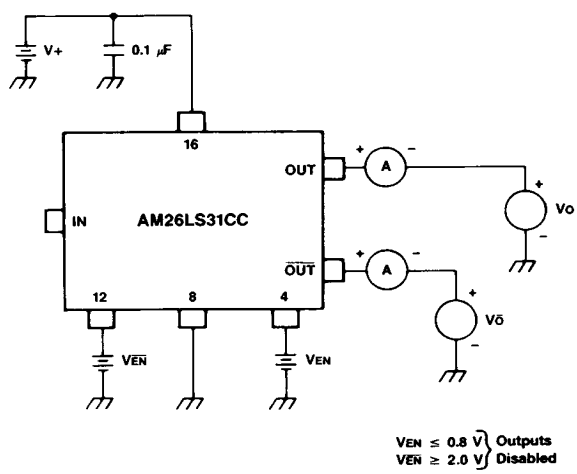


Figure 4. Output Current (Disabled)

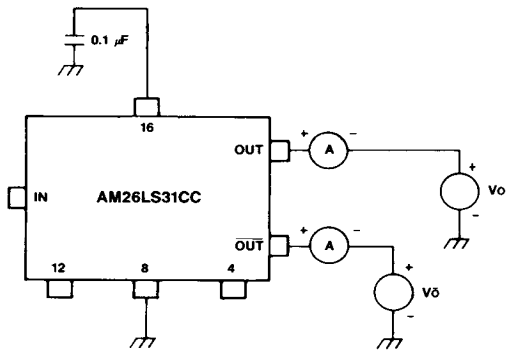


Figure 5. Output Current (Power OFF)

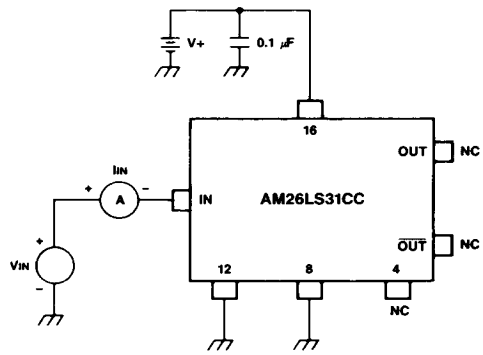


Figure 7. Input Currents (Low, High, Reverse)

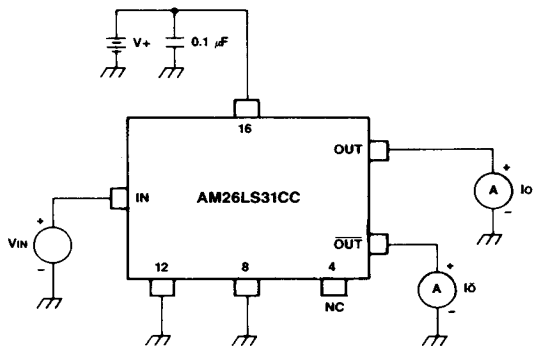


Figure 6. Output Current (Short Circuit)

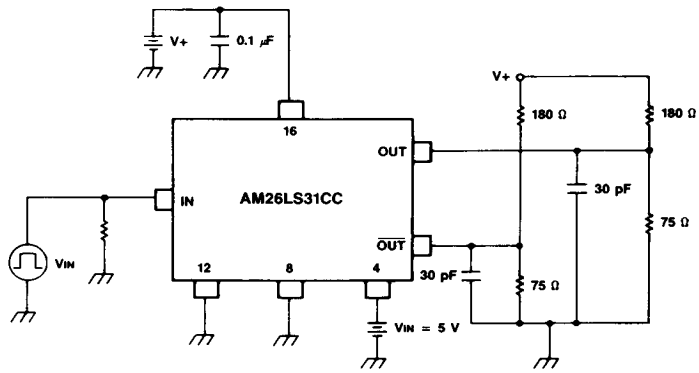
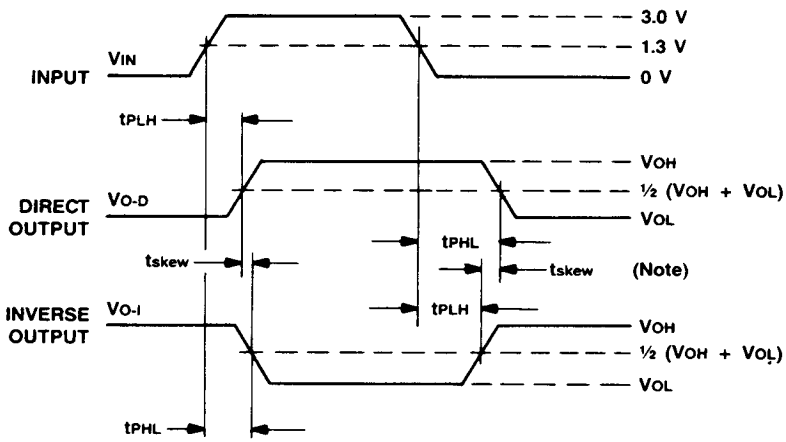
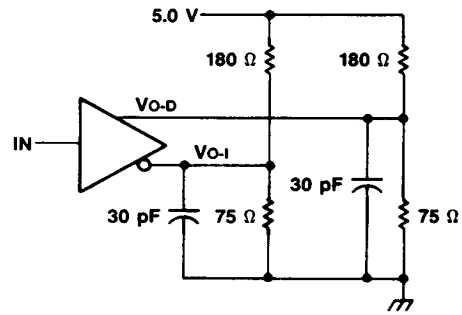


Figure 8. Switching Time

Timing Diagrams





NOTE: t_{skew} IS DEFINED AS THE ABSOLUTE TIME DIFFERENCE BETWEEN THE AVERAGE VOLTAGE OF THE INPUT AND ITS COMPLEMENT. THE AVERAGE VOLTAGE IS ½ (V_{OH} + V_{OL}). EITHER OUTPUT, V_{O-D} OR V_{O-I}, MAY OCCUR FIRST.

Figure 9. Propagation Delay and t_{SKEW} Diagram and Associated Load Schematic

Timing Diagrams
(Continued)

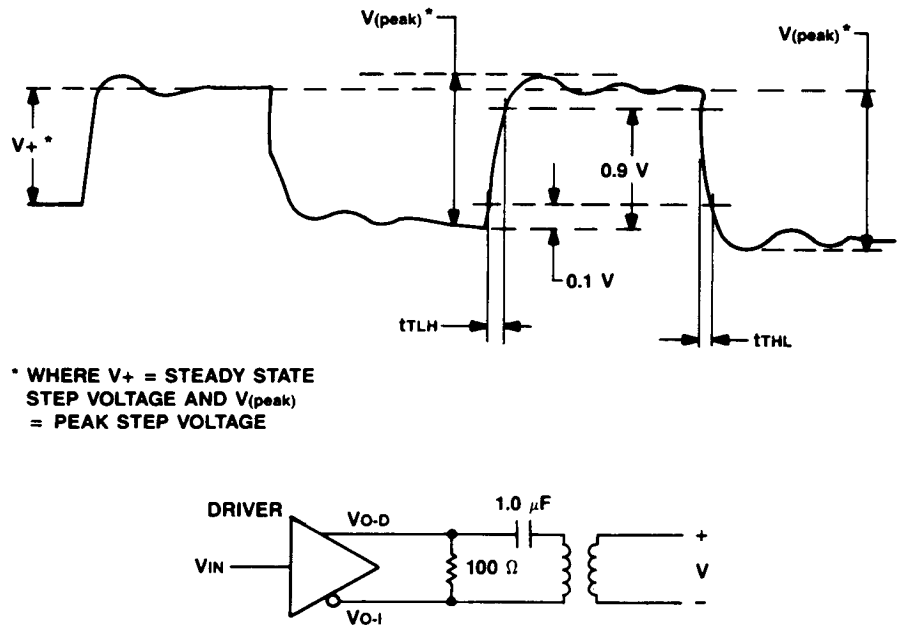


Figure 10. Overshoot Diagram and Associated Load Schematic

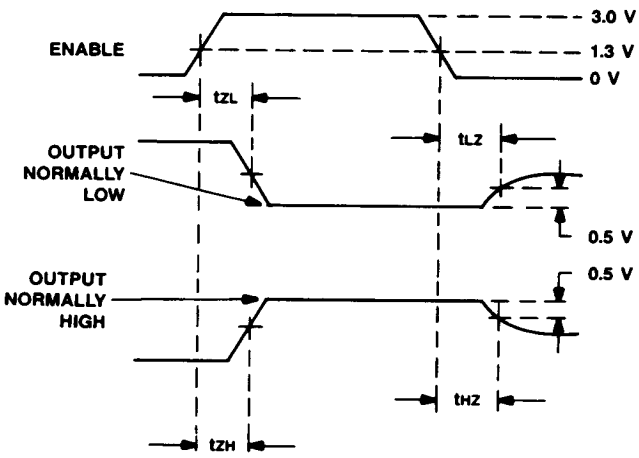


Figure 11. ENABLE and Output Waveforms

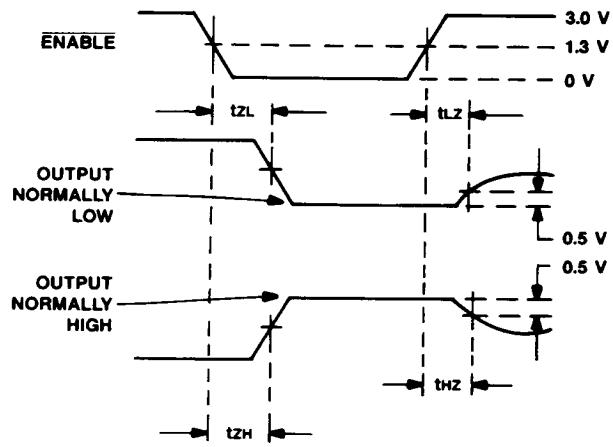


Figure 12. $\overline{\text{ENABLE}}$ and Output Waveforms

Timing Diagrams
(Continued)

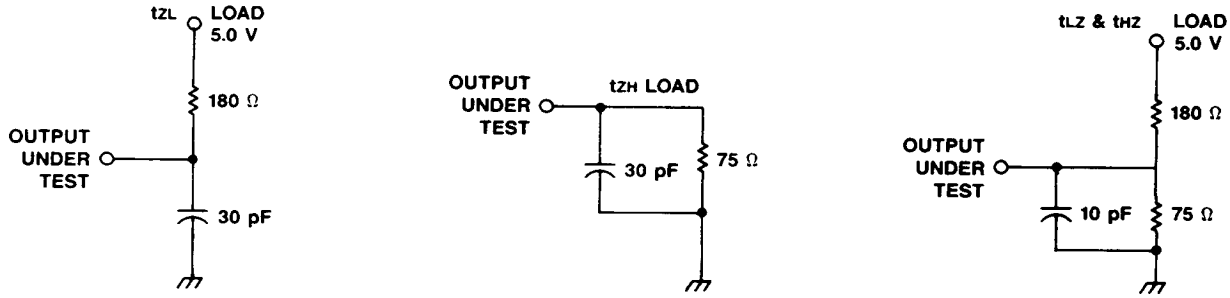


Figure 13. Associated ENABLE, $\overline{\text{ENABLE}}$ Loading Diagrams

Applications

The following Truth Table shows the V +, ENABLE, $\overline{\text{ENABLE}}$, and Data In conditions which must be met to provide specific Driver Output States (both direct and inverse outputs).

The application diagram (Figure 14) illustrates basic information for application of the AM26LS31CC Quad Line Driver device in a two-wire balanced RS-422A system.

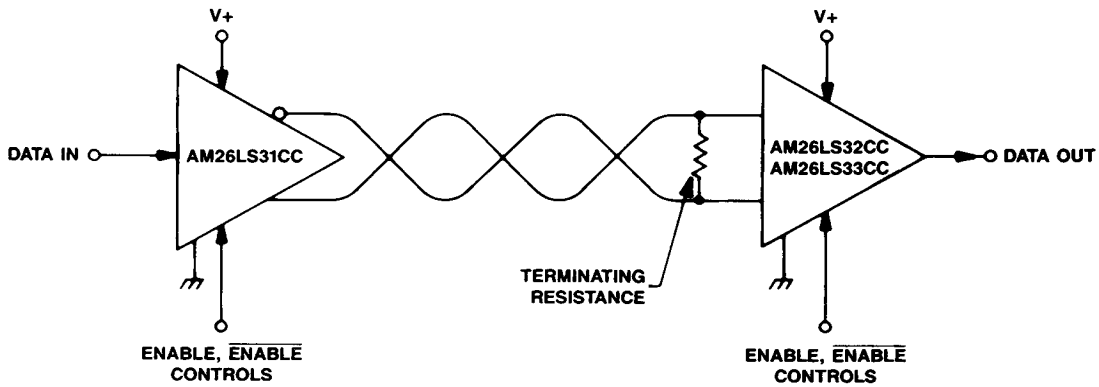


Figure 14. AM26LS31CC Quad Line Driver Application Diagram

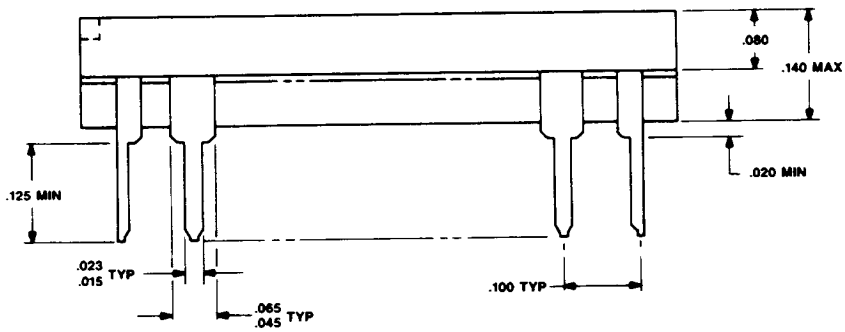
AM26LS31CC Quad Line Driver Truth Table

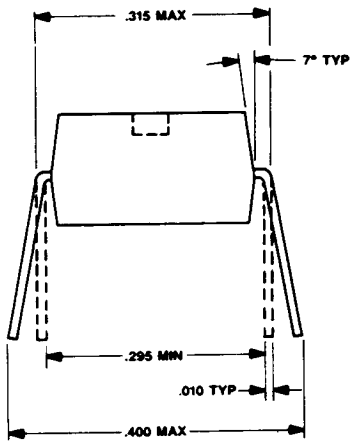
Condition*	Data In*	Direct Output	Inverse Output
ENABLE is High	High	High	Low
ENABLE is High	Low	Low	High
$\overline{\text{ENABLE}}$ is Low	High	High	Low
$\overline{\text{ENABLE}}$ is Low	Low	Low	High
ENABLE is Low $\overline{\text{ENABLE}}$ is Low	Don't Care	High Impedance	 Impedance
V + is Low (≤ 0.5 V)	Don't Care	High Impedance	High Impedance

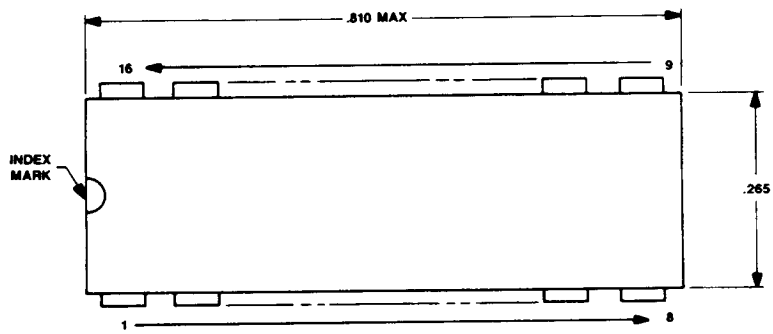
* High and Low levels for ENABLE, $\overline{\text{ENABLE}}$, and Data In are TTL levels ($V_{IH} \geq 2.0$ V, $V_{IL} \leq 0.8$ V).

Outline Drawing

(Dimensions in Inches)







Note: Pin numbers are shown for reference only

Ordering Information

DEVICE	COMCODE
AM26LS31CC	104438049

For additional information, contact your AT&T Account Manager, or call:

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