

Am26LS38

Quad Differential Backplane Transceiver

DISTINCTIVE CHARACTERISTICS

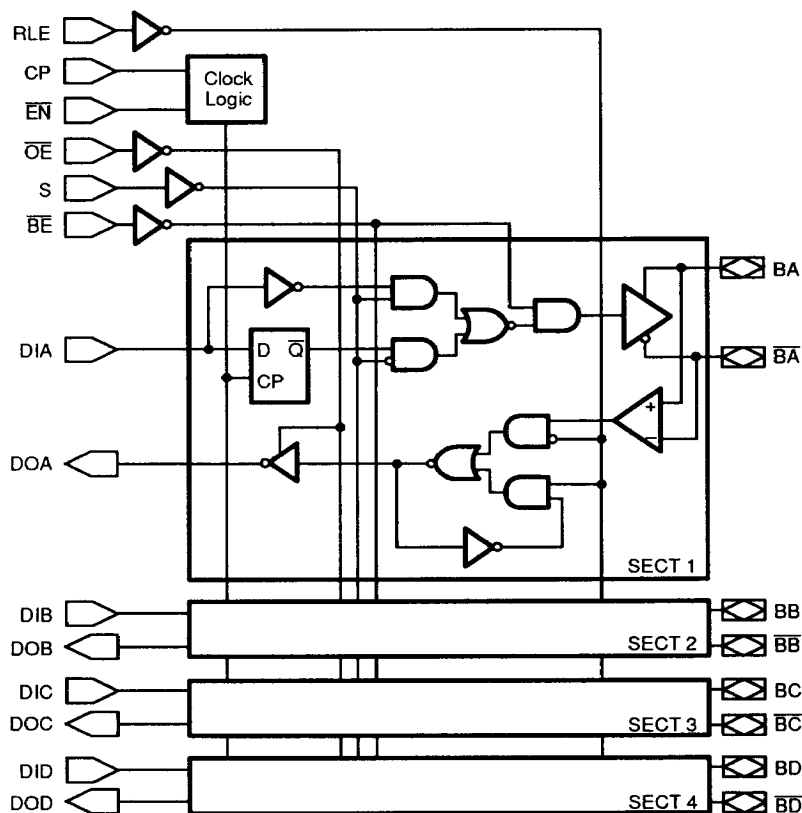
- 10 Mb data rate
- 0.45 V DC noise margin
- Biasing line terminations allow low voltage swing while maintaining high noise margin
- Pair delay 55 ns maximum
- Controlled driver skew to minimize noise
- Driver register and receiver latch with register bypass mode
- Driver output short-circuit protected to V_{CC} limits
- Outputs disabled during power-up and down
- Three-state receiver outputs maintain Hi-Z during power-up and down and over V_{CC} range

GENERAL DESCRIPTION

The Am26LS38 is a high performance backplane transceiver designed to integrate Schottky TTL performance, high noise immunity and wired logic capability into a low cost differential backplane structure. The resulting

backplane can have up to 24 receiver unit loads in a party-line, wired-OR logic configuration, with a guaranteed fail-safe state, and operates from a single 5 V power supply.

BLOCK DIAGRAM

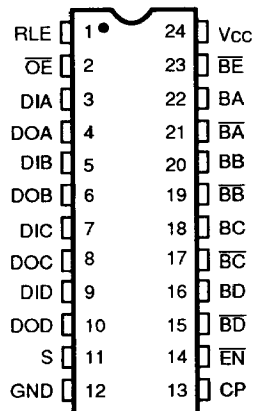


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CONNECTION DIAGRAM

Top View

DIP

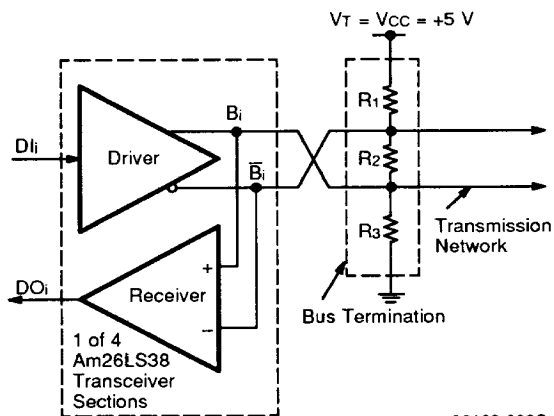


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Note:

Pin 1 is marked for orientation.

SYSTEM CONFIGURATION DIAGRAM

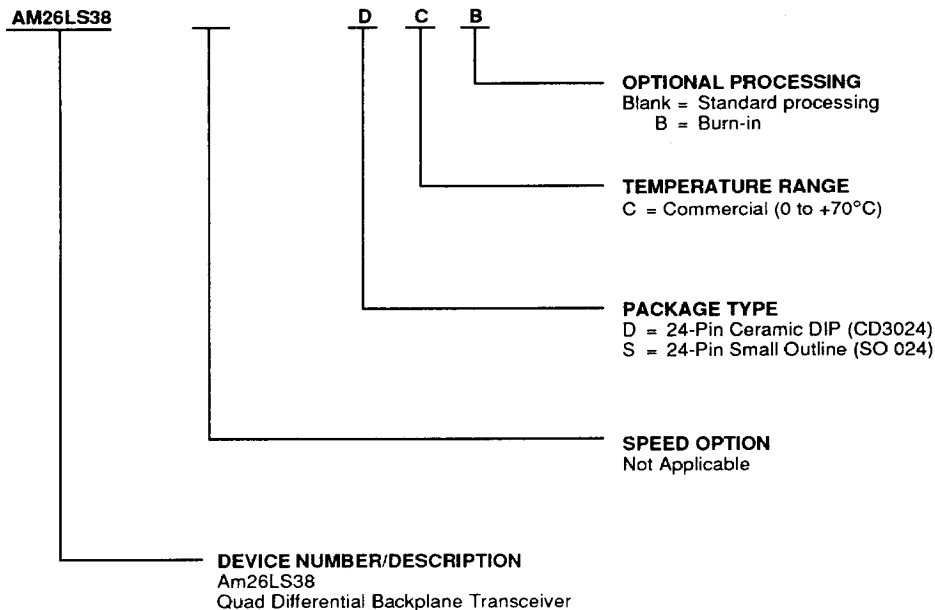


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ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
AM26LS38	DC, DCB, SC

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

PIN DESCRIPTION

Pin No.	Name	I/O	Description
22, 20 18, 16, 21, 19, 17, 15	BA, BB, BC, BD (B _i), BA, BB, BC, BD (B _i)	I/O	Paired open emitter (B _i)/ open collector (B _i) driver outputs and receiver inputs. The driver outputs are either simultaneously active or simultaneously inactive. In the inactive state (D _i = LOW) both drivers (B _i and B _i) are turned off and the voltage differential representing the OFF state is determined by the line terminating resistor networks. In the active state (D _i = HIGH), both drivers are driven on and act to reverse the voltage differential across the line to produce the ON state. The open-emitter/open-collector outputs are always connected in a wired-OR (or wired-AND) configuration. A driver is disabled by making its outputs inactive.
23	BE	I	Bus Enable operates to enable or disable all output drivers by making them inactive when BE = HIGH and controlled by data input when BE = LOW.
13	CP	I	Clock Pulse input to the driver register enters data on the LOW-to-HIGH transition.
3, 5, 7, 9	DIA, DIB, DIC, DID (D _i)	I	Data inputs each driver's buffer or register. A HIGH input to D _i will result in an active (ON) output. A LOW input will cause an inactive (OFF) output.
4, 6, 8, 10	DOA, DOB, DOC, DOD (D _O)	O	Receiver data latch outputs. An inactive bus (OFF state) will produce a LOW D _O output and an active bus (ON state) will produce a HIGH D _O output.
14	EN	I	Clock Enable for the driver registers. EN = LOW enables D _i data to be clocked into the respective register. EN = HIGH acts to hold previous data in each register regardless of the state of CP.
2	OE	I	Output Enable for the receiver latch output buffer. When OE is LOW the outputs are enabled. When OE is HIGH all receiver outputs are in the high impedance state.
1	RLE	I	Receiver Latch Enable for the receiver latches. When RLE is HIGH the latches are transparent. When RLE is LOW received data meeting the setup and hold requirements relative to the HIGH-to-LOW transition of RLE will be stored.
11	S	I	Select input control for the drivers. When S is HIGH driver data from the registers will be selected (Register Mode). When S is LOW (Buffer Mode) the drivers respond to the D _i inputs directly, bypassing the driver registers.

Inputs									Outputs			Function
RLE	CP	EN	OE	S	BE	D _i	B _i	B _i	B _i	B _i	D _O _i	
H	X	X	L	L	L	L	NA	NA	L	H	L	Driver buffer mode (loop test)
H	X	X	L	L	L	H	NA	NA	H	L	H	
H	↑	L	L	H	L	L	NA	NA	L	H	L	Driver register mode
H	↑	L	L	H	L	H	NA	NA	H	L	H	
H	X	X	L	X	H	X	L	H	NA	NA	L	Receiver latch mode
H	X	X	L	X	H	X	H	L	NA	NA	H	
L	X	X	L	X	H	X	X	X	X	X	DO _{in-1}	Receiver in circulation
X	X	X	H	X	H	X	X	X	X	X	Z	Receiver output in high impedance state

H = HIGH

L = LOW

↑ = LOW-to-HIGH transition of clock

DO_{in-1} = Previous state of D_O,

Z = High impedance

X = Don't care

NA = Not applicable

FUNCTIONAL DESCRIPTION

The Am26LS38 represents a new approach in backplane transceiver design. Its unipolar differential signaling scheme minimizes problems associated with crosstalk and the loss of noise immunity due to common mode voltage while providing high speed, party line and wired logic capabilities.

A good ground system and shielding are the best methods for limiting noise on the backplane. Ground planes can significantly reduce inductive ground voltage ringing. Where multilayer PC backplane are not a reasonable choice, a differential bus can be created using the Am26LS38 and twisted pair or any balanced transmission medium.

A backplane designed with an Am26LS38 has 3 main elements; 1) a driver section, 2) a receiver section, 3) and a controlled impedance differential line with a pre-biasing line termination. The scheme for driver, receiver, and termination resistors is shown in Figure A.

System Operation

The system has two operational states.

1. Active – driver outputs on
2. Passive – driver outputs off

This 2-state (active/passive) operation makes passive or wired logic functions possible. In the passive state, the lines assume a known polarity and voltage (pre-biased bus). The passive bus state may be assigned either the false (wired-OR) or true (wired-AND) sense, potentially reducing the number of backplane signal lines.

The 2-state driver employs active pull-down (open collector) and active pull-up (open emitter) output stages (Figure A). When a driver is active, both output stages turn on. This impresses a 0.5 V minimum voltage differential on the bus, reversing the voltage across R_2 . In the passive mode both output stages are off. The voltage levels and polarities return to the conditions set by the pre-biasing resistive network. In either state the voltage across the differential lines are symmetrical about $V_{CC}/2$. The system achieves high speeds because the

voltage levels required to change state are very close together.

The receiver is designed with a ± 50 mV threshold voltage. This low threshold level combined with a driver output greater than 500 mV provides a high degree of tolerance to attenuation and reflection effects in the cable. Receiver hysteresis provides differential noise immunity. Without hysteresis, a small amount of noise around the switching threshold could cause errors.

Propagation delay skew ($t_{PHL} - t_{PLH}$) is controlled. The system allows up to 1.5 V of common mode voltage.

Terminating the Transmission Line or Bus

Common mode reflections in the line can be reduced significantly by symmetrically terminating the bus. This increases the tolerance to common mode noise. Centering the network at $V_{CC}/2$ ($R_1 = R_3$) further improves the performance by causing all induced noise and reflections to appear as a common mode signal (Figure B).

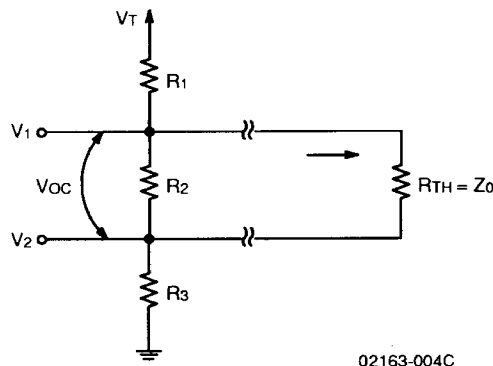
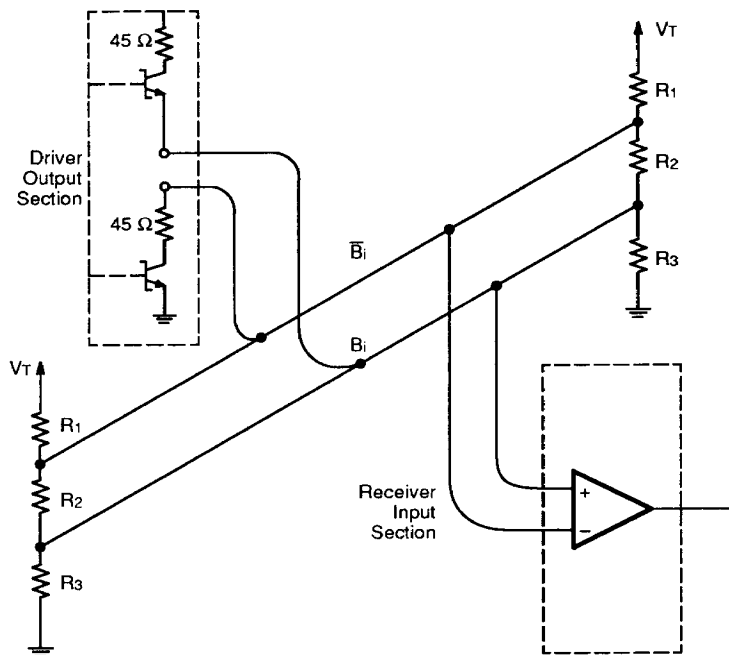


Figure B. Termination Circuit



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Figure A. The Scheme for Driver, Receiver, and Termination Resistors

A first order approximation of resistor values may be developed by letting the ratio of R_1 to R_2 be 2:1, and the Thevenin equivalent resistance of the termination equal the characteristic impedance of the line (Z_0).

Then:

$$(1) V_{OC} = V_T \frac{R_2}{R_2 + 2R_1}$$

$$(2) R_{TH} = \frac{2R_1R_2}{2R_1 + R_2}$$

From equation (1) and (2),

$$(3) R_1 = \frac{V_T R_{TH}}{2V_{OC}}$$

$$(4) R_2 = \frac{V_T R_{TH}}{V_T - V_{OC}}$$

If $V_T = 5\text{ V}$, $V_{OC} = 1.0\text{ V}$, and $R_{TH} = 90\Omega = Z_0$, we can derive that $R_1 \sim 220\Omega$, $R_2 \sim 110\Omega$.

Second order adjustments require attention to unit loading factors (receiver differential input resistance is in parallel with R_2), transmission rates and a host of other factors.

Data Path

Figure C shows the data path from one driver to another receiver for one bit of the bus interface.

The transmit register or buffer and receiver latch are configured to provide two modes of operation. The register and latch can provide local storage for output and input data. In the non-storage mode the buffer input to the driver can be selected and the receiver can be wired transparent. Incorporating storage on-chip provides improved speed and lower package count without significant penalty in the non-storage mode.

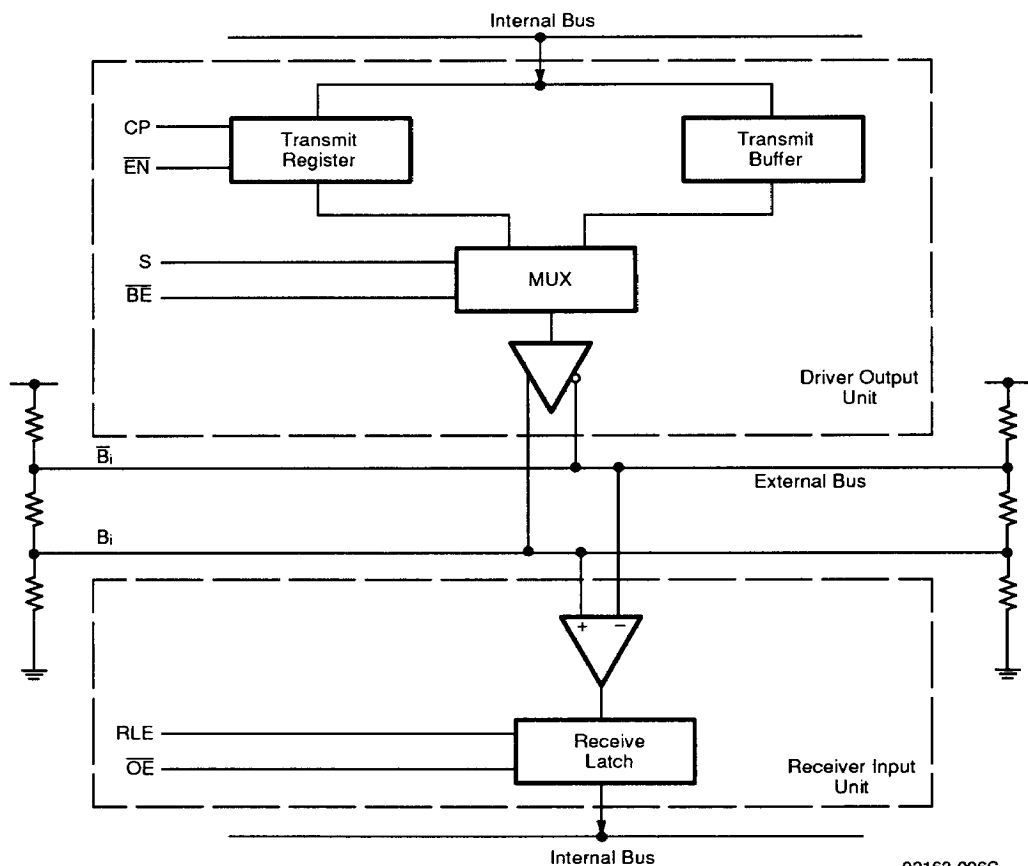
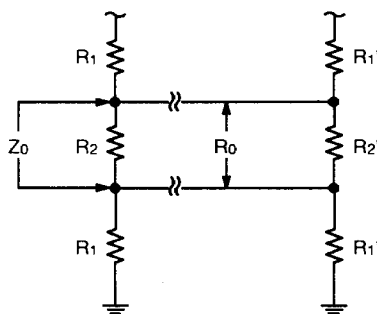


Figure C. The Data Path for One Bit of the Bus Interface

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Equivalent Circuit Recommended Termination

Termination Resistors and Equivalent Impedance

Z_0	$R_1 = R_1'$	$R_2 = R_2'$
90 Ω	220 Ω	110 Ω
120 Ω	300 Ω	150 Ω

Minimum line V_0 (differential voltage) = 0.5 V

Equivalent Termination Versus DC Resistance

Z_0	R_0
88.0 Ω	44.0 Ω
120.0 Ω	60.0 Ω

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	7.0 V
Common Mode Range	0 to V_{CC}
Differential Mode Range (REC)	0 to V_{CC}
Logic Inputs	5.5 V
Storage Temperature Range	-65 to +150°C

OPERATING RANGES**Commercial (C) Devices**

Temperature	0 to +70°C
Supply Voltage	+4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

DC CHARACTERISTICS over operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions		Min.	Typ.	Max.	Unit
Bus Driver Output							
V _O	Output Differential Voltage (Driver Active) V _{Bi} – V _{Bi}	BE = LOW DI _i = HIGH Test Circuit #1		0.5			V
I _{SS}	Output Current	DI _i = HIGH Test Circuit #2 BE = LOW	I _a	–22.5	–55	–115	mA
			I _b	+22.5	+55	+115	
I _{SC}	Output Short Circuit Current	V _{CC} = 5.5 V		–75	–150	–250	mA
Bus Receiver Input							
V _{TH}	Differential Input Threshold Voltage	V _{CM} = 0 to V _{CC} V _{OUT} = V _{OL} or V _{OH}		–50	±10	+50	mV
R _{IN}	Input Resistance to GND	0 ≤ V _{CC} ≤ V _{CC} Max.		4	5.7		kΩ
R _{IN}	Differential Input Resistance	0 ≤ V _{CC} ≤ V _{CC} Max.		8	11.4		kΩ
V _{OS}	Center Voltage	Test Circuit #3 Active and Passive		2.0	V _{CC} /2	3.0	V
V _{OS} - V _{OS}	Center Voltage Difference (Active vs Passive)	Test Circuit #3			90	300	mV
Non-Bus Input and Outputs							
V _{OH}	Output HIGH Voltage	ΔV _{IN} = +0.1 V	I _{OH} = –15 mA	2.4	3.4		V
			I _{OH} = –24 mA	2.0	3.3		
V _{OL}	Output LOW Voltage	ΔV _{IN} = –0.1 V	MIL, I _{OL} = 32 mA			0.5	V
			COM'L, I _{OL} = 48 mA			0.5	
V _{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for All Inputs		2.0			V
V _{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for All Inputs				0.8	V
I _{IL}	Input LOW Current	V _{IN} = 0.4 V	Data		–275	–400	μA
			Control		–0.65	–1.0	mA
			Clock		–0.65	–1.0	mA
I _{IH}	Input HIGH Current	V _{IN} = 2.7 V			0.1	+50	μA
I _{SC}	Output Short Circuit Current	V _{CC} = 5.5 V		–75	–150	–250	mA
I _I	Input Leakage Current	V _{IN} = 5.5 V				1	mA
V _{IC}	Input Clamp Voltage	I _{IN} = –18 mA			–0.75	–1.2	V
I _{OZ}	Leakage Current Passive	V _O = 2.4 V				+50	μA
		V _O = 0.4 V				–50	
I _{CC}	Power Supply Current	BE, OE = HIGH				145	mA





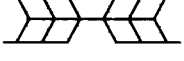
SWITCHING CHARACTERISTICS ($T_A = +25^\circ\text{C}$, $V_{CC} = 5.0\text{ V}$)

Parameter Symbol	Parameter Description		Test Conditions		Min.	Typ.	Max.	Unit
tDBA	DI to Bi/ $\overline{\text{Bi}}$ Propagation Delay	Active	$\overline{\text{BE}} = \text{LOW}$	Test Circuit #1		7	10	ns
tDBP		Passive	S = LOW			7	10	
tCBA	CP to Bi/ $\overline{\text{Bi}}$ Propagation Delay	Active	$\overline{\text{BE}} = \text{LOW}$	Test Circuit #1		10.5	16	ns
tCBP		Passive	S = HIGH			13	16	
tPA	$\overline{\text{BE}}$ to Bi/ $\overline{\text{Bi}}$ Propagation Delay	Active	DI = HIGH	Test Circuit #1		8.5	12	ns
tPP		Passive	S = LOW			4	8	
ts	DI to Clock Setup Time		$\overline{\text{BE}} = \text{LOW}$		5	2.5		ns
tH	DI to Clock Hold Time				2	0		
ts	$\overline{\text{EN}}$ to Clock Setup Time				8	4		
tH	$\overline{\text{EN}}$ to Clock Hold Time				0	−4		
ts	Bi/ $\overline{\text{Bi}}$ to RLE Setup Time				5	2.5		
tH	Bi/ $\overline{\text{Bi}}$ to RLE Hold Time				2	0.7		
tPLZ/tPHZ	$\overline{\text{OE}}$ to DO _i Disable Time		CL = 50 pF	Test Circuit #4			20	ns
tPLZ/tPHZ			CL = 5 pF	Test Circuit #4			13	
tPZL	$\overline{\text{OE}}$ to DO _i Disable Time		Test Circuit #4				17	ns
tPZH							17	
tPLH	RLE to DO _i		$\overline{\text{OE}} = \text{LOW}$	Test Circuit #4		11	13	ns
tPHL						14	17	
tPRX	Bi/ $\overline{\text{Bi}}$ to DO _i		RLE = HIGH $\overline{\text{OE}} = \text{LOW}$	Test Circuit #4		12	17	ns
tPLH	$\overline{\text{BE}}$ to DO _i Propagation Delay		RLE = HIGH $\overline{\text{OE}} = \text{LOW}$	Test Circuits #1, #4		15	25	ns
tPHL								
tPLH	DI to DO _i (Buffer Mode)		S = LOW RLE = HIGH $\overline{\text{OE}} = \text{LOW}$	Test Circuits #1, #4		18	25	ns
tPHL								
tPLH	CP to DO _i (Register Mode)		S = HIGH RLE = HIGH $\overline{\text{OE}} = \text{LOW}$	Test Circuits #1, #4		22	28	ns
tPHL								
tPWL	Clock Pulse Width	LOW			10	3		ns
tPWH		HIGH			10	5		
tPWH	RLE Pulse Width	HIGH			10	6		ns
tsKEW	Propagation Delay Skew (tPLH − tPHL)		VCC = 5 V CL = 50 pF Measurement VCC/2			±1	±5	ns

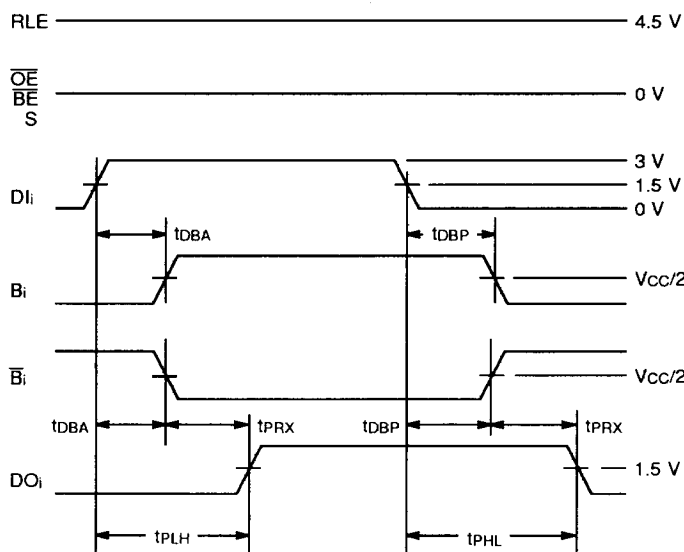
SWITCHING CHARACTERISTICS over operating range unless otherwise specified

Parameter Symbol	Parameter Description		Test Conditions	T _A = 0 to +70°C V _{CC} = 5.0 V ±10%		Unit
				Min.	Max.	
t _{DBA}	D _I to B/ _I \overline{B}_i Propagation Delay	Active	$\overline{B}\overline{E}$ = LOW Test Circuit #1		12	ns
t _{DBP}		Passive	S = LOW		12	
t _{CBA}	CP to B/ _I \overline{B}_i Propagation Delay	Active	$\overline{B}\overline{E}$ = LOW Test Circuit #1		20	ns
t _{CBP}		Passive	S = HIGH		20	
t _{PA}	$\overline{B}\overline{E}$ to B/ _I \overline{B}_i Propagation Delay	Active	D _I = HIGH Test Circuit #1		17	ns
t _{PP}		Passive	S = LOW		12	
t _S	D _I to Clock Setup Time		$\overline{B}\overline{E}$ = LOW	7		ns
t _H	D _I to Clock Hold Time			3		
t _S	\overline{EN} to Clock Setup Time			10		
t _H	\overline{EN} to Clock Hold Time			0		
t _S	B/ _I \overline{B}_i to RLE Setup Time			7		
t _H	B/ _I \overline{B}_i to RLE Hold Time			3		
t _{PLZ} /t _{PHZ}	\overline{OE} to D _{O_i} Disable Time		C _L = 50 pF Test Circuit #4		17	ns
t _{PLZ} /t _{PHZ}			C _L = 5 pF Test Circuit #4		10	
t _{PZL}	\overline{OE} to D _{O_i} Enable Time		Test Circuit #4		15	ns
t _{PZH}					15	
t _{PLH}	RLE to D _{O_i}		\overline{OE} = LOW Test Circuit #4		15	ns
t _{PHL}					20	
t _{PRX}	B/ _I \overline{B}_i to D _{O_i}		RLE = HIGH \overline{OE} = LOW Test Circuit #4		21	ns
t _{PLH}	$\overline{B}\overline{E}$ to D _{O_i} Propagation Delay		RLE = HIGH Test Circuits #1, #4		32	ns
t _{PHL}	Delay		\overline{OE} = LOW			
t _{PLH}	D _I to D _{O_i} (Buffer Mode)		S = LOW Test Circuits #1, #4		30	ns
t _{PHL}			RLE = HIGH \overline{OE} = LOW			
t _{PLH}	CP to D _{O_i} (Register Mode)		S = HIGH Test Circuits #1, #4		35	ns
t _{PHL}			RLE = HIGH \overline{OE} = LOW			
t _{PWL}	Clock Pulse Width	LOW		10		ns
t _{PWH}		HIGH		10		
t _{PWH}	RLE Pulse Width	HIGH		13		ns
t _{SKW}	Propagation Delay Skew (t _{PLH} – t _{PHL})		V _{CC} = 5 V Test Circuit #1 C _L = 50 pF Measurement V _{CC} /2		±7	ns

KEY TO SWITCHING WAVEFORMS

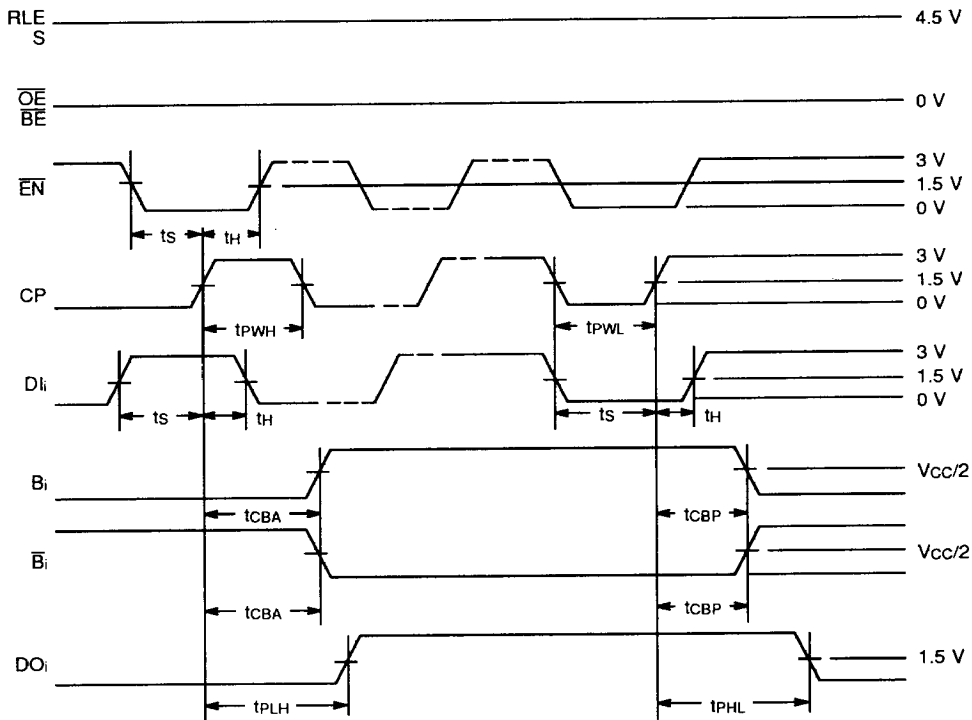
WAVEFORM	INPUTS	OUTPUTS
	Must Be Steady	Will Be Steady
	May Change from H to L	Will Be Changing from H to L
	May Change from L to H	Will Be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High Impedance "Off" State

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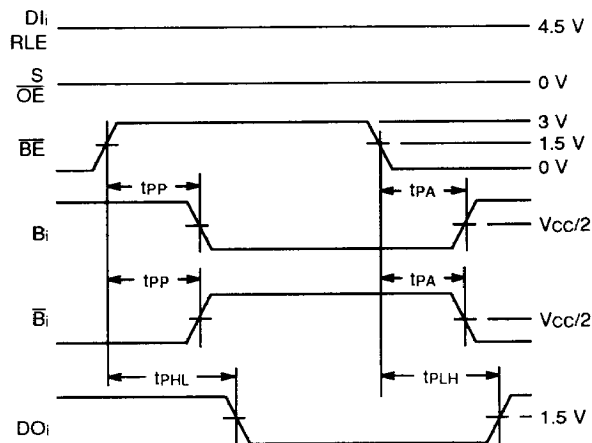
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Di to Bi, Bi-bar, DOi (Buffer Mode)



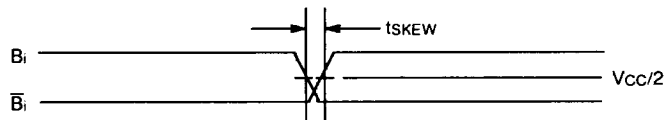
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CP to B_i , \bar{B}_i , DO_i (Register Mode)



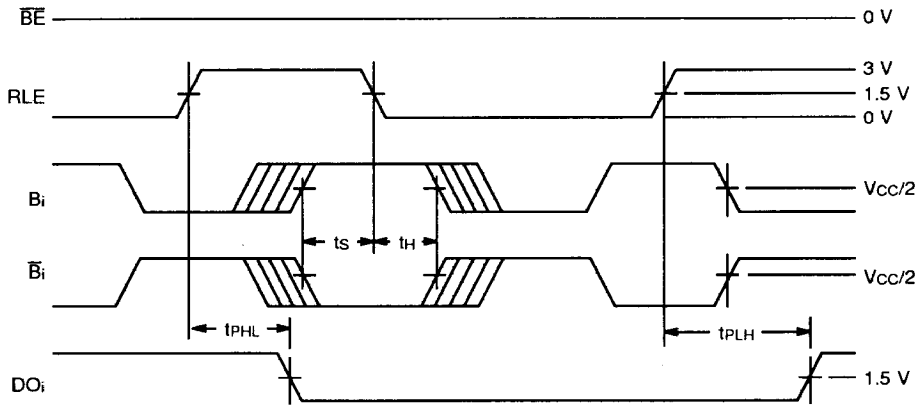
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$\bar{B}E$ to B_i , \bar{B}_i , DO_i (Passive and Active)



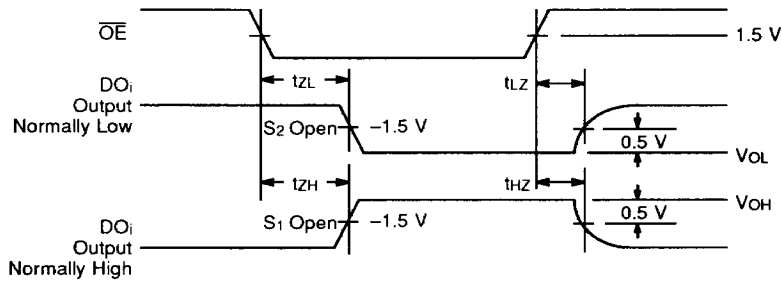
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Output to Output



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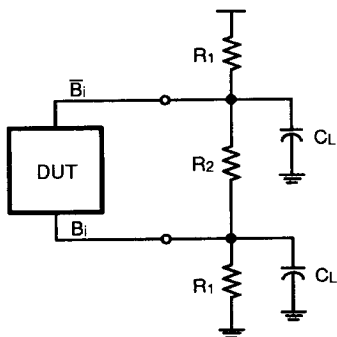
RLE to DO_i



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$\bar{O}E$ to DO_i

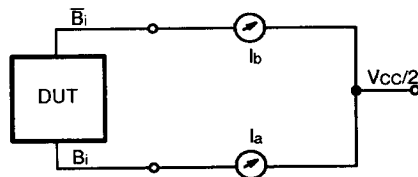
SWITCHING TEST CIRCUITS



$R_1 = 200\Omega$
 $R_2 = 50\Omega$
 $C_L = 50\text{pF}$

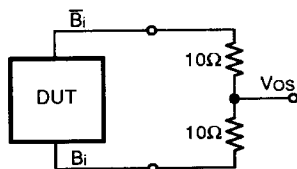
Test Circuit #1

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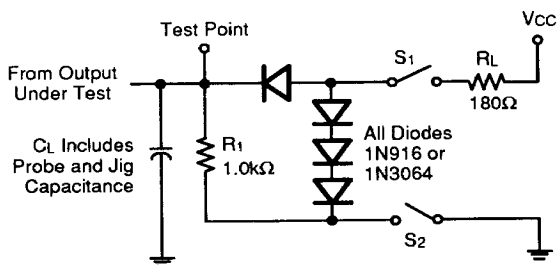
Test Circuit #2

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Test Circuit #3

02163-016C



Test Circuit #4

02163-017C

Notes:

1. $C_L = 50\text{ pF}$ unless otherwise specified.
2. S_1 and S_2 are closed except where shown.