Am27512

65,536 x 8-Bit UV Erasable PROM

PRELIMINARY

DISTINCTIVE CHARACTERISTICS

- Fast access time — as low as 250ns
- Programming voltage: 12.5V
- low Power consumption
  - Active: 525mW
  - Standby: 132mW
- Single 5V power supply
- ±10% V_{CC} supply tolerance available
- Fully static operation – no clocks
- Separate chip enable and output enable controls
- TTL compatible inputs/outputs
- 28-pin JEDEC approved Am27512 pin-out
- Pin compatible to Am2764, Am27256, Am27128 EPROMS and Am92256 – 256K ROM
- Fast programming time
- Auto select mode for automated programming

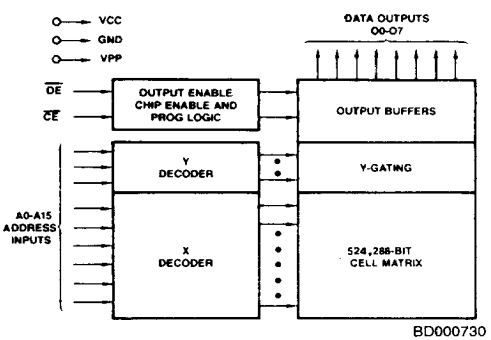
GENERAL DESCRIPTION

The Am27512 is a 524,288 bit UV-light erasable and electrically programmable read-only memory. It is organized as 65,536 words by 8-bits per word. The standard Am27512 offers a fast 250ns access time allowing operation with high-speed microprocessors without any WAIT state.

To eliminate bus contention in a multi-bus microprocessor system, the Am27512 offers separate Output Enable ($\overline{OE}$) and Chip Enable ($\overline{CE}$) controls.

All signals are TTL levels, including programming signals. Bit locations may be programmed singly, in blocks or at random. To reduce programming time, the Am27512 may be programmed using 1ms pulses. The Am27512 can be programmed in as little as six minutes.

BLOCK DIAGRAM



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MODE SELECT TABLE

Inputs			Output	Mode
$\overline{CE}/\overline{PGM}$	$\overline{OE}/V_{PP}$	A_9		
L	L	X	D_{OUT}	Read
L	H	X	HIGH Z	Output Disable
H	X	X	HIGH Z	Standby
L	V_{PP}	X	D_{IN}	Program
L	L	X	D_{OUT}	Program Verify
H	V_{PP}	X	HIGH Z	Program Inhibit
L	L	H	CODE	Auto Select

PRODUCT SELECTOR GUIDE

P/L P/L P/L P/L P/L

Part Number	Am27512	Am27512-25	Am27512-3	Am27512-30	Am27512-45
Supply Voltage	5V±5%	5V±10%	5V±5%	5V±10%	5V±10%
Access Time	250ns		300ns		450ns
Chip Enable Delay	250ns		300ns		450ns
Output Enable Delay	100ns		120ns		150ns

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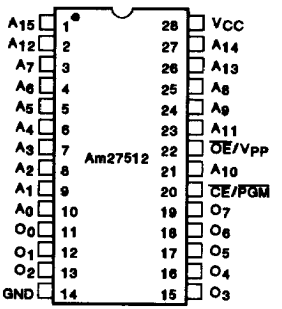
CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation

$A_0 - A_{15}$: Address
$O_0 - O_7$: Outputs
$\overline{OE}/V_{PP}$: Output Enable/V_{PP}
$\overline{CE}/\overline{PGM}$: Chip Enable/Program

ORDERING INFORMATION

Am27512-25 D C

- Temperature
  - C – Commercial (0°C to +70°C)
  - I – Industrial (–40°C to +85°C)
  - L – Extended (–55°C to +100°C)
  - M – Military (–55°C to +125°C)
- Package
  - D – 28-pin CERDIP
- Speed Select
  - No code, Am27512-25 } 250ns
  - Am27512-3, Am27512-30 } 300ns
  - Am27512-45 450ns
- Device Type
  - 8-bit UV erasable PROM

Valid Combinations	
Am27512-3 Am27512-30	DC, DI, DL
No Code Am27512-25 Am27512-45	DC, DI, DL, DM

ERASING THE Am27512

In order to clear all locations of their programmed contents, it is necessary to expose the Am27512 to an ultraviolet light source. A dosage of 15 Wseconds/cm^2 is required to completely erase an Am27512. This dosage can be obtained by exposure to an ultraviolet lamp [(wavelength of 2537 Angstroms (Å)] with intensity of 12000μW/cm^2 for 15 to 20 minutes. The Am27512 should be about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the Am27512, and similar devices, will erase with light sources having wavelengths shorter than 4000 Angstroms. Although erasure times will be much longer than with UV sources at 2537Å, nevertheless the exposure to fluorescent light and sunlight will eventually erase the Am27512 and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package window should be covered by an opaque label or substance.

PROGRAMMING THE Am27512

Upon delivery, or after each erasure, the Am27512 has all 65,536 bytes in the "1," or high state. "0"s are loaded into the Am27512 through the procedure of programming.

The programming mode is entered when 12.5V is applied to the $\overline{OE}/V_{PP}$ pin, and $\overline{CE}/\overline{PGM}$ is at TTL-low. The data to be programmed is applied 8 bits in parallel to the data output pins.

The flow chart on Page 6 shows the Interactive Programming Algorithm. Interactive algorithms reduce programming time by using short (1ms) program pulses and giving each address only as many pulses as necessary in order to reliably program the data. After each pulse is applied to a given address, the data in that address is verified. If the data does not verify, an additional pulse is applied for a maximum of 25 pulses. This process is repeated while sequencing through each address of the Am27512. This part of the algorithm is done at V_{CC} = 6.0V to assure that each EPROM bit is programmed to a sufficiently high threshold voltage. After the entire memory has been programmed with the 1ms program pulse, the entire memory is given an additional "overprogram" by cycling through each address and applying an additional 2ms program pulse. After the final address is completed, the entire EPROM memory is verified at V_{CC} = 5V±5%.

AUTO SELECT MODE

The Auto Select mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ±5°C ambient temperature range that is required when programming the Am27512.

To activate this mode, the programming equipment must force 11.5 to 12.5V on address line A_{PP}(pin 24) of the Am27512. Two identifier bytes may then be sequenced from the device outputs by toggling address line A_0 (pin 10) from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during Auto Select Mode.

Byte 0 ($A_0 = V_{IL}$) represents the manufacturer code and byte 1 ($A_0 = V_{IH}$) the device identifier code. For the Am27512 these two identifier bytes are given in the table on the next page. All identifiers for manufacturer and device codes will possess odd parity, with the MSB (O_7) defined as the parity bit.

READ MODE

The Am27512 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of OE, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC} - t_{OE}$.

STANDBY MODE

The Am27512 has a standby mode which reduces the active power dissipation by 75% from 525mW to 132mW (values for 0 to +70°C). The Am27512 is placed in the standby mode by applying a TTL high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

OUTPUT OR-TIEING

To accommodate multiple memory connections, a 2 line control function is provided to allow for:

1. Low memory power dissipation
2. Assurance that output bus contention will not occur.

It is recommended that $\overline{CE}$ be decoded and used as the primary device selecting function, while $\overline{OE}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

PROGRAM INHIBIT

Programming of multiple Am27512s in parallel with different data is also easily accomplished. Except for $\overline{CE}/\overline{PGM}$, all like inputs including $\overline{OE}/V_{PP}$ of the parallel Am27512s may be common. A TTL low-level program pulse applied to an Am27512s $\overline{CE}/\overline{PGM}$ input with $\overline{OE}/V_{PP}$ at 12.5V will program that Am27512. A high-level $\overline{CE}/\overline{PGM}$ inputs inhibits the other Am27512s from being programmed.

PROGRAM VERIFY

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify must be performed with $\overline{OE}/V_{PP}$ and $\overline{CE}/\overline{PGM}$ at V_{IL}. Data should be verified t_{DV} after the falling edge of $\overline{CE}$.

SYSTEM APPLICATIONS

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of chip enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. A 0.1μF ceramic capacitor (high frequency, low inherent inductance) should be used on each device between V_{CC} and GND to minimize transient effects. In addition, to overcome the voltage droop caused by the inductive effects of the printed circuit board traces on EPROM arrays, a 4.7μF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

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ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Ambient Temperature with
Power Applied ..... −10°C to +135°C
Voltage on All Inputs and V_{CC}
with Respect to GND ..... +6.25V to −0.6V
V_{PP} Supply Voltage with Respect
to Ground During Programming ..... +13.5V to −0.6V
Voltage on Pin 24 with Respect
to Ground ..... +13.5V to −0.6V

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Temperature
Commercial ..... 0°C to +70°C
Industrial ..... −40°C to +85°C
Extended ..... −55°C to +100°C
Military ..... −55°C to +125°C

Supply Voltages
Am27512, -3, -4 ..... +4.75V to +5.25V
Am27512, -25, -30, -45 ..... +4.5V to +5.5V

Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Symbol	Parameter	Test Conditions		Min	Typ	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0V to 5.5V				10	µA
I_{LO}	Output Leakage Current	V_{OUT} = 0V to 5.5V				10	µA
I_{CC1}	V_{CC} Standby Current (Note 5)	$\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IL}	C devices			25	mA
			M devices			40	
I_{CC2}	V_{CC} Active Current (Note 5)	$\overline{OE}$ = $\overline{CE}$ = V_{IL}	C devices			100	mA
			M devices			120	
V_{IL}	Input Low Voltage			−0.1		+0.8	Volts
V_{IH}	Input High Voltage			2.0		V_{CC}+1	Volts
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA				0.45	Volts
V_{OH}	Output High Voltage	I_{OH} = −400µA		2.4			Volts
C_{IN}	Input Capacitance	V_{IN} = 0V (Note 3)			5	7	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V (Note 3)			8	12	pF
C_{IN2}	$\overline{OE}$/V_{PP} Input Capacitance	V_{IN} = 0V (Note 3)			12	20	pF
C_{IN3}	$\overline{CE}$/$\overline{PGM}$ Input Capacitance	V_{IN} = 0V (Note 3)			9	12	pF

Notes:

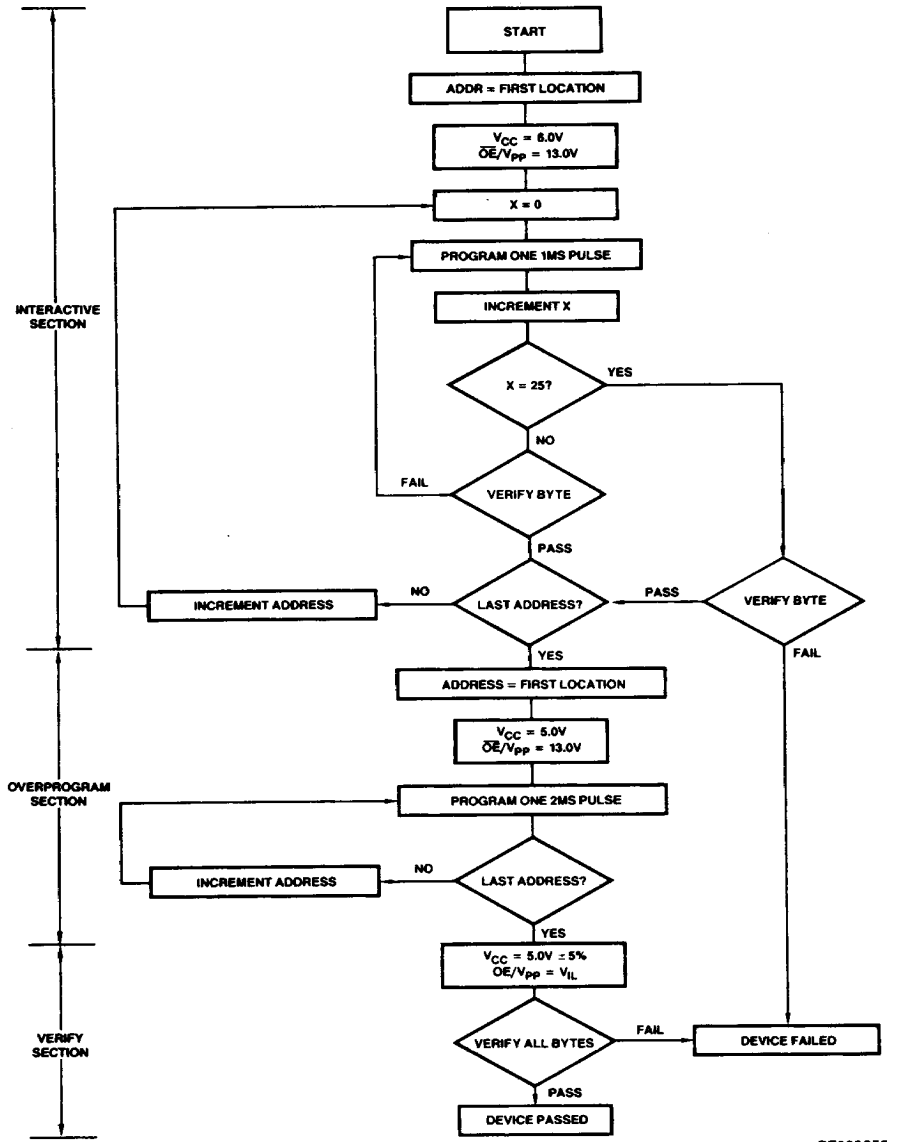
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. Typical values are for nominal supply voltages.
3. This parameter is only sampled and not 100% tested.
4. Caution: The Am27512 must not be removed from or inserted into a socket or board when Vpp or V_{PP} is applied.
5. I_{CC1} max is 40mA and I_{CC2} max is 120mA for Am27512-45.

IDENTIFIER BYTES

Identifier	A_0 (10)	O_7 (19)	O_6 (18)	O_5 (17)	O_4 (16)	O_3 (15)	O_2 (13)	O_1 (12)	O_0 (11)	Hex Data
Manufacturer Code	L	0	0	0	0	0	0	0	1	01
Device Code	H	1	0	0	0	0	1	0	1	85

Notes: 1. A_9 = 12.0V ±0.5V.
2. A_1 − A_6, A_{10} − A_{15}, $\overline{CE}$, $\overline{OE}$ = V_{IL}.
3. A_{14}=Don't Care.

INTERACTIVE PROGRAMMING FLOW CHART



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INTERACTIVE PROGRAMMING ALGORITHM DC PROGRAMMING CHARACTERISTICS

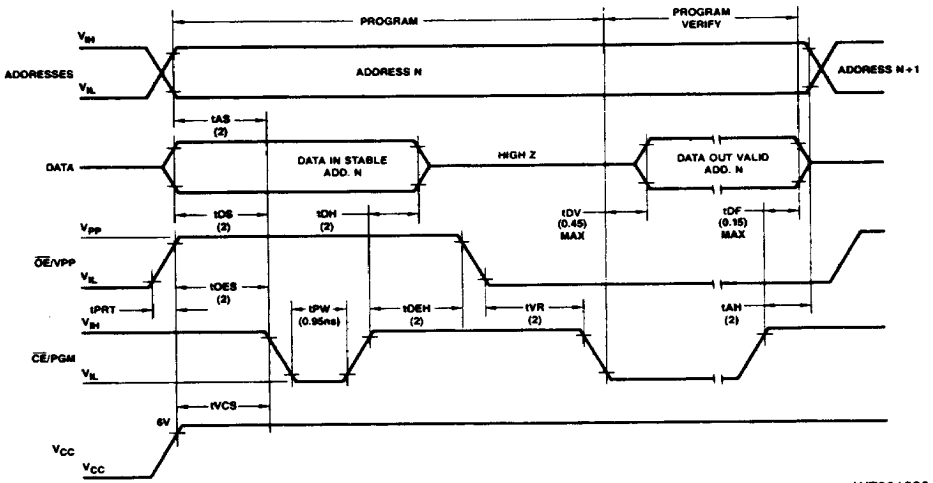
Symbol	Parameter	Test Conditions	Min	Max	Units
I_{LI}	Input Current (All Inputs)	$V_{IN} = V_{IL}$ or V_{IH}		10	μA
V_{OL}	Output Low Voltage During Verify	$I_{OL} = 2.1$ mA		0.45	Volts
V_{OH}	Output High Voltage During Verify	$I_{OH} = -400\mu A$	2.4		Volts
I_{CC}	V_{CC} Supply Current (Program and Verify)			150	mA
V_{IL}	Input Low Level (All Inputs)		-0.1	0.8	Volts
V_{IH}	Input High Level (All Inputs Except $\overline{OE}/V_{PP}$)		2.0	$V_{CC}+1$	Volts
I_{PP}	V_{PP} Supply Current (Program)	$\overline{CE} = V_{IL}$, $\overline{OE}/V_{PP} = 12.5V$		30	mA
V_{ID}	A_9 Auto Select Voltage		11.5	12.5	Volts

SWITCHING PROGRAMMING CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min	Max	Units
t_{AS}	Address Setup Time	Input tR and tF (10% to 90%) = 20ns Input Signal Levels = 0.8 to 2.2V Timing Measurement Reference Level: Inputs: 1V and 2V Outputs: 0.8V and 2V	2		μS
t_{OES}	Output Enable Setup Time		2		μS
t_{DS}	Data Setup Time		2		μS
t_{AH}	Address Hold Time		2		μS
t_{OEH}	Output Enable Hold Time		2		μS
t_{DH}	Data Hold Time		2		μS
t_{DF} (Note 2)	Chip Enable to Output Float Delay		0	150	ns
t_{DV} (Note 2)	Data Valid from $\overline{CE}$ ($\overline{CE} = V_{IL}$, $\overline{OE} = V_{IL}$)			450	ns
t_{PW}	Program Pulse Width		.95	3.15	ms
t_{PRT}	Program Pulse Rise Time		50		ns
t_{VR}	V_{PP} Recovery Time		2		μS
t_{VCS}	V_{CC} Setup Time		2		μS

Notes:
1. When programming the Am27512, a 0.1μF capacitor is required across $\overline{OE}/V_{PP}$ and ground to suppress spurious voltage transients which may damage the device.
2. This parameter is only sampled and is not 100% tested.

PROGRAM WAVEFORMS



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Notes: 1. All times shown in ( ) are minimum in μsec unless otherwise specified.
2. t_{DV} and t_{DF} are characteristics at the device but must be accommodated by the programmer.

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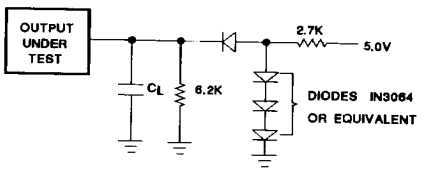
SWITCHING TEST CIRCUIT



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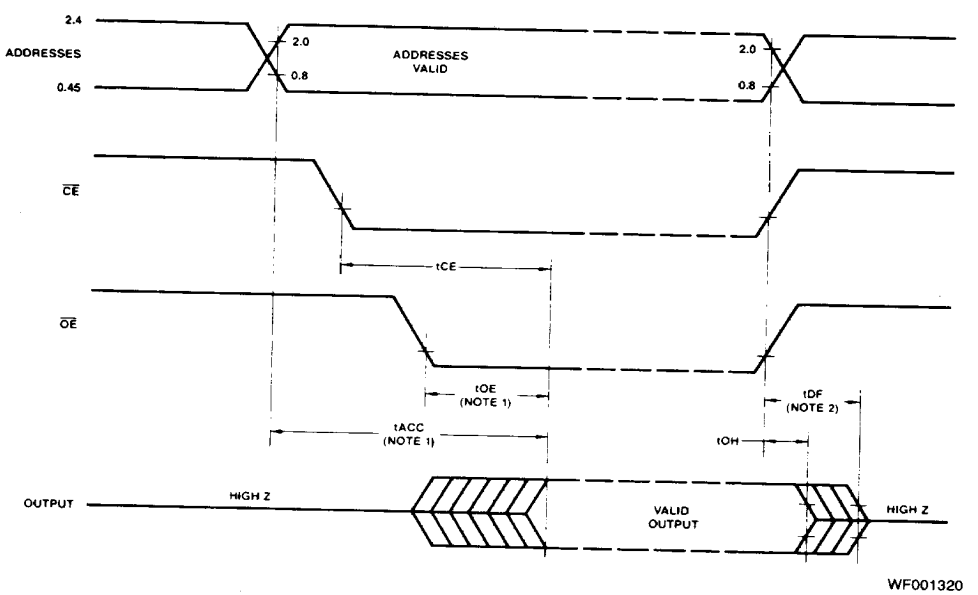
C_L = 100pF, including jig capacitance.

SWITCHING CHARACTERISTICS over operating range unless otherwise specified

No.	Symbol	Description	Test Conditions		Min Values	Maximum Values			Units
					All Types	27512-25 27512	27512-30 27512-3	27512-45	
1	t_{ACC}	Address to Output Delay	Output load: 1TTL gate and C_L = 100pF Input Rise and Fall Times ≤ 20ns Input Pulse Levels: 0.45 to 2.4V Timing Measurement Reference Level: Inputs: 1V and 2V Outputs: 0.8V and 2V	$\overline{CE} = \overline{OE} = V_{IL}$		250	300	450	ns
2	t_{CE}	Chip Enable to Output Delay		$\overline{OE} = V_{IL}$		250	300	450	ns
3	t_{OE}	Output Enable to Output Delay		$\overline{CE} = V_{IL}$		100	120	150	ns
4	t_{DF} (Note 3)	Output Enable High to Output float		$\overline{CE} = V_{IL}$	0	60	105	130	ns
5	t_{OH} (Note 3)	Output Hold from Addresses,CE orOE Whichever Occured First		$\overline{CE} = \overline{OE} = V_{IL}$	0				ns

SWITCHING WAVEFORMS



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Notes: 1. $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{OE}$ without impact on t_{ACC}.
2. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.