

# PLC16V8 Series Erasable and OTP PAL<sup>®</sup>-Type Device

Signetics Programmable Logic  
Product Specification

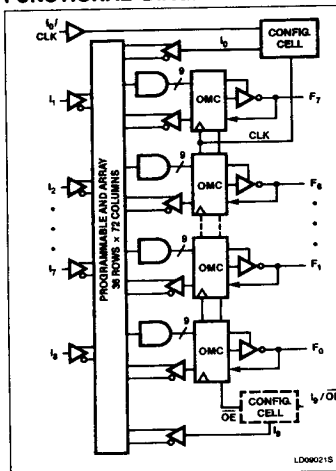
## Application Specific Products • Series 20

### DESCRIPTION

The PLC16V8 Programmable Array Logic device is a 20-pin CMOS PLD designed to replace full-power as well as quarter-power and half-power Series 20 PAL<sup>®</sup> devices. Available in four speed/power configurations, the generic PLC16V8 device can be configured to emulate 22 different PAL devices in multiple speed/power configurations. The more complex AND/OR logic functions can be easily implemented with the PLC16V8 because of the flexibility inherent to its generic Output Macro Cell architecture.

The PLC16V8 is a two-level logic element comprised of 10 inputs, 72 AND gates and 8 Output Macro Cells (OMC). Each Output Macro Cell can be individually configured as a dedicated input, a dedicated output, a bidirectional I/O or as a registered output with feedback. This generic architecture provides a means of reducing documentation, inventory and manufacturing related costs. Furthermore, the PLC16V8 series devices are designed to accept both TTL and CMOS input levels to facilitate logic integration in almost any system environment.

### FUNCTIONAL DIAGRAM



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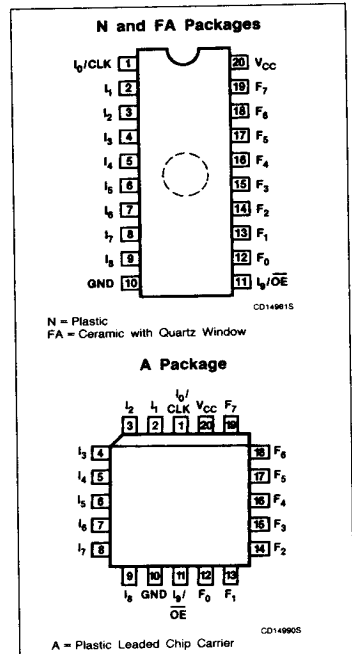
### FEATURES

- 100% functional replacement for Series 20 PAL devices
  - IOL = 24mA
- Low power performance:
  - 50 and 90mA max
  - All inputs and outputs switching at 15MHz
- Equivalent bipolar performance
  - 35 and 45ns t<sub>PD</sub>
  - 28.5 and 22.2MHz f<sub>MAX</sub> (async)
- EPROM cell technology
  - Erasable
  - 100% testable
  - Reconfigurable (quartz window package only)
- TTL and CMOS compatible
- Security fuse
- Available in 300mil-wide DIP with quartz window, plastic DIP (OTP), or PLCC (OTP)

### PIN LABEL DESCRIPTIONS

|   |                                      |
|---|--------------------------------------|
| I | Dedicated input                      |
| B | Bidirectional input/output           |
| O | Dedicated output                     |
| D | Registered output (D-type flip-flop) |

### PIN CONFIGURATIONS



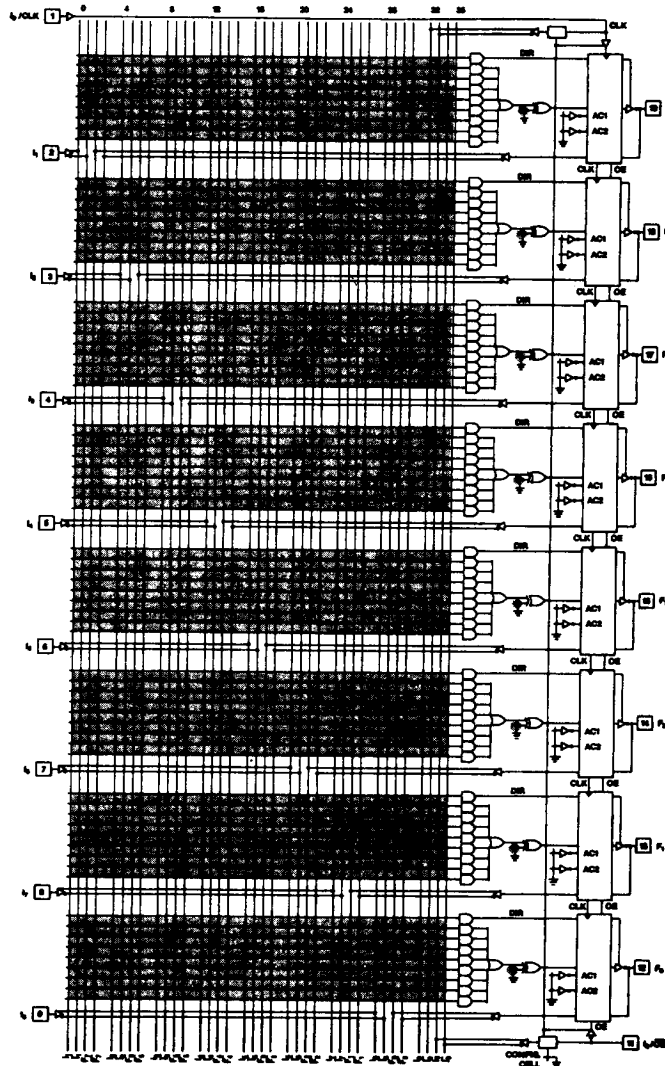
### PAL DEVICE TO PLC16V8 OUTPUT PIN CONFIGURATION CROSS REFERENCE

| PIN NO. | PLC 16V8            | 16L8 16H8 16P8 | 16R4 16RP4 | 16R6 16RP6 | 16R8 16RP8 | 16L2 16H2 16P2 | 14L4 14H4 14P4 | 12L6 12H6 12P6 | 10L8 10H8 10P8 |
|---------|---------------------|----------------|------------|------------|------------|----------------|----------------|----------------|----------------|
| 1       | I <sub>0</sub> /CLK | I              | CLK        | CLK        | CLK        | I              | I              | I              | I              |
| 19      | F <sub>7</sub>      | B              | B          | B          | D          | I              | I              | I              | O              |
| 18      | F <sub>6</sub>      | B              | B          | D          | D          | I              | I              | O              | O              |
| 17      | F <sub>5</sub>      | B              | D          | D          | D          | I              | O              | O              | O              |
| 16      | F <sub>4</sub>      | B              | D          | D          | D          | O              | O              | O              | O              |
| 15      | F <sub>3</sub>      | B              | D          | D          | D          | O              | O              | O              | O              |
| 14      | F <sub>2</sub>      | B              | D          | D          | D          | I              | O              | O              | O              |
| 13      | F <sub>1</sub>      | B              | B          | D          | D          | I              | I              | O              | O              |
| 12      | F <sub>0</sub>      | B              | B          | B          | D          | I              | I              | I              | O              |
| 11      | I <sub>9</sub> /OE  | I              | OE         | OE         | OE         | I              | I              | I              | I              |

# Erased and OTP PAL<sup>®</sup>-Type Device

PLC16V8 Series

## LOGIC DIAGRAM



### NOTES:

In the unprogrammed or virgin state:

All cells are in a conductive state.  
All AND gate locations are pulled to a logic "0" (Low).  
Output polarity is non-inverting.

Pins 1 and 11 are configured as Inputs 0 and 9, respectively, via the configuration cell. The clock and OE functions are disabled.

All output macro cells (OMC) are configured as bidirectional I/O, with the outputs disabled via the direction term.  
"1" Denotes a programmable cell location.

L0666058

June 22, 1988

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## PLC16V8 Series

Signetics' AMAZE PLD design software supports all aspects of design, simulation and programming. For simple conversion of existing PAL device codes into the PLCL16V8 series format, a PAL-to-V8 Converter is also available. This stand-alone, single-disk software package translates a PAL device code (from a device or a JEDEC standard fuse map) into an equivalent PLCL16V8 series JEDEC format. The PAL-to-V8 converter, which runs on an IBM PC or compatible, includes the necessary programmer interface software for most commercially available programmers.

The PLC16V8 has 8 individually programmable Output Macro Cells. The 72 AND inputs (or product terms) from the programmable AND array are connected to the 8 OMCs in groups of 9. Eight of the AND terms are dedicated to logic functions; the ninth is for asynchronous direction control.

### CONFIGURATION CELL

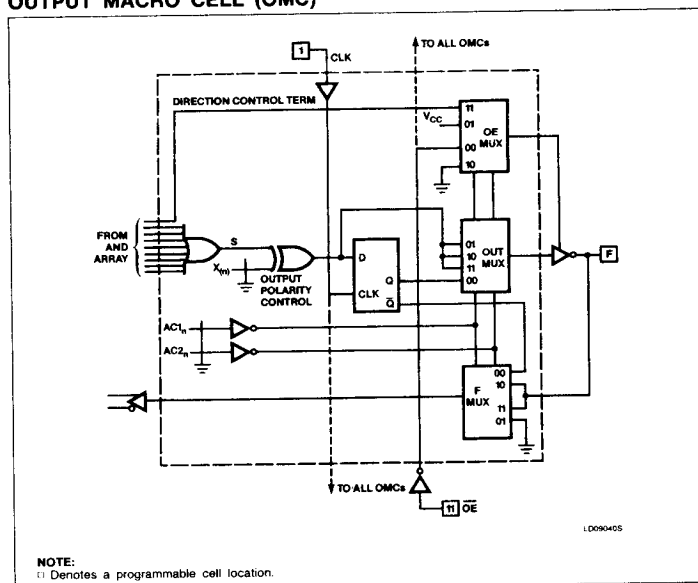
If any one OMC is configured as registered, the configuration cell will be automatically config-

| FUNCTION                            | CONTROL CELL CONFIGURATIONS |                  |              | COMMENTS                                                                                   |
|-------------------------------------|-----------------------------|------------------|--------------|--------------------------------------------------------------------------------------------|
|                                     | AC1 <sub>n</sub>            | AC2 <sub>n</sub> | CONFIG. CELL |                                                                                            |
| Registered mode                     | Programmed                  | Programmed       | Programmed   | Dedicated clock from Pin 1. OE Control for all registered OMCs from Pin 11 only.           |
| Bidirectional I/O mode <sup>1</sup> | Unprogrammed                | Unprogrammed     | Unprogrammed | Pins 1 and 11 are dedicated inputs. 3-State control from AND array only.                   |
| Fixed input mode                    | Unprogrammed                | Programmed       | Unprogrammed | Pins 1 and 11 are dedicated inputs.                                                        |
| Fixed output mode                   | Programmed                  | Unprogrammed     | Unprogrammed | Pins 1 and 11 are dedicated inputs. The feedback path (via F <sub>MUX</sub> ) is disabled. |

**NOTE:**

**NOTE:**  
1. This is the virgin state as shipped from the factory.

### OUTPUT MACRO CELL (OMC)



ured (via the design software) to ensure that the clock and output enable functions are enabled on Pins 1 and 11, respectively. If none of the OMCs are registered, the configuration cell will be programmed such that Pins 1 and

11 are dedicated inputs. The programming codes are as follow:

|                                       |   |
|---------------------------------------|---|
| Pin 1 = CLK, Pin 11 = $\overline{OE}$ | L |
| Pin 1 and Pin 11 = Input              | H |

# Erased and OTP PAL<sup>®</sup>-Type Device

## PLC16V8 Series

### ORDERING INFORMATION

| DESCRIPTION                                            |                                             |                                   | ORDER CODE           |
|--------------------------------------------------------|---------------------------------------------|-----------------------------------|----------------------|
| Propagation Delay (Max)                                |                                             | I <sub>CC</sub> (Active at 15MHz) |                      |
| t <sub>PD</sub> = 35ns                                 | f <sub>MAX</sub> = 18.1MHz<br>(Synchronous) | 50mA                              | PLC16V8Q35           |
|                                                        |                                             | 90mA                              | PLC16V8H35           |
| t <sub>PD</sub> = 45ns                                 | f <sub>MAX</sub> = 13.3MHz<br>(Synchronous) | 50mA                              | PLC16V8Q45           |
|                                                        |                                             | 90mA                              | PLC16V8H45           |
| Package Type                                           |                                             |                                   | PACKAGE <sup>1</sup> |
| 20-pin Plastic DIP (one time programmable; OTP)        |                                             |                                   | N                    |
| 20-pin Plastic Leaded Chip Carrier                     |                                             |                                   | A                    |
| 20-pin Ceramic DIP with quartz window (reprogrammable) |                                             |                                   | FA                   |

**NOTE:**

1. The package order code directly follows the device order code, i.e., PLC16V8Q35N for Plastic DIP (OTP).

### ABSOLUTE MAXIMUM RATINGS<sup>1</sup>

| SYMBOL           | PARAMETER                   | RATINGS                       | UNIT            |
|------------------|-----------------------------|-------------------------------|-----------------|
| V <sub>CC</sub>  | Supply voltage              | -0.5 to +7                    | V <sub>DC</sub> |
| V <sub>IN</sub>  | Input voltage               | -0.5 to V <sub>CC</sub> + 0.5 | V <sub>DC</sub> |
| V <sub>OUT</sub> | Output voltage              | -0.5 to V <sub>CC</sub> + 0.5 | V <sub>DC</sub> |
| I <sub>IN</sub>  | Input currents              | -10 to +10                    | mA              |
| I <sub>OUT</sub> | Output currents             | +24                           | mA              |
| T <sub>A</sub>   | Operating temperature range | 0 to +75                      | °C              |
| T <sub>STG</sub> | Storage temperature range   | -65 to +150                   | °C              |

**NOTE:**

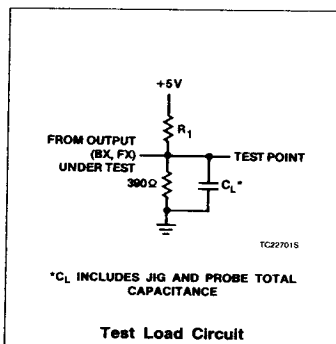
1. Stresses above those listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification of the device is not implied.

### THERMAL RATINGS

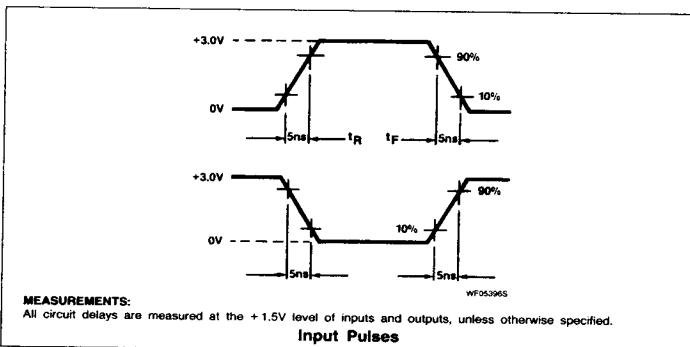
| TEMPERATURE                                   |       |
|-----------------------------------------------|-------|
| Maximum junction                              | 150°C |
| Maximum ambient                               | 75°C  |
| Allowable thermal rise<br>ambient to junction | 75°C  |

The PLC16V8 device is also processed to military requirements for operation over the military temperature range. For specifications and ordering information consult the Signetics Military Data Book.

### AC TEST CONDITIONS



### VOLTAGE WAVEFORMS



# Erasable and OTP PAL®-Type Device

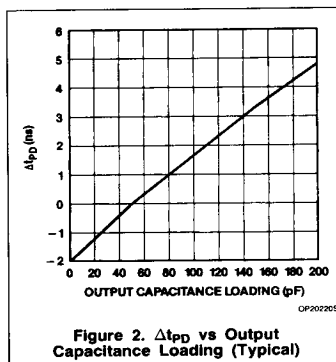
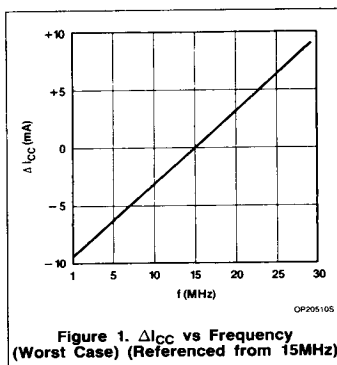
## PLC16V8 Series

### DC ELECTRICAL CHARACTERISTICS $0^{\circ}\text{C} \leq T_A \leq +75^{\circ}\text{C}$ , $4.75 \leq V_{CC} \leq 5.25\text{V}$

| SYMBOL                      | PARAMETER                                            | TEST CONDITION                                               | LIMITS            |                  |                       | UNIT |
|-----------------------------|------------------------------------------------------|--------------------------------------------------------------|-------------------|------------------|-----------------------|------|
|                             |                                                      |                                                              | Min               | Typ <sup>1</sup> | Max                   |      |
| Input voltage <sup>2</sup>  |                                                      |                                                              |                   |                  |                       |      |
| V <sub>IL</sub>             | Low                                                  | V <sub>CC</sub> = Min                                        | -0.3              |                  | 0.8                   | V    |
| V <sub>IH</sub>             | High                                                 | V <sub>CC</sub> = Max                                        | 2.0               |                  | V <sub>CC</sub> + 0.3 | V    |
| Output voltage <sup>2</sup> |                                                      |                                                              |                   |                  |                       |      |
| V <sub>OL</sub>             | Low                                                  | V <sub>CC</sub> = Min<br>I <sub>OL</sub> = 24mA              |                   |                  | 0.5                   | V    |
| V <sub>OH</sub>             | High                                                 | I <sub>OH</sub> = -3.2mA                                     | 2.4               |                  |                       | V    |
| Input current               |                                                      |                                                              |                   |                  |                       |      |
| I <sub>IL</sub>             | Low <sup>6</sup>                                     | V <sub>IN</sub> = GND                                        |                   |                  | -10                   | μA   |
| I <sub>IH</sub>             | High                                                 | V <sub>IN</sub> = V <sub>CC</sub>                            |                   |                  | 10                    | μA   |
| Output current              |                                                      |                                                              |                   |                  |                       |      |
| I <sub>O(OFF)</sub>         | Hi-Z state                                           | V <sub>OUT</sub> = V <sub>CC</sub><br>V <sub>OUT</sub> = GND |                   |                  | 10<br>-10             | μA   |
| I <sub>OS</sub>             | Short-circuit <sup>3, 7</sup>                        | V <sub>OUT</sub> = GND                                       |                   |                  | -130                  | mA   |
| I <sub>CC</sub>             | V <sub>CC</sub> supply current (Active) <sup>4</sup> | I <sub>OUT</sub> = 0mA f = 15MHz <sup>5</sup>                | Quarter power (Q) |                  | 50                    | mA   |
|                             |                                                      |                                                              | Half power (H)    |                  | 90                    | mA   |
| Capacitance                 |                                                      |                                                              |                   |                  |                       |      |
| C <sub>I</sub>              | Input                                                | V <sub>CC</sub> = 5V<br>V <sub>IN</sub> = 2.0V               |                   | 12               |                       | pF   |
| C <sub>B</sub>              | I/O                                                  | V <sub>B</sub> = 2.0V                                        |                   | 15               |                       | pF   |

#### NOTES:

1. All typical values are at  $V_{CC} = 5\text{V}$ ,  $T_A = +25^{\circ}\text{C}$ .
2. All voltage values are with respect to network ground terminal.
3. Duration of short-circuit should not exceed one second. Test one at a time.
4. Tested with TTL input levels:  $V_{IL} = 0.45\text{V}$ ,  $V_{IH} = 2.4\text{V}$ . Measured with all inputs and outputs switching.
5. Refer to Figure 1,  $\Delta I_{CC}$  vs Frequency (worst case). (Referenced from 15MHz)
6.  $I_{IL}$  for Pin 1 ( $I_Q/\text{CLK}$ ) is  $\pm 10\mu\text{A}$  with  $V_{IN} = 0.4\text{V}$ .
7. Refer to Figure 2 for  $\Delta t_{PD}$  vs output capacitance loading.



# Erasable and OTP PAL<sup>®</sup>-Type Device

## PLC16V8 Series

### AC ELECTRICAL CHARACTERISTICS $0^{\circ}\text{C} \leq T_A \leq +75^{\circ}\text{C}$ , $4.75\text{V} \leq V_{CC} \leq 5.25\text{V}$ $R_2 = 390\Omega$

| SYMBOL                                                       | PARAMETER                                                        | TO                | FROM              | TEST CONDITION <sup>1</sup>                                |                     | PLC16V8Q-35<br>PLC16V8H-35 |              | PLC16V8Q-45<br>PLC16V8H-45 |              | UNIT |
|--------------------------------------------------------------|------------------------------------------------------------------|-------------------|-------------------|------------------------------------------------------------|---------------------|----------------------------|--------------|----------------------------|--------------|------|
|                                                              |                                                                  |                   |                   | R <sub>1</sub> (Ω)                                         | C <sub>L</sub> (pF) | Min                        | Max          | Min                        | Max          |      |
| Pulse width                                                  |                                                                  |                   |                   |                                                            |                     |                            |              |                            |              |      |
| t <sub>CKP</sub>                                             | Clock period<br>(Minimum<br>t <sub>IS</sub> + t <sub>CKO</sub> ) | CLK +             | CLK +             |                                                            |                     | 55                         |              | 75                         |              | ns   |
| t <sub>CKH</sub>                                             | Clock width High                                                 | CLK -             | CLK +             |                                                            |                     | 20                         |              | 25                         |              | ns   |
| t <sub>CKL</sub>                                             | Clock width Low                                                  | CLK +             | CLK -             |                                                            |                     | 20                         |              | 25                         |              | ns   |
| Hold time                                                    |                                                                  |                   |                   |                                                            |                     |                            |              |                            |              |      |
| t <sub>IH</sub>                                              | Input or feedback<br>data hold time                              | Input ±           | CLK +             |                                                            |                     | 0                          |              | 0                          |              | ns   |
| Setup time                                                   |                                                                  |                   |                   |                                                            |                     |                            |              |                            |              |      |
| t <sub>IS</sub>                                              | Input or feedback<br>data setup time                             | CLK +             | I ±, F ±          |                                                            |                     | 30                         |              | 40                         |              | ns   |
| Propagation delay                                            |                                                                  |                   |                   |                                                            |                     |                            |              |                            |              |      |
| t <sub>PD</sub>                                              | Delay from input<br>to active output                             | F ±               | I ±, F ±          | 200                                                        | 50                  |                            | 35           |                            | 45           | ns   |
| t <sub>CKO</sub>                                             | Clock High to<br>output valid<br>access Time                     | F ±               | CLK +             | 200                                                        | 50                  |                            | 25           |                            | 35           | ns   |
| t <sub>OE1</sub> <sup>3</sup>                                | Product term<br>enable to active<br>output                       | F ±               | I ±, F ±          | Active-High R = 1.5k<br>Active-Low R = 550                 | 50                  |                            | 35           |                            | 45           | ns   |
| t <sub>OD1</sub> <sup>2</sup>                                | Product term<br>disable to outputs<br>off                        | F ±               | I ±, F ±          | From V <sub>OH</sub> R = ∞<br>From V <sub>OL</sub> R = 200 | 5                   |                            | 35           |                            | 45           | ns   |
| t <sub>OD2</sub> <sup>2</sup>                                | Pin 11 output<br>disable High to<br>outputs off                  | F ±               | OE -              | From V <sub>OH</sub> R = ∞<br>From V <sub>OL</sub> R = 200 | 5                   |                            | 25           |                            | 30           | ns   |
| t <sub>OE2</sub> <sup>3</sup>                                | Pin 11 output<br>enable to active<br>output                      | F ±               | OE +              | Active-High R = 1.5k<br>Active-Low R = 550                 | 50                  |                            | 25           |                            | 30           | ns   |
| t <sub>PPR</sub>                                             | Power-up reset                                                   | F +               | V <sub>CC</sub> + |                                                            |                     |                            | 35           |                            | 45           | ns   |
| Frequency of operation (t <sub>IS</sub> + t <sub>CKO</sub> ) |                                                                  |                   |                   |                                                            |                     |                            |              |                            |              |      |
| f <sub>MAX</sub>                                             | Maximum<br>frequency                                             | Synch.<br>Asynch. |                   | 200                                                        | 50                  |                            | 18.1<br>28.5 |                            | 13.3<br>22.2 | MHz  |

#### NOTES:

1. Refer also to AC Test Conditions. (Test Load Circuit)

2. 3-State levels are measured  $\pm 0.5\text{V}$  from the active steady-state level.

3. Resistor values of 1.5k and 550 $\Omega$  provide 3-State levels of 1.0V and 2.0V, respectively. Output timing measurements are to 1.5V level.

# Erasable and OTP PAL®-Type Device

## PLC16V8 Series

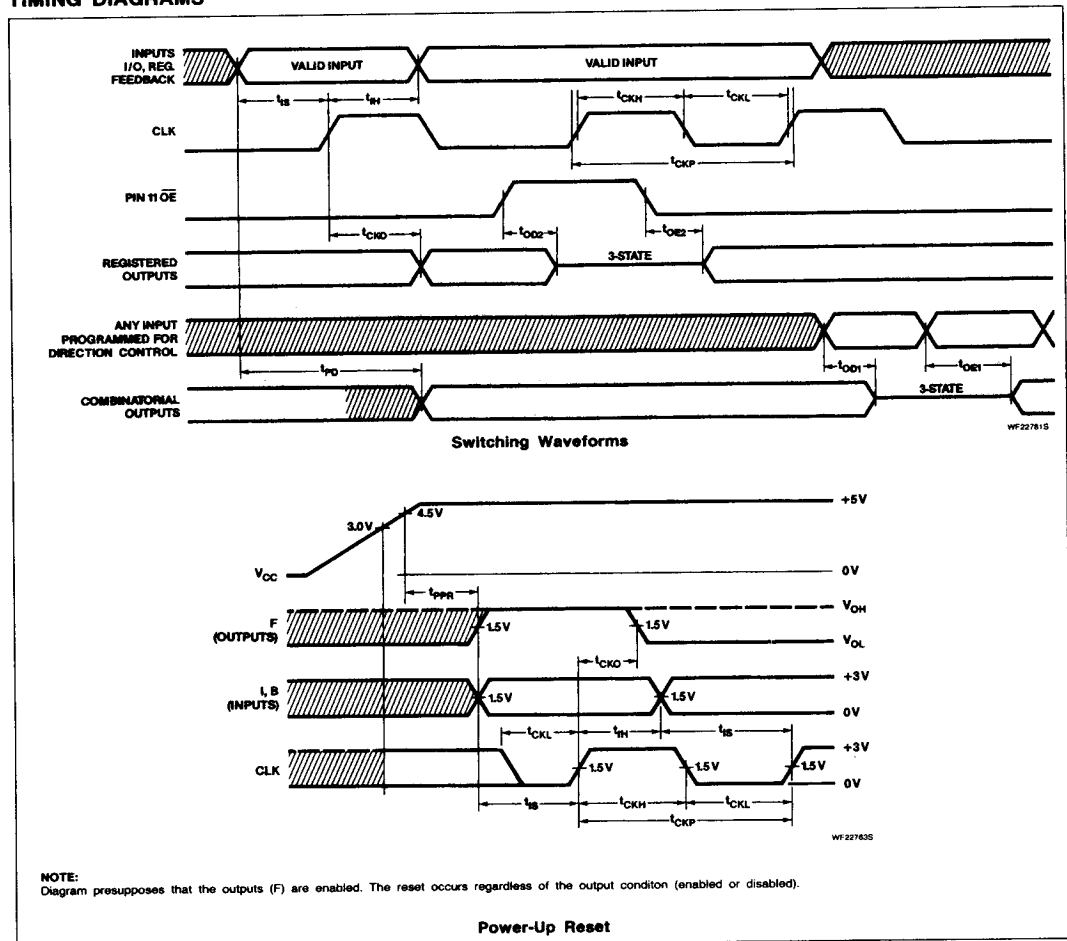
### POWER-UP RESET

In order to facilitate state machine design and testing, a power-up reset function has been incorporated in the PLC16V8. All internal registers will reset to active-Low (logical "0") after a specified period of time ( $t_{PPR}$ ). Therefore, any OMC that has been configured as a

registered output will always produce an active-High on the associated output pin because of the inverted output buffer. The internal feedback ( $\bar{Q}$ ) of a registered OMC will also be set High. The programmed polarity of OMC will not affect the active-High output condition during a system power-up condition.

The following conditions must be considered when the asynchronous power-up reset occurs.  $V_{CC}$  rise to 4.5V (90%) must be monotonic. The clock input must stabilize to a valid TTL level prior to the  $V_{CC}$  rise to 60% (3.0V). All input setup and hold times ( $t_{IS}$  and  $t_{IH}$ ) must be adhered to prior to clocking the device.

### TIMING DIAGRAMS



# Erasable and OTP PAL<sup>®</sup>-Type Device

## PLC16V8 Series

### REGISTER PRELOAD FUNCTION (DIAGNOSTIC MODE ONLY)

In order to facilitate the testing of state machine/controller designs, a diagnostic mode register preload feature has been incorporated into the PLC16V8 series device. This feature enables the user to load the registers

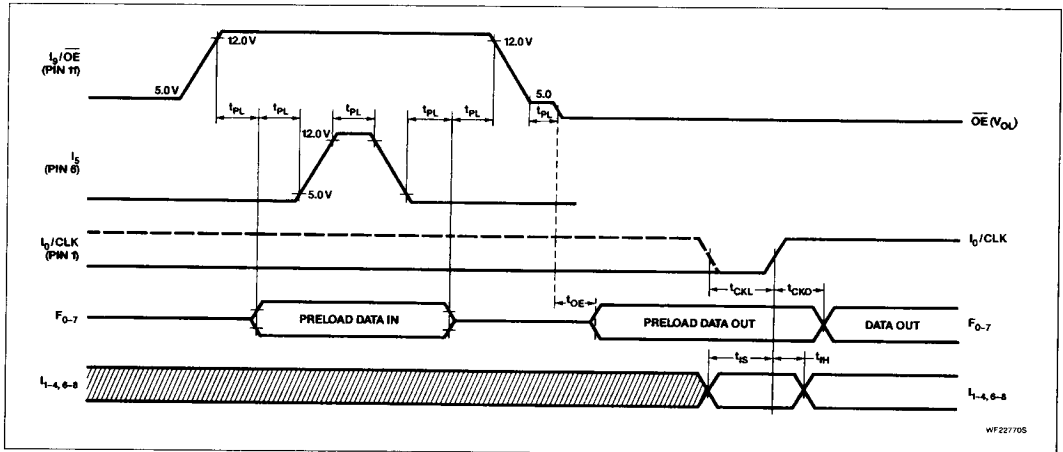
with predetermined states while a super voltage is applied to Pins 11 and 6 ( $I_9/\overline{OE}$  and  $I_5$ ). (See diagram for timing and sequence.)

To read the data out, Pins 11 and 6 must be returned to normal TTL levels. The outputs,  $F_0-7$ , must be enabled in order to read data out. The Q outputs of the registers will reflect

data in as input via  $F_0-7$  during preload. Subsequently, the register Q output via the feedback path will reflect the complement of the data in as input via  $F_0-7$ .

Refer to the voltage waveform for timing and voltage references.

### REGISTER PRELOAD (DIAGNOSTIC MODE)



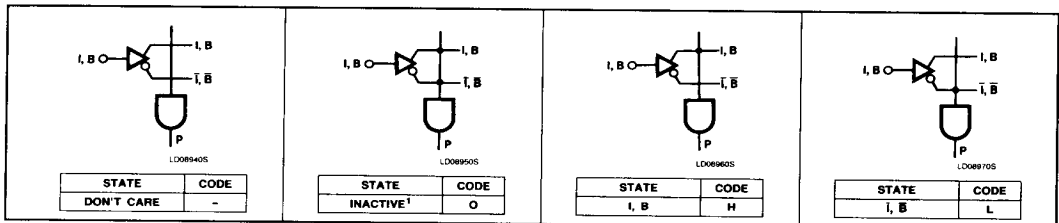
### LOGIC PROGRAMMING

The FPLA can be programmed by means of Logic Programming equipment.

With Logic programming, the AND/Ex-OR gate input connections necessary to implement the desired logic function are coded directly from logic equations using the Program Table. Similarly, various OMC configurations are implemented by programming the Architecture Control bits AC1 and AC2, as shown below. Note that the configuration cell is automatically programmed based on the OMC configuration.

In this table, the logic state of variables I, P, and B associated with each Sum Term S is assigned a symbol which results in the proper fusing pattern of corresponding link pairs, defined as follows:

### "AND" ARRAY — (I, B)

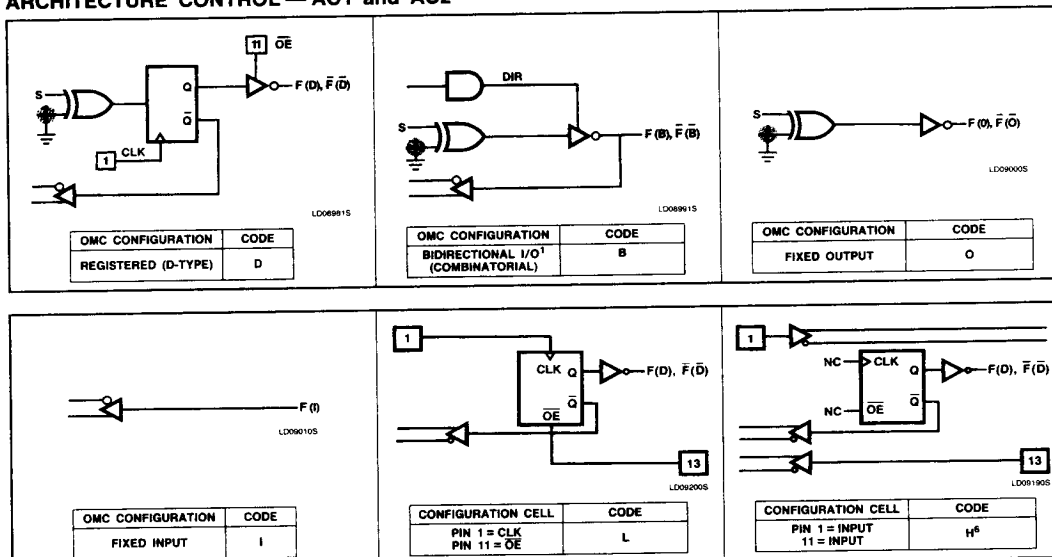




# Erasable and OTP PAL®-Type Device

## PLC16V8 Series

### ARCHITECTURE CONTROL — AC1 and AC2



#### NOTE:

- A factory shipped unprogrammed device is configured such that:
1. All cells are in a conductive state.
2. All AND gates are pulled to a logic "0" (Low).
3. Output polarity is non-inverting.
4. Pins 1 and 11 are configured as inputs 0 and 9. The clock and OE functions are disabled.
5. All Output Macro Cells (OMCs) are configured as bidirectional I/O, with the outputs disabled via the direction term.
6. This configuration cannot be used if any OMCs are configured as registered (Code = D). The configuration cell will be automatically configured to ensure that the clock and output enable functions are enabled on Pins 1 and 11, respectively, if any one OMC is programmed as registered.

### ERASURE CHARACTERISTICS (For Quartz Window Packages Only)

The erasure characteristics of the PLC16V8 Series devices are such that erasure begins to occur upon exposure to light with wavelengths shorter than approximately 4000 Angstroms ( $\text{\AA}$ ). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000 – 4000 $\text{\AA}$  range. Data shows that constant exposure to room level fluorescent lighting could erase a typical PLC16V8 in approximately three years, while

it would take approximately one week to cause erasure when exposed to direct sunlight. If the PLC16V8 is to be exposed to these types of lighting conditions for extended periods of time, opaque labels should be placed over the window to prevent unintentional erasure.

The recommended erasure procedure for the PLC16V8 is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms ( $\text{\AA}$ ). The integrated dose (i.e., UV intensity  $\times$  exposure time) for erasure should be a minimum of 15Wsec/cm<sup>2</sup>. The erasure

time with this dosage is approximately 30 to 35 minutes using an ultraviolet lamp with a 12,000 $\mu\text{W}/\text{cm}^2$  power rating. The device should be placed within one inch of the lamp tubes during erasure. The maximum integrated dose a CMOS EPLD can be exposed to without damage is 7258Wsec/cm<sup>2</sup> (1 week @ 12000 $\mu\text{W}/\text{cm}^2$ ). Exposure of these CMOS EPLDs to high intensity UV light for longer periods may cause permanent damage.

The maximum number of guaranteed erase/write cycles is 50. Data retention exceeds 20 years.

## PLC16V8 Series

| CONFIGURATION CELL (CLK/ $\overline{\text{OE}}$ CONTROL) |  |  |  |  |  |
|----------------------------------------------------------|--|--|--|--|--|
| ARCH. CONTROL BITS                                       |  |  |  |  |  |
| OUTPUT POLARITY                                          |  |  |  |  |  |

[illegible]

\* THE CONFIGURATION CELL IS AUTOMATICALLY PROGRAMMED BASED ON THE OMC ARCHITECTURE.

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