Signetics

PLS103
Field-Programmable Gate Array (16 × 9 × 9)

Signetics Programmable Logic
Product Specification

Application Specific Products
- **Series 28**

DESCRIPTION

The PLS103 is a bipolar, fuse Programmable Gate Array. The device consists of nine AND/NAND gates which share 16 common inputs. The type of gate is selected by programming the output as active-High (H) or active-Low (L). Each of the 16 inputs $I_0 - I_{15}$ can be programmed to provide the True (H), Complement (L), or Don't Care (—) state to each of the nine AND/NAND gates. OR/NOR logic functions can also be implemented by complementing the inputs and outputs via on-chip inverting buffers.

The device is field programmable, which means that custom patterns are immediately available.

The PLS103 includes chip-enable control for output strobing and inhibit. It features 3-State outputs for ease of expansion of input variables and application in bus-organized systems.

Order codes are listed in the Ordering Information Table.

FEATURES

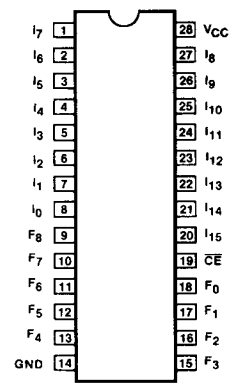
- **Field-Programmable (Ni-Cr link)**
- **16 input variables**
- **9 output functions**
- **Chip Enable input**
- **I/O propagation delay: 35ns (max.)**
- **Power dissipation: 600mW (typ.)**
- **Input loading: −100μA (max.)**
- **3-State outputs**
- **Output disable function: Hi-Z**
- **Fully TTL compatible**

APPLICATIONS

- **Random logic**
- **Address decoders**
- **Code detectors**
- **Peripheral selectors**
- **Fault monitors**
- **Machine state decoders**

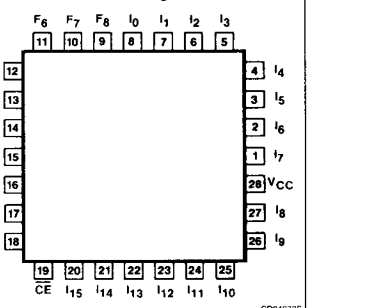
PIN CONFIGURATIONS

N Package



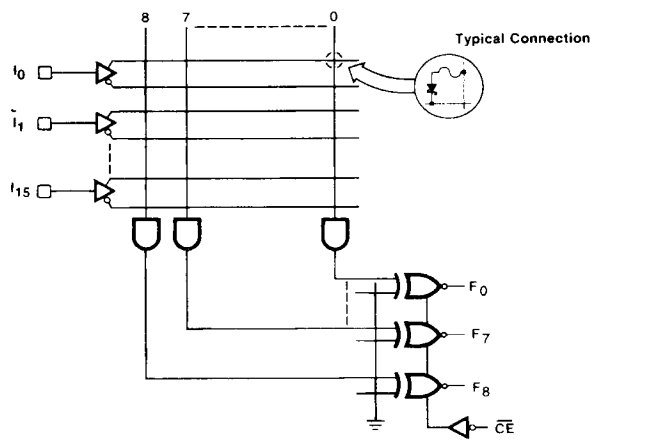
CD04285S

A Package



CD04272S

FUNCTIONAL DIAGRAM



LD01460S

Fusible Ni-Cr links are initially intact at all array cross-points.

LOGIC FUNCTION

TYPICAL OUTPUT FUNCTIONS:

ACTIVE-HIGH

$$X = A \cdot \overline{B} \cdot C \cdot \ldots$$

ACTIVE-LOW

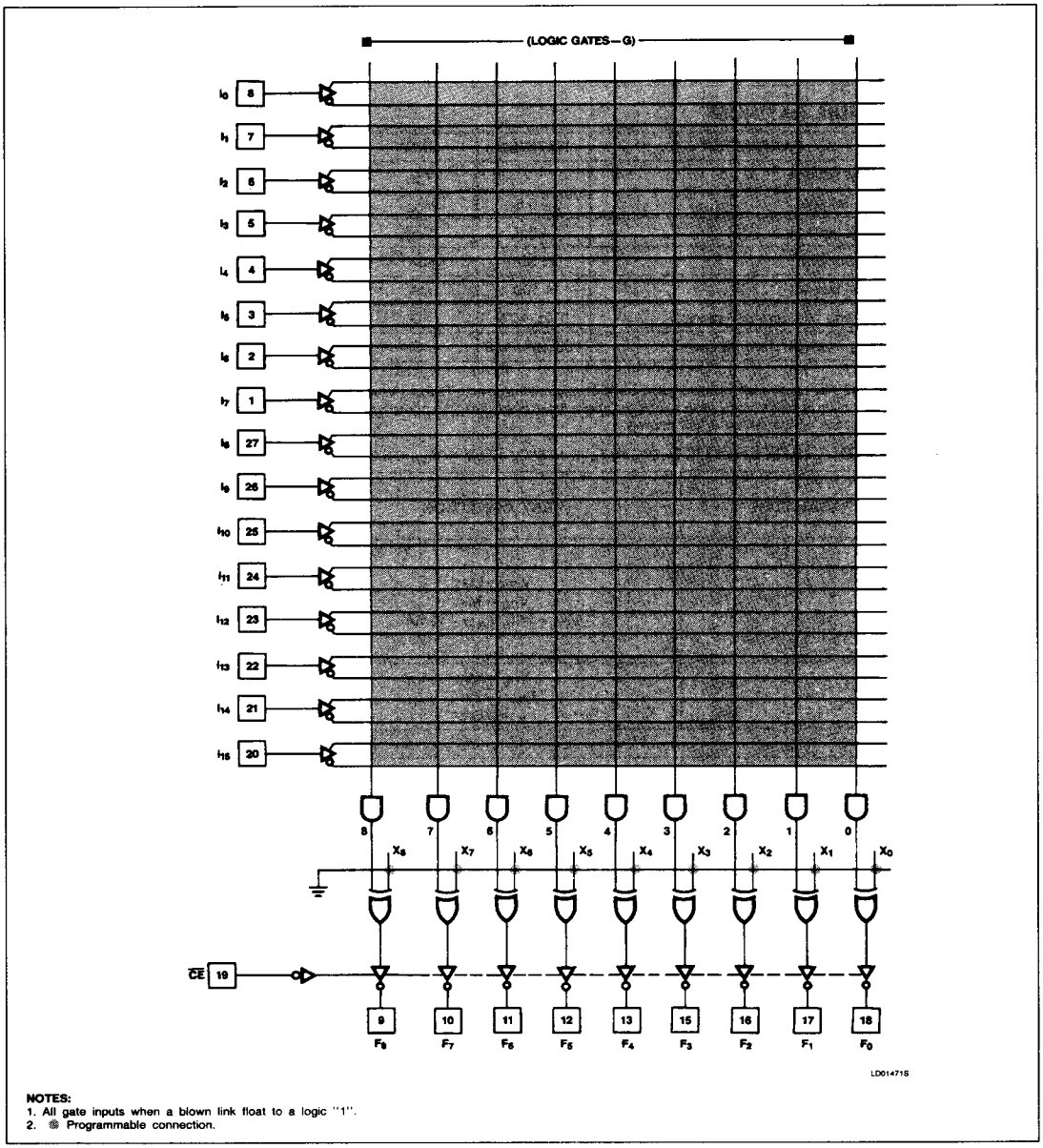
$$X = \overline{A \cdot \overline{B} \cdot C \cdot \ldots}$$
$$X = \overline{A} + B + \overline{C} + \ldots$$

NOTES:
1. For each of the 9 outputs, either function X (active-High) or $\overline{X}$ (active-Low) is available, but not both. The desired output polarity is programmed via the Ex-OR gates.
2. X, A, B, C, etc. are user defined connections to fixed inputs (I) and output pins (O).

Field-Programmable Gate Array (16 × 9 × 9)

PLS103

FPGA LOGIC DIAGRAM



NOTES:
1. All gate inputs when a blown link float to a logic "1".
2. ⊛ Programmable connection.

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PLS103

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
28-pin Plastic DIP 600mil-wide	PLS103N
28-pin Plastic Leaded Chip Carrier	PLS103A

THERMAL RATINGS

TEMPERATURE	
Maximum junction	150°C
Maximum ambient	75°C
Allowable thermal rise ambient to junction	75°C

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATINGS	UNIT
V_{CC}	Supply voltage	+7	V_{DC}
V_{IN}	Input voltage	+5.5	V_{DC}
V_O	Output voltage	+5.5	V_{DC}
I_{IN}	Input current	±30	mA
I_{OUT}	Output current	+100	mA
T_A	Operating temperature range	0 to +75	°C
T_{STG}	Storage temperature range	−65 to +150	°C

NOTE:

1. Stresses above those listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other conditions above those indicated in the operational and programming specification of the device is not implied.

DC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS			UNIT
			Min	Typ[2]	Max	
Input voltage[1]						
V_{IH}	High	V_{CC} = Max	2.0			V
V_{IL}	Low	V_{CC} = Min			0.8	V
V_{IC}	Clamp[3]	V_{CC} = Min, I_{IN} = −12mA		−0.8	−1.2	V
Output voltage[1]						
V_{OH}	High[5]	V_{CC} = Min I_{OH} = −2mA	2.4			V
V_{OL}	Low[4]	I_{OL} = 9.6mA		0.35	0.45	V
Input current						
I_{IH}	High	V_{IN} = 5.5V		< 1	25	μA
I_{IL}	Low	V_{IN} = 0.45V		−10	−100	μA
Output current						
$I_{O(OFF)}$	Hi-Z state	$\overline{CE}$ = High, V_{CC} = Max V_{OUT} = 5.5V		1	40	μA
		V_{OUT} = 0.45V		−1	−40	
I_{OS}	Short circuit[3,6]	$\overline{CE}$ = Low, V_{OUT} = 0V	−15		−70	mA
I_{CC}	V_{CC} supply current[7]	V_{CC} = Max		120	170	mA
Capacitance						
C_{IN}	Input	V_{CC} = 5.0V V_{IN} = 2.0V		8		pF
C_{OUT}	Output	V_{OUT} = 2.0V		15		pF

Notes on following page.

Field-Programmable Gate Array (16 × 9 × 9)

AC ELECTRICAL CHARACTERISTICS $R_1 = 470\Omega$, $R_2 = 1k\Omega$, $C_L = 30pF$, $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TO	FROM	LIMITS			UNIT
				Min	Typ[2]	Max	
Propagation delay							
t_{PD}	Input	Output	Input		20	35	ns
t_{CE}	Chip enable	Output	Chip enable		15	30	ns
Disable time							
t_{CD}	Chip disable	Output	Chip enable		15	30	ns

NOTES:
1. All voltage values are with respect to network ground terminal.
2. All typical values are at $V_{CC} = 5V$, $T_A = +25°C$.
3. Test one pin at a time.
4. Measure with a programmed logic condition for which the output under test is at a low logic level. Output sink current is supplied through a resistor to V_{CC}.
5. Measured with V_{IL} applied to $\overline{CE}$ and a logic high at the output.
6. Duration of short circuit should not exceed 1 second.
7. I_{CC} is measured with the outputs open.

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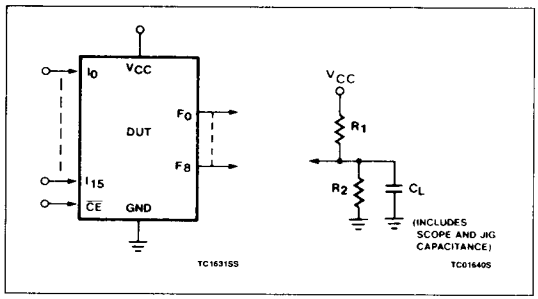
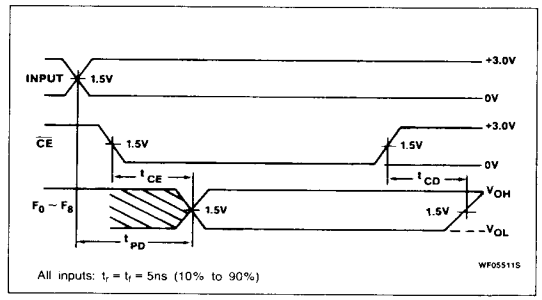
PLS103

TEST LOAD CIRCUITS



VOLTAGE WAVEFORMS



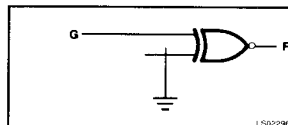
LOGIC PROGRAMMING

In a virgin device all Ni-Cr links are intact. PLS013 logic designs can be generated using Signetics' AMAZE PLD design software or one of several other commercially available, JEDEC standard PLD design software packages. Boolean and/or state equation entry is accepted.

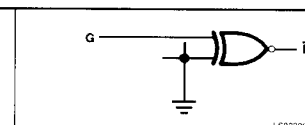
PLS013 logic designs can also be generated using the program table entry format detailed on the following pages. This program table entry format is supported by the Signetics' AMAZE PLD design software (PTP module). AMAZE is available free of charge to qualified users.

To implement the desired logic functions, the state of each logic variable from logic equations (I, B, O, P, etc.) is assigned a symbol. The symbols for TRUE, COMPLEMENT, INACTIVE, PRESET, etc., are defined below.

OUTPUT POLARITY – (F)

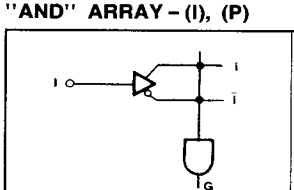


ACTIVE LEVEL	CODE
HIGH (NON-INVERTING)	H



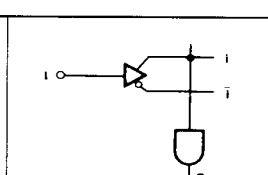
ACTIVE LEVEL	CODE
LOW[1] (INVERTING)	L

"AND" ARRAY – (I), (P)



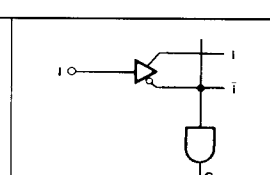
STATE	CODE
INACTIVE[1,2]	O

LS02310S



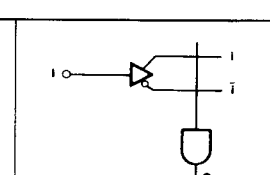
STATE	CODE
I	H

LS02320S



STATE	CODE
I	L

LS02330S



STATE	CODE
DON'T CARE	—

LS02340S

NOTES:
1. This is the initial unprogrammed state of all links.
2. Any gate G_n will be unconditionally inhibited if both the True and Complement fuses of any input (I) are left intact.

VIRGIN STATE

The PLS103 virgin device is factory shipped in an unprogrammed state, with all fuses intact, such that:

1. All P_n terms are disabled (inactive).
2. All P_n terms are active on all outputs.
3. All outputs are active-Low.

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PLS103

FPGA PROGRAM TABLE

CUSTOMER NAME _____	THIS PORTION TO BE COMPLETED BY SIGNETICS
PURCHASE ORDER # _____	CF (XXXX) _____
SIGNETICS DEVICE # _____	CUSTOMER SYMBOLIZED PART # _____
TOTAL NUMBER OF PARTS _____	DATE RECEIVED _____
PROGRAM TABLE # _____	COMMENTS _____

F_0 (18) = _____

F_1 (17) = _____

F_2 (16) = _____

F_3 (15) = _____

F_4 (13) = _____

F_5 (12) = _____

F_6 (11) = _____

F_7 (10) = _____

F_8 (9) = _____

GATE / POLARITY	INPUT I_{15}	I_{14}	I_{13}	I_{12}	I_{11}	I_{10}	I_9	I_8	I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0
F_0																
F_1																
F_2																
F_3																
F_4																
F_5																
F_6																
F_7																
F_8																
PIN NO.	20	21	22	23	24	25	26	27	1	2	3	4	5	6	7	8
VARIABLE NAME																

NOTES:
1. The FPGA is shipped with all links intact. Thus a background of entries corresponding to states of virgin links exists in the table, shown BLANK for clarity.
2. Unused Inputs are normally programmed Don't Care (—).
3. Unused Gates can be left blank.

PROGRAM TABLE ENTRIES

AND (I)	
INACTIVE	0
I	H
$\overline{I}$	L
Don't Care	—

CONTROL (POL.)	
HIGH	H
LOW	L

LD022605