# Programmable logic array ($18 \times 42 \times 10$)

# PLUS153–10

## DESCRIPTION

The PLUS153–10 PLD is a high speed, combinatorial Programmable Logic Array. The Philips Semiconductors state-of-the-art Oxide Isolated Bipolar fabrication process is employed to produce maximum propagation delays of 10ns or less.

The 20-pin PLUS153 device has a programmable AND array and a programmable OR array. Unlike PAL® devices, 100% product term sharing is supported. Any of the 32 logic product terms can be connected to any or all of the 10 output OR gates. Most PAL ICs are limited to 7 AND terms per OR function; the PLUS153–10 can support up to 32 input wide OR functions.

The polarity of each output is user-programmable as either Active-High or Active-Low, thus allowing AND-OR or AND-NOR logic implementation. This feature adds an element of design flexibility, particularly when implementing complex decoding functions.

The PLUS153–10 device is user-programmable using one of several commercially available, industry standard PLD programmers.

## FEATURES

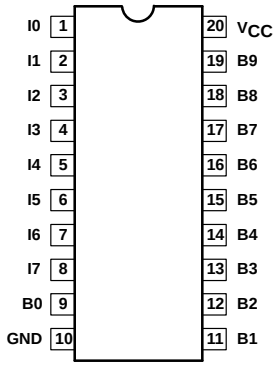
- I/O propagation delays (worst case)
  - PLUS153–10 – 10ns max.
- Functional superset of 16L8 and most other 20-pin combinatorial PAL devices
- Two programmable arrays
  - Supports 32 input wide OR functions
- 8 inputs
- 10 bi-directional I/O
- 42 AND gates
  - 32 logic product terms
  - 10 direction control terms
- Programmable output polarity
  - Active-High or Active-Low
- Security fuse
- 3-State outputs
- Power dissipation: 825mW (typ.)
- TTL Compatible

## APPLICATIONS

- Random logic
- Code converters
- Fault detectors
- Function generators
- Address mapping
- Multiplexing

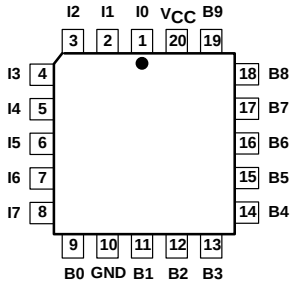
## PIN CONFIGURATIONS

**N Package**




N = Plastic DIP (300mil-wide)

**A Package**




A = Plastic Leaded Chip Carrier

## ORDERING INFORMATION

| DESCRIPTION | $t_{PD}$ (MAX) | ORDER CODE | DRAWING NUMBER |
|---|---|---|---|
| 20-Pin Plastic Dual-In-Line 300mil-wide | 10ns | PLUS153–10N | 0408D |
| 20-Pin Plastic Leaded Chip Carrier | 10ns | PLUS153–10A | 0400E |

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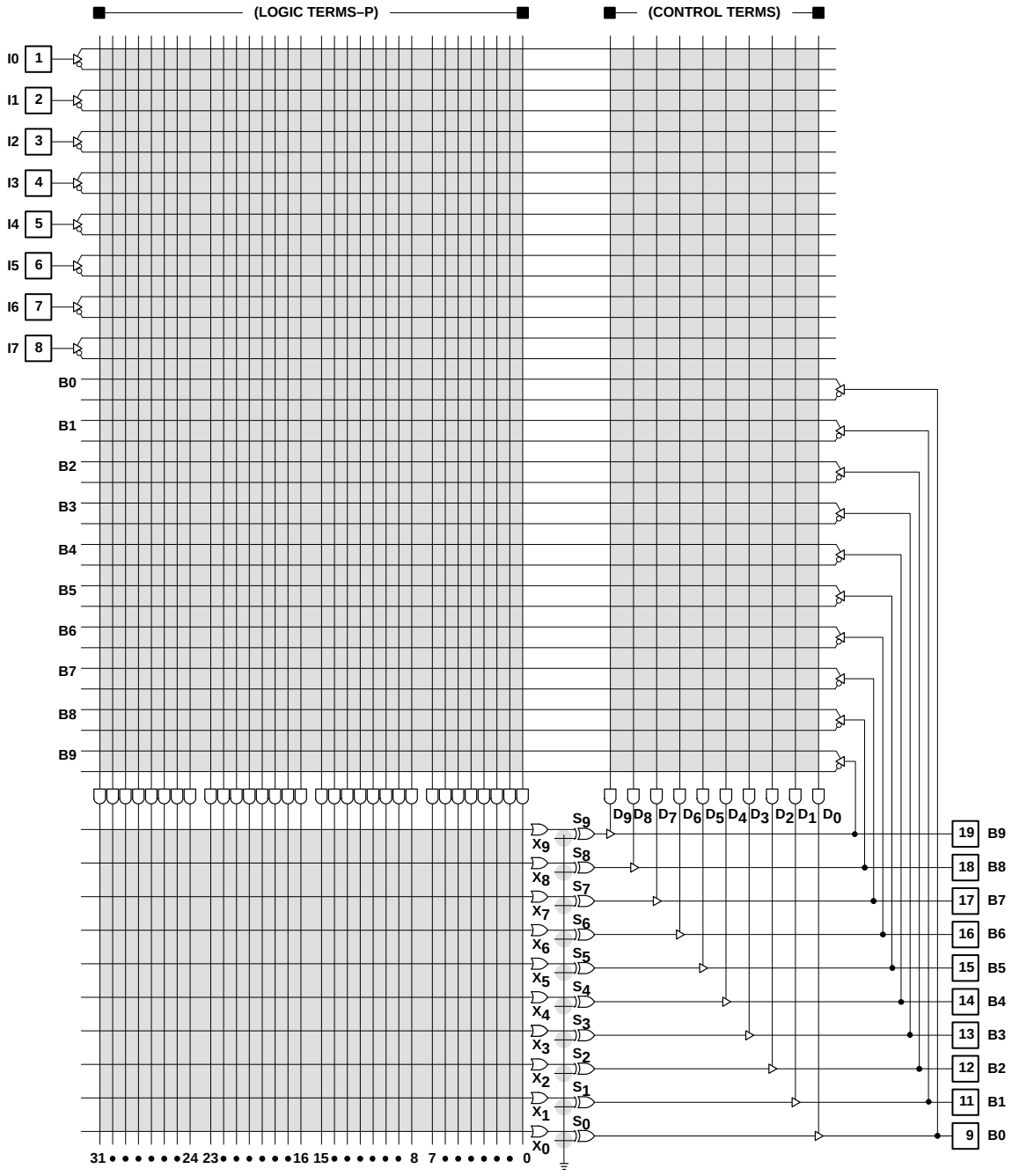
## LOGIC DIAGRAM




**NOTES:**
1. All programmed 'AND' gate locations are pulled to logic "1".
2. All programmed 'OR' gate locations are pulled to logic "0".
3. ● Programmable connection.

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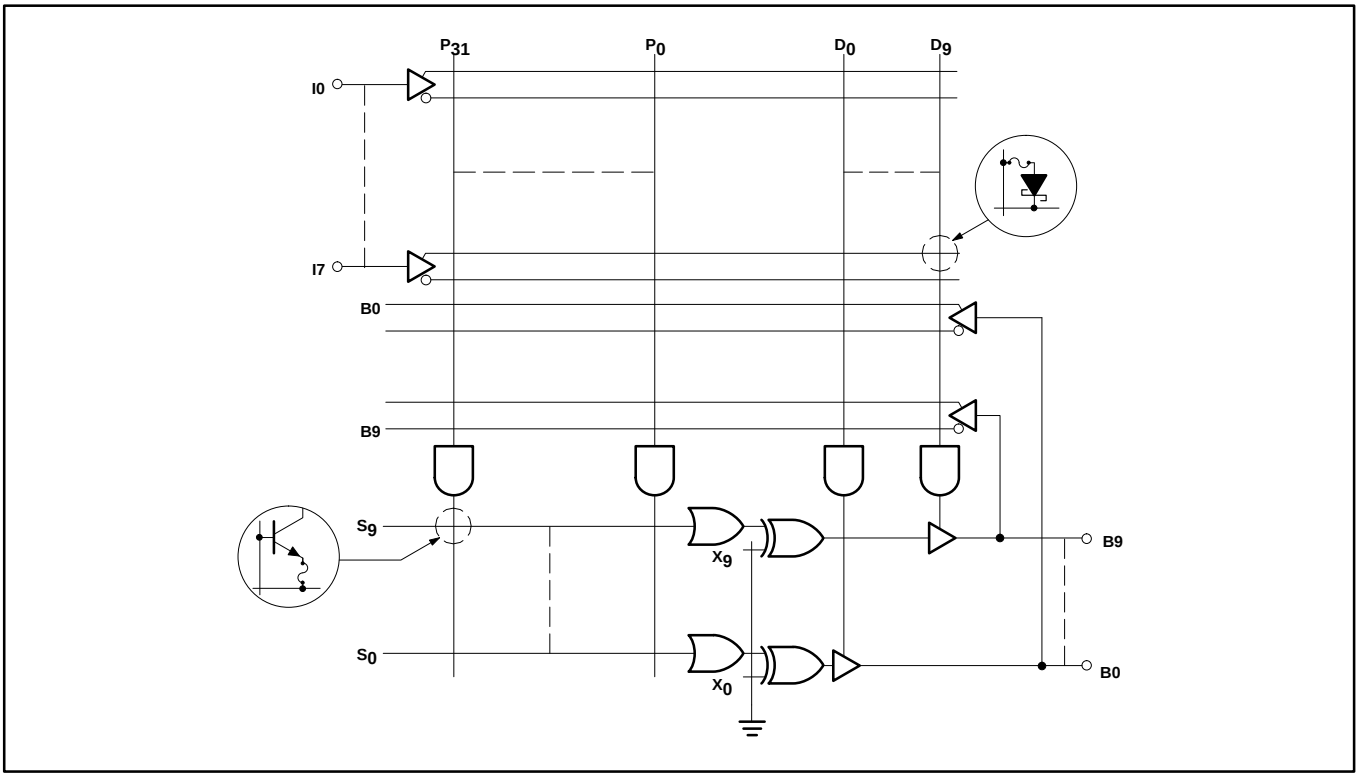
## FUNCTIONAL DIAGRAM




## ABSOLUTE MAXIMUM RATINGS[1]

| SYMBOL | PARAMETER | RATING MIN | RATING MAX | UNIT |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | +7 | $V_{DC}$ |
| $V_{In}$ | Input voltage | | +5.5 | $V_{DC}$ |
| $V_{OUT}$ | Output voltage | | +5.5 | $V_{DC}$ |
| $I_{IN}$ | Input currents | –30 | +30 | mA |
| $I_{OUT}$ | Output currents | | +100 | mA |
| $T_{amb}$ | Operating free-air temperature range | 0 | +75 | °C |
| $T_{stg}$ | Storage temperature range | –65 | +150 | °C |

**NOTES:**
1. Stresses above those listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification of the device is not implied.

## THERMAL RATINGS

| TEMPERATURE | |
|---|---|
| Maximum junction | 150°C |
| Maximum ambient | 75°C |
| Allowable thermal rise ambient to junction | 75°C |

## DC ELECTRICAL CHARACTERISTICS

$0°C \le T_{amb} \le +75°C$, $4.75 \le V_{CC} \le 5.25V$

| SYMBOL | PARAMETER | TEST CONDITIONS | LIMITS | | | UNIT |
|---|---|---|---|---|---|---|
| | | | MIN | TYP[1] | MAX | |
| **Input voltage[2]** | | | | | | |
| $V_{IL}$ | Low | $V_{CC}$ = MIN | | | 0.8 | V |
| $V_{IH}$ | High | $V_{CC}$ = MAX | 2.0 | | | V |
| $V_{IC}$ | Clamp | $V_{CC}$ = MIN, $I_{IN}$ = –12mA | | –0.8 | –1.2 | V |
| **Output voltage[2]** | | | | | | |
| | | $V_{CC}$ = MIN | | | | |
| $V_{OL}$ | Low[4] | $I_{OL}$ = 15mA | | 0.4 | 0.5 | V |
| $V_{OH}$ | High[5] | $I_{OH}$ = –2mA | 2.4 | 2.9 | | V |
| **Input current[9]** | | | | | | |
| | | $V_{CC}$ = MAX | | | | |
| $I_{IL}$ | Low | $V_{IN}$ = 0.45V | | –20 | –100 | µA |
| $I_{IH}$ | High | $V_{IN}$ = $V_{CC}$ | | 1 | 40 | µA |
| **Output current** | | | | | | |
| | | $V_{CC}$ = MAX | | | | |
| $I_{O(OFF)}$ | Hi-Z state[8] | $V_{OUT}$ = 2.7V | | 0 | 80 | µA |
| | | $V_{OUT}$ = 0.45V | | –15 | –140 | |
| $I_{OS}$ | Short circuit[3, 5, 6] | $V_{OUT}$ = 0V | –15 | –30 | –70 | mA |
| $I_{CC}$ | $V_{CC}$ supply current[7] | $V_{CC}$ = MAX | | 165 | 200 | mA |
| **Capacitance** | | | | | | |
| | | $V_{CC}$ = 5V | | | | |
| $C_{IN}$ | Input | $V_{IN}$ = 2.0V | | 8 | | pF |
| $C_B$ | I/O | $V_B$ = 2.0V | | 15 | | pF |

**NOTES:**
1. All typical values are at $V_{CC}$ = 5V, $T_{amb}$ = +25°C.
2. All voltage values are with respect to network ground terminal.
3. Test one at a time.
4. Measured with inputs I0 – I2 = 0V, inputs I3 – I5 = 4.5V, inputs I7 = 4.5V and I6 = 10V. For outputs B0 – B4 and for outputs B5 – B9 apply the same conditions except I7 = 0V.
5. Same conditions as Note 4 except I7 = +10V.
6. Duration of short circuit should not exceed 1 second.
7. $I_{CC}$ is measured with inputs I0 – I7 and B0 – B9 = 0V.
8. Leakage values are a combination of input and output leakage.
9. $I_{IL}$ and $I_{IH}$ limits are for dedicated inputs only (I0 – I7).

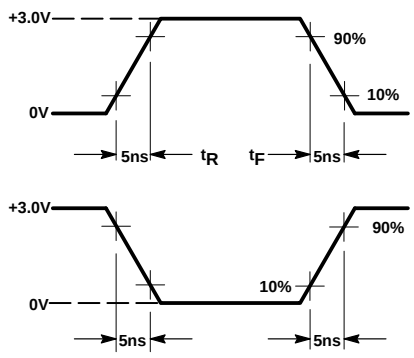
## AC ELECTRICAL CHARACTERISTICS

$0°C \le T_{amb} \le +75°C$, $4.75V \le V_{CC} \le 5.25V$, $R_1 = 300\Omega$, $R_2 = 390\Omega$

| SYMBOL | PARAMETER | FROM | TO | TEST CONDITION | LIMITS | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | | MIN | TYP | MAX | |
| $t_{PD}$ | Propagation Delay[2] | Input +/– | Output +/– | $C_L$ = 30pF | | 8 | 10 | ns |
| $t_{OE}$ | Output Enable[1] | Input +/– | Output – | $C_L$ = 30pF | | 8 | 10 | ns |
| $t_{OD}$ | Output Disable[1] | Input +/– | Output + | $C_L$ = 5pF | | 8 | 10 | ns |

**NOTES:**
1. For 3-State output; output enable times are tested with $C_L$ = 30pF to the 1.5V level, and $S_1$ is open for high-impedance to High tests and closed for high-impedance to Low tests. Output disable times are tested with $C_L$ = 5pF. High-to-High impedance tests are made to an output voltage of $V_T = (V_{OH} – 0.5V)$ with $S_1$ open, and Low-to-High impedance tests are made to the $V_T = (V_{OL} + 0.5V)$ level with $S_1$ closed.
2. All propagation delays are measured and specified under worst case conditions.

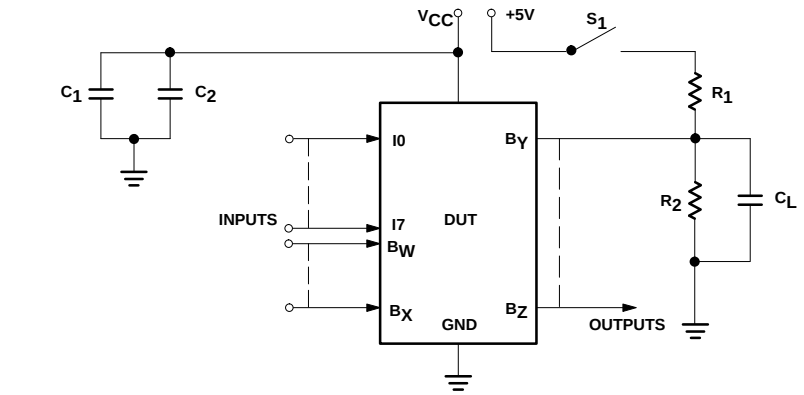
## VOLTAGE WAVEFORMS




**MEASUREMENTS:**
All circuit delays are measured at the +1.5V level of inputs and outputs, unless otherwise specified.

**Input Pulses**

## TEST LOAD CIRCUIT

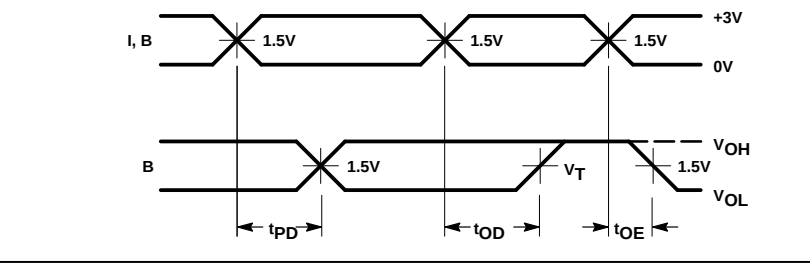



**NOTE:**
$C_1$ and $C_2$ are to bypass $V_{CC}$ to GND.

## TIMING DEFINITIONS

| SYMBOL | PARAMETER |
|---|---|
| $t_{PD}$ | Propagation delay between input and output. |
| $t_{OD}$ | Delay between input change and when output is off (Hi-Z or High). |
| $t_{OE}$ | Delay between input change and when output reflects specified output level. |

## TIMING DIAGRAM



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## LOGIC PROGRAMMING

The PLUS153–10 is fully supported by industry standard (JEDEC compatible) PLD CAD tools, including Philips Semiconductors SNAP design software package. ABEL™ and CUPL™ design software packages also support the PLUS153–10 architecture.

All packages allow Boolean and state equation entry formats. SNAP, ABEL and CUPL also accept, as input, schematic capture format.

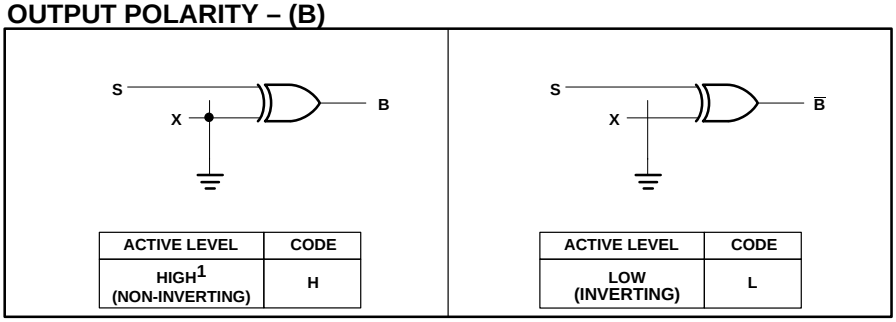
PLUS153–10 logic designs can also be generated using the program table entry format, which is detailed on the following page. This program table entry format is supported by SNAP only.

To implement the desired logic functions, the state of each logic variable from logic equations (I, B, O, P, etc.) is assigned a symbol. The symbols for TRUE, COMPLEMENT, INACTIVE, PRESET, etc., are defined below.

## PROGRAMMING AND SOFTWARE SUPPORT

Refer to Section 9 *(Development Software)* and Section 10 *(Third-Party Programmer/Software Support)* of this data handbook for additional information.

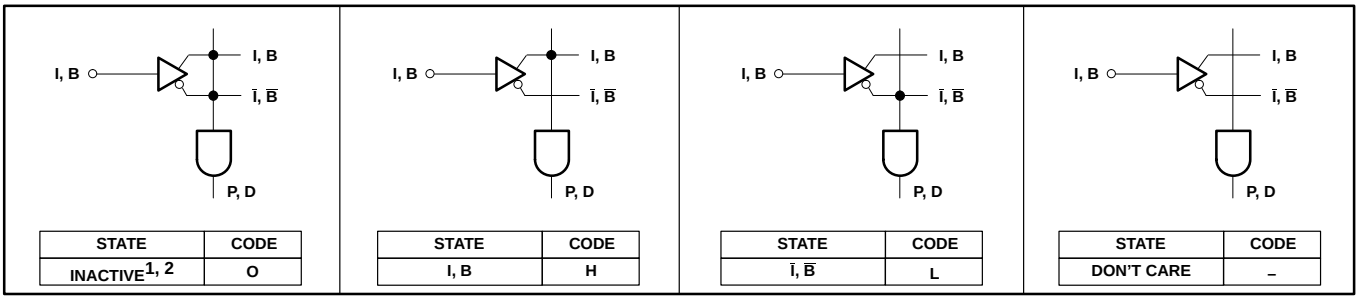
## OUTPUT POLARITY – (B)




| ACTIVE LEVEL | CODE |
|---|---|
| HIGH[1] (NON-INVERTING) | H |

| ACTIVE LEVEL | CODE |
|---|---|
| LOW (INVERTING) | L |

## AND ARRAY – (I, B)



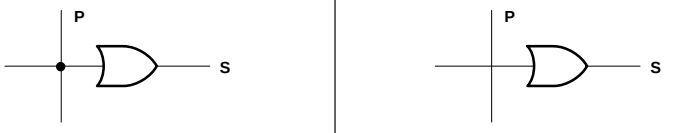

| STATE | CODE |
|---|---|
| INACTIVE[1, 2] | O |

| STATE | CODE |
|---|---|
| I, B | H |

| STATE | CODE |
|---|---|
| $\overline{I}$, $\overline{B}$ | L |

| STATE | CODE |
|---|---|
| DON'T CARE | – |

## OR ARRAY – (B)




| $P_n$ STATUS | CODE |
|---|---|
| ACTIVE[1] | A |

| $P_n$ STATUS | CODE |
|---|---|
| INACTIVE | ● |

**NOTES:**
1. This is the initial unprogrammed state of all links.
2. Any gate $P_n$ will be unconditionally inhibited if both the true and complement of an input (either I or B) are left intact.

## VIRGIN STATE

A factory shipped virgin device contains all fusible links intact, such that:

1. All outputs are at "H" polarity.
2. All $P_n$ terms are disabled.
3. All $P_n$ terms are active on all outputs.

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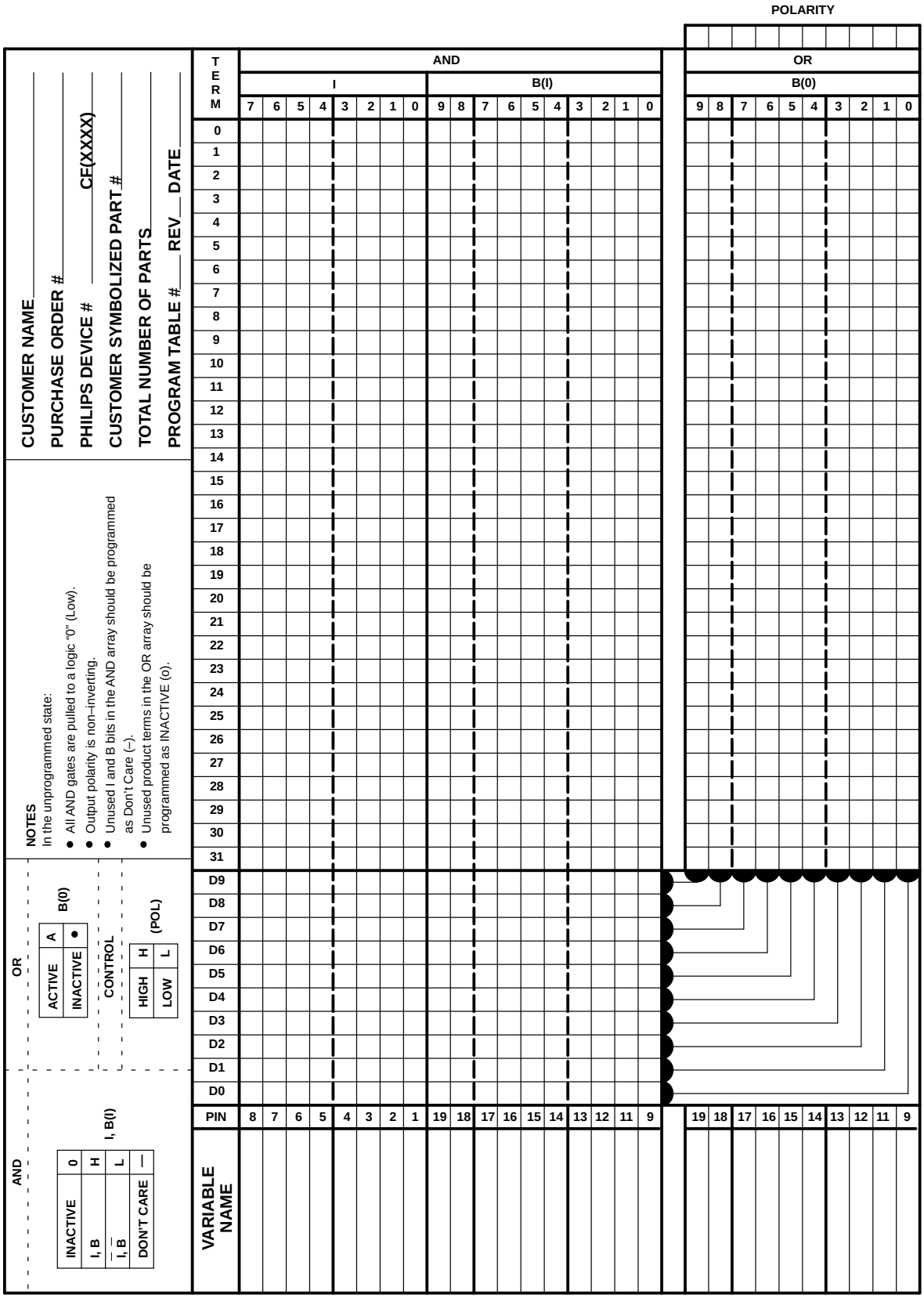
## PROGRAM TABLE



## SNAP RESOURCE SUMMARY DESIGNATIONS