FEATURES

- Integrates four full-duplex T1 Extended Superframe (ESF) facility data link interfaces in a single device.
- Provides termination of each independent ESF data link at either the full 4 kbit/s, or at a 2 kbit/s data rate compatible with ZBTSI encoding.
- Detects and generates bit-oriented codes on each ESF data link.
- Provides four independent, full-duplex transceivers, suitable for general-purpose HDLC applications up to 2 Mbit/s.
- Allows reception and transmission of T1.403 and PUB 54016 messages.
- Also capable of terminating the T3 C-bit parity format path maintenance data link and far-end alarm and control channel.
- Supports polled, interrupt-driven, or DMA servicing of the HDLC interfaces.
- Provides a generic 8-bit microprocessor bus interface for configuration, control and status monitoring.
- Low power CMOS technology.
- 68-pin PLCC package.

APPLICATIONS

- General Purpose HDLC data link processing.
- T1.403 and Pub 54016 data link processing.
- DS-3 C-bit path maintenance and far-end alarm and control processing.
- Ideal for use in multiplexers, CSUs, DACs, transmission and other telecommunications equipment.

REFERENCES

- American National Standard for Telecommunications, ANSI T1.403-1989 - "Carrier to Customer Installation - DS1 Metallic Interface Specification."
- American National Standard for Telecommunications, ANSI T1.107-1988 - "Digital Hierarchy - Formats Specification."
- American National Standard for Telecommunications, ANSI T1.103-1987 - "Digital Hierarchy - Synchronous DS3 Format Specifications."
- American National Standard for Telecommunications, ANSI T1.404-1989 - "Carrier to Customer Installation - DS3 Metallic Interface Specification."
- AT&T, PUB 54016, - "Requirements For Interfacing Digital Terminal Equipment to Service Employing the Extended Superframe Format," October 1984.
- Bell Communications Research, TA-TSY-000147 - "DS1 Rate Digital Service Monitoring Unit Functional Specifications," Issue 1, October 1987.
- Bell Communications Research, TR-TSY-000194 - "The Extended Superframe Format Interface Specification," Issue 1, December 1987.
- CCITT Blue Book, Recommendation Q.921 - "ISDN User-Network Interface Data Link Layer Specification", Volume VI, Fascicle VI.9, 1988.
- International Organization for Standardization, ISO 3309:1984 - "High-Level Data Link Control Procedures -- Frame Structure".
- Pacific Microelectronics Centre, "T1 Solutions Databook," Issue 1, 1990.

DESCRIPTION

The PM4374 QFDL Quad Facility Data Link Transceiver provides termination of up to four independent T1 Extended Superframe (ESF) facility data link (FDL) channels. Each channel handles LAPD/HDLC traffic, and supports bit-oriented code generation and detection. A single QFDL can terminate the data links of four ESF or ZBTSI format DS1 signals. The QFDL may also be used to terminate the path maintenance data link and the far end alarm and control channel of T3 systems that utilize the C-bit parity format. A single QFDL can terminate the data links and alarm and control channels of two C-bit parity format DS3 signals. The QFDL is implemented using the PMC Telecom System Block (TSB) library of ASIC functional blocks.

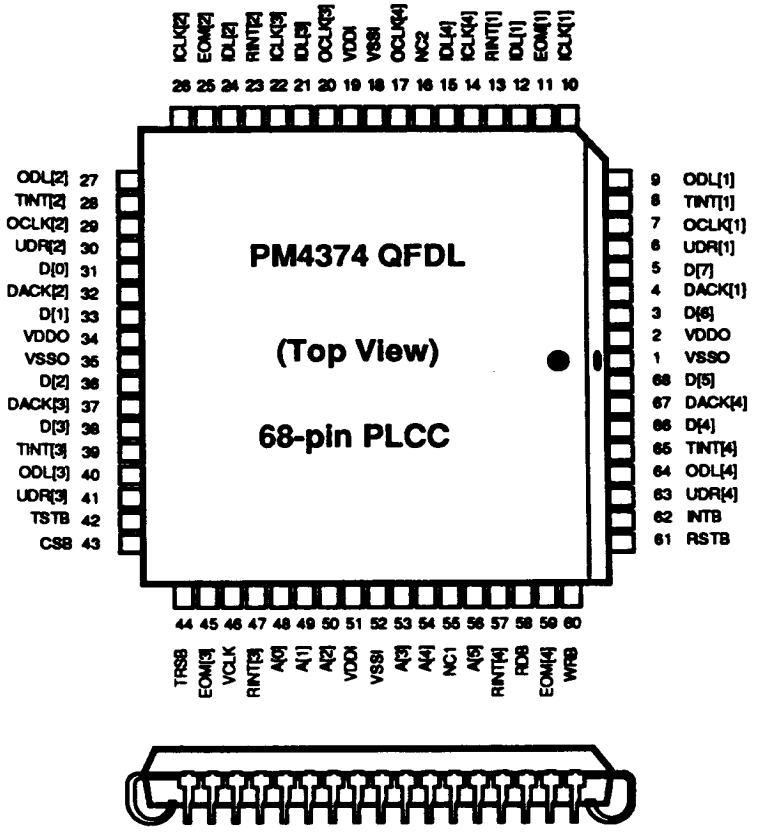
Each channel of the QFDL provides a full-duplex HDLC interface. The transmitter and receiver for each channel have individual clock inputs, and may be run at independent rates. The transmitter is implemented using the PM4105 XFDL T1 Data Link Transmitter TSB. The receiver uses the PM4206 RFDL T1 Data Link Receiver TSB, which includes a 4-byte FIFO receive buffer. Each HDLC interface supports polled, interrupt-driven and DMA servicing.

Each channel of the QFDL supports the detection and generation of ESF bit-oriented codes (BOCs). The transmission of BOCs is done by the PM4106 XBOC T1 Bit-Oriented Code Transmitter TSB. The reception of BOCs is handled by the PM4211 RBOC T1 Bit-Oriented Code Detector TSB, which supports polled or interrupt-driven servicing.

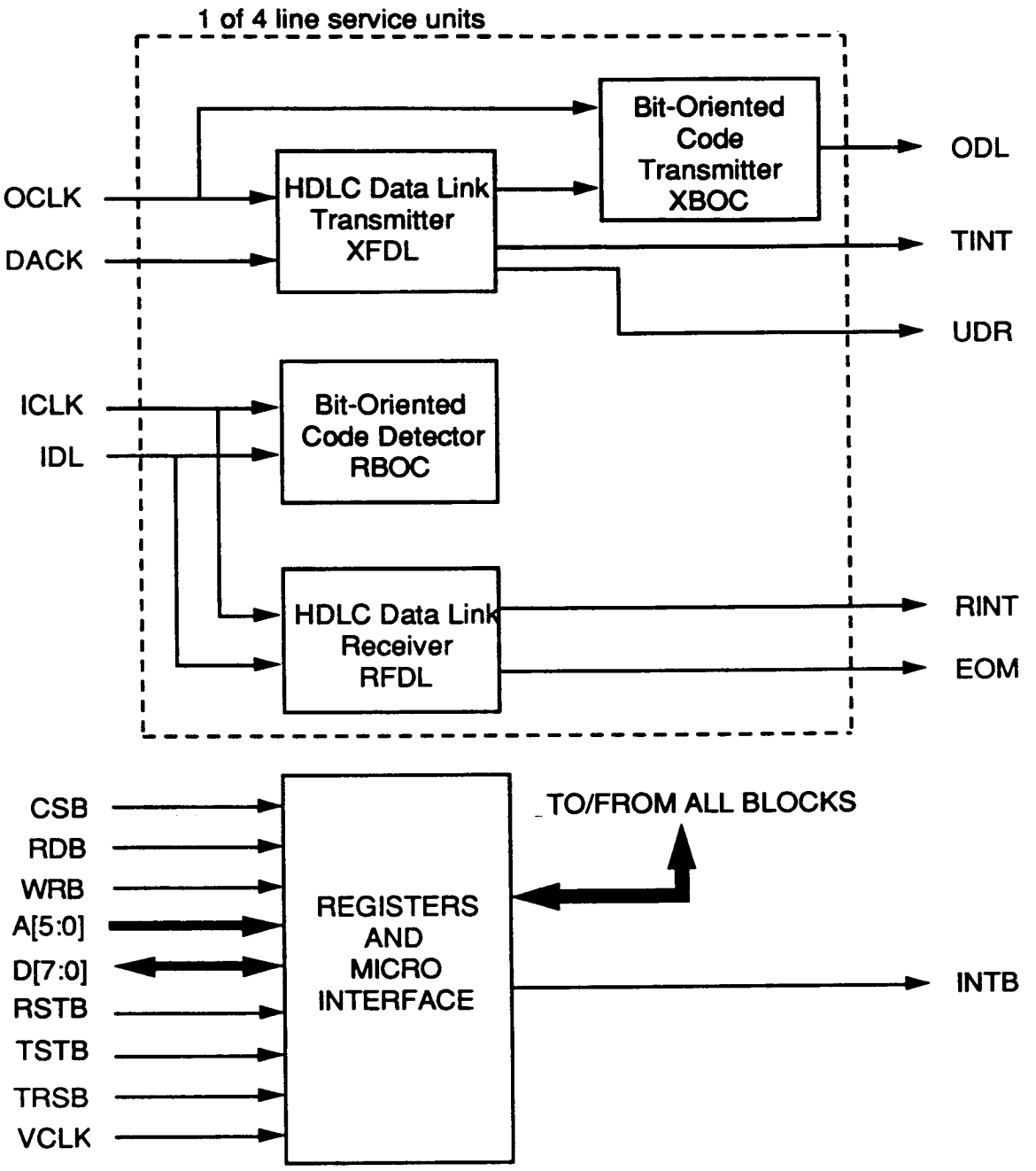
The QFDL is configured, controlled and monitored via a generic 8-bit microprocessor bus through which all internal registers are accessed. All sources of interrupts can be identified, acknowledged, or masked via this interface.

PACKAGE AND PINOUT

The QFDL is packaged in a 68-pin PLCC package.



BLOCK DIAGRAM



CONNECTOR DESCRIPTION

Pin Name	Type	Pin No.	Function
IDL[1] IDL[2] IDL[3] IDL[4]	Input	15 21 11 25	Each input data link (IDL[4:1]) signal is sampled on the rising edge of its corresponding ICLK[4:1] signal.
ICLK[1] ICLK[2] ICLK[3] ICLK[4]	Input	16 20 12 24	The data link input clock (ICLK[4:1]) signals are nominally 2 kHz or 4kHz, 50% duty cycle clocks.
ODL[1] ODL[2] ODL[3] ODL[4]	Output	8 28 3 33	Each output data link (ODL[4:1]) signal is updated on the falling edge of its corresponding OCLK[4:1] signal.
OCLK[1] OCLK[2] OCLK[3] OCLK[4]	Input	14 22 10 26	The data link output clock (OCLK[4:1]) signals are nominally 2 kHz or 4kHz, 50% duty cycle clocks.
RINT[1] RINT[2] RINT[3] RINT[4]	Output	5 31 62 42	The active high receive interrupt (RINT[4:1]) signals go high when an event occurs which changes the status of the corresponding HDLC receiver. The RINT[4:1] signals are updated on the falling edge of the corresponding ICLK[4:1] signal.
EOM[1] EOM[2] EOM[3] EOM[4]	Output	4 32 61 43	The active high end of message (EOM[4:1]) signals go high when the last byte of a sequence is read from the corresponding HDLC receiver, or if that receiver's buffer overruns. The EOM[4:1] signals are updated on the falling edge of the corresponding ICLK[4:1] signal.
TINT[1] TINT[2] TINT[3] TINT[4]	Output	7 64 29 40	The active high transmit interrupt (TINT[4:1]) signals indicate that the last data byte written to the corresponding HDLC transmitter has been set up for transmission, and that another byte must be written to that channel of the QFDL. The TINT[4:1] signals are updated on the falling edge of the corresponding OCLK[4:1] signal.
DACK[1] DACK[2] DACK[3] DACK[4]	Input	4 32 37 67	The active high DMA request acknowledge (DACK[4:1]) signals forces the TINT[4:1] outputs low. This removes the DMA request when the TINT[4:1] outputs are used to drive the DMA controller.

UDR[1] UDR[2] UDR[3] UDR[4]	Output	6 30 63 41	The active high underrun (UDR[4:1]) signals indicate that the transmit buffer of the corresponding HDLC transmitter has underrun, and that transmission of the HDLC frame on that channel has been aborted. The UDR[4:1] signals are updated on the falling edge of the corresponding OCLK[4:1] signal.
INTB	Output	59	The active low interrupt (INTB) output is brought low when any of the TINT[4:1] or RINT[4:1] outputs go high, or when any of the bit-oriented code detectors detect a valid code, provided that the interrupt source in question is not masked. The TINT[4:1] and RINT[4:1] outputs may be masked completely or only masked from activating INTB. INTB goes high when the appropriate Interrupt Status Register is read, acknowledging the interrupt. Note that INTB will remain low until all active, unmasked interrupt sources are acknowledged. INTB is an open drain output.
CSB	Input	45	The active low chip select (CSB) signal must be low to enable QFDL register accesses.
D[0] D[1] D[2] D[3] D[4] D[5] D[6] D[7]	I/O	39 38 37 36 65 66 67 68	The bidirectional data bus (D[7:0]) is used during QFDL read and write accesses.
RDB	Input	53	The active low read enable (RDB) signal is pulsed low to enable a QFDL register read access. The QFDL drives the D[7:0] bus with the contents of the addressed register while RDB and CSB are both low.
WRB	Input	50	The active low write strobe (WRB) signal is pulsed low to enable a QFDL register write access. The D[7:0] bus contents are clocked into the addressed normal mode register on the rising edge of WRB while CSB is low.
VCLK	Input	17	The test vector clock (VCLK) signal is used during QFDL production testing to verify internal functionality.

TSTB	Input	44	The active low test mode select (TSTB) signal is low during QFDL production testing. TSTB must be high to enable normal operation.
RSTB	Input	60	The active low reset (RSTB) signal asynchronously resets the QFDL.
TRSB	Input	46	The test register select (TRSB) signal discriminates between normal and test mode register accesses. TRSB is low during test mode register accesses, and is high during normal mode register accesses. TRSB must be high to enable normal operation.
A[0] A[1] A[2] A[3] A[4] A[5]	Input	47 48 49 54 55 56	The address bits (A[5:0]) select specific registers during QFDL register accesses.
VDDO[0] VDDO[1]	Power	2 34	The pad ring power pins (VDDO[1:0]) must be connected to a common +5 VDC supply together with the VDDI[1:0] pins.
VDDI[0] VDDI[1]	Power	19 51	The core power pins (VDDI[1:0]) must be connected to a common +5 VDC supply together with the VDDO[1:0] pins.
VSSO[0] VSSO[1]	Ground	1 35	The pad ring ground pins (VSSO[1:0]) must be connected to a common ground together with the VSSI[1:0] pins.
VSSI[0] VSSI[1]	Ground	18 52	The core ground pins (VSSI[1:0]) must be connected to a common ground together with the VSSO[1:0] pins.

Notes on Pin Description:

1. VDDI and VSSI are the +5 V and ground connections, respectively, for the core circuitry of the device. VDDO and VSSO are the +5 V and ground connections, respectively, for the pad ring circuitry of the device. These power supply connections must all be utilized and must all connect to a common +5 V or ground rail, as appropriate. There is no low impedance connection within the PM4374 between the core and pad ring supply rails. Failure to properly make these connections may result in improper operation or damage to the device.
2. Inputs TSTB, RSTB, and TRSB have integral pull-up resistors and inputs DACK[4:1] and VCLK have integral pull-down resistors.

FUNCTIONAL DESCRIPTION

HDLC Data Link Transmitter

The HDLC Data Link Transmitter (XFDL) is a microprocessor peripheral designed to transmit LAPD/HDLC data frames on the ESF facility data link (FDL). The XFDL performs all data serialization, CRC generation, and zero-bit stuffing, as well as flag, idle, and abort sequence insertion.

When enabled, the XFDL continuously transmits the flag character (01111110). Data bytes to be transmitted by the XFDL are provided on an interrupt-driven basis by writing to a double-buffered Transmit Data Register. After the parallel-to-serial conversion of each data byte, an interrupt is generated to signal the controller to write the next byte into the Transmit Data Register. Upon completion of the frames, a CRC-CCITT frame check sequence (if CRC insertion has been enabled) or a flag (if CRC insertion has not been enabled) is transmitted, followed by idle flag sequences.

If there are more than five consecutive ones in the raw transmit data or in the CRC data, a zero is stuffed into the serial data output. This prevents the unintentional transmission of flag or abort characters.

Abort characters can be continuously transmitted at any time by setting a control bit. During transmission, an underrun situation can occur if data is not written to the Transmit Data Register before the previous byte has been depleted. In this case, an abort sequence is automatically transmitted, and the controlling processor is notified via the UDR signal.

Bit-Oriented Code Transmitter

The Bit-Oriented Code Transmitter (XBOC) transmits 63 of the possible 64 bit-oriented codes (BOCs) over the facility data link (FDL) channel in extended superframe (ESF) framing format. The 64th possible code (111111) is similar to the HDLC idle sequence and is used in the XBOC to disable transmission of any bit-oriented codes.

BOCs are transmitted on the FDL as a 16-bit sequence consisting of 8 ones, 1 zero, 6 code bits, and 1 trailing zero (111111110xxxxxx0). This sequence is continuously transmitted until disabled by forcing the six code bits to 111111.

HDLC Data Link Receiver

The HDLC Data Link Receiver (RFDL) is a microprocessor peripheral used to receive LAPD/HDLC frames on the ESF facility data link (FDL). The RFDL detects the change from flag characters to the first data frame byte, removes stuffed bits from the frame data, and computes the frame check sequence (CRC-CCITT) associated with the frame.

The RFDL places received data into a four-byte FIFO buffer. Interrupts can be enabled to occur after one, two, or three frame bytes have been received (programmable FIFO fill level), or disabled completely. Software selects the interrupt generation interval by assigning values to two bits in the RFDL Enable Register. Each read of the RFDL Data Register should be followed by a read of the RFDL Status Register. The RFDL Status Register contains a FIFO status bit (FE) that indicates the full/empty status of the four-byte FIFO. While the FE bit is a logic 0, the FIFO is not empty; successive reads of the RFDL Data Register must therefore be performed, followed by reads of the RFDL Status Register until the FE bit is a logic 1 (i.e., until the FIFO buffer is empty). The RFDL Data Register must not be read if the FE bit is a logic 1.

If the software selects the FIFO fill level to be two bytes before an interrupt is generated (i.e., 4 ms in an ESF 4 kbit/s message link), the corresponding maximum interrupt service time is 6 ms (i.e., 3 frame byte periods). If the maximum interrupt service time is exceeded, the overrun bit (OVR) in the RFDL Status Register is set to logic 1, and an interrupt is immediately generated. An interrupt is also generated upon reception of an abort sequence while the link is active. The FLG bit in the RFDL Status Register is set to logic 0 upon reception of an abort sequence.

Bit-Oriented Code Detector

The Bit-Oriented Code Detector (RBOC) detects the presence of 63 of the 64 possible bit-oriented codes (BOCs) transmitted in the facility data link (FDL) channel in ESF framing format. The 64th code ("111111") is identical to the HDLC Idle sequence and is ignored by the RBOC.

Bit-oriented codes are received on the FDL channel as 16-bit sequences, each consisting of 8 ones, a zero, 6 code bits, and a trailing zero ("111111110xxxxxx0"). BOCs are validated when repeated at least 10 times in normal ESF mode (4 kbit/s link) or at least 5 times in ESF mode with ZBTSI coding (2 kbit/s). The RBOC can be enabled to declare a received code valid if it has been observed for 8 out of 10 times or for 4 out of 5 times, as specified by the AVC bit in the RBOC Control Register.

Valid BOCs are indicated through the RBOC Interrupt Status Register. The BOC bits are set to all ones ("111111") if no valid code has been detected. The RBOC can be programmed to generate an interrupt when a detected code has been validated.

The RBOC can be programmed to generate an interrupt when the facility data link goes idle.

Registers and Microprocessor Interface

The Registers and Microprocessor Interface Block allows for device level configuration of each of the four Facility Data Link Transceivers in the QFDL package. For each transceiver interrupt status, loopback, and interrupt enable registers are provided. For the QFDL device there is a master interrupt status register and a master test register.

REGISTER DESCRIPTION

Normal mode registers are used to configure and monitor the operation of the QFDL. Normal mode registers (as opposed to test mode registers) are selected when TRSB (CBI[13]) is high.

Notes on Normal Mode Register Bits:

1. Writing values into unused register bits has no effect. Reading back unused bits can produce either a logic 1 or a logic 0; hence unused register bits should be masked off by software when read.

2. All configuration bits that can be written into can also be read back. This allows the processor controlling the TSB to determine the programming state of the block.

3. Writeable normal mode register bits are cleared to logic 0 upon reset unless otherwise noted.

4. Writing into read-only normal mode register bit locations does not affect TSB operation unless otherwise noted.

Normal Mode Register Memory Map (TRSB=1)

FDL1	FDL2	FDL3	FDL4	REGISTER DESCRIPTION
00H	10H	20H	30H	XFDL Configuration and Control
01H	11H	21H	31H	XFDL Status
02H	12H	22H	32H	XFDL Transmit Data
03H	13H	23H	33H	Unused
04H	14H	24H	34H	RFDL Configuration
05H	15H	25H	35H	RFDL Interrupt Status and Control
06H	16H	26H	36H	RFDL Status
07H	17H	27H	37H	RFDL Receive Data
08H	18H	28H	38H	Unused
09H	19H	29H	39H	XBOC Transmit Code
0AH	1AH	2AH	3AH	RBOC Enable
0BH	1BH	2BH	3BH	RBOC Interrupt Status and Received Code
0CH	1CH	2CH	3CH	Transceiver Interrupt Status
0DH	1DH	2DH	3DH	Transceiver Loopback
0EH	1EH	2EH	3EH	Transceiver Interrupt Enable
0FH	1FH			Unused
		2FH		Identification Register
			3FH	Master Interrupt Status

Transceiver Registers

Registers xCH
Transceiver Interrupt Status

Bit	Type	Function
Bit 7	R	0
Bit 6	R	0
Bit 5	R	0
Bit 4	R	0
Bit 3	R	TINT
Bit 2	R	RINT
Bit 1	R	BINT
Bit 0	R	0

A Transceiver Interrupt Register is provided for each of the four independent Facility Data Link Transceivers at read addresses 0CH, 1CH, 2CH, and 3CH.

The TINT bit is a logic 1 when the XFDL is producing an active interrupt. The TINT[x] chip output pin tracks the value of the TINT bit in this register.

The RINT bit is a logic 1 when the RFDL is producing an active interrupt. The RINT[x] chip output pin tracks the value of the RINT bit in this register.

The BINT bit is a logic 1 when the RBOC is producing an active interrupt. The INTB chip output pin tracks the inverted value of the BINT bit in this register if RBOC interrupts are enabled and no other interrupts occur.

Bits 0,4,5,6,7 are read as logic 0 to facilitate an indirect jump to an interrupt handling routine.

Register xDH:
Transceiver Loopback Register

Bit	Type	Function
Bit 7		Unused
Bit 6		Unused
Bit 5		Unused
Bit 4		Unused
Bit 3		Unused
Bit 2		Unused
Bit 1		Unused
Bit 0	R/W	LB

A Transceiver Loopback Register is provided for each of the four independent Facility Data Link Transceivers at read/write addresses 0DH, 1DH, 2DH, and 3DH.

When a logic 1 is written to the LB bit then OCLK is internally connected to ICLK and IDL is internally connected to ODL. This feature allows the external microprocessor to test most of the QFDL's internal circuitry without any special off chip wiring.

Register xEH:
Transceiver Interrupt Enable Register

Bit	Type	Function
Bit 7		Unused
Bit 6		Unused
Bit 5		Unused
Bit 4		Unused
Bit 3		Unused
Bit 2		Unused
Bit 1	R/W	TEN
Bit 0	R/W	REN

A Transceiver Interrupt Enable Register is provided for each of the four independent Facility Data Link Transceivers at read/write addresses 0EH, 1EH, 2EH, and 3EH.

When a logic 1 is written to the TEN bit then the TINT output is included in the OR function which produces the INTB output.

When a logic 1 is written to the REN bit then the RINT output is included in the OR function which produces the INTB output.

Register 2FH
Identification Register

Bit	Type	Function
Bit 7	R	0
Bit 6	R	0
Bit 5	R	0
Bit 4	R	0
Bit 3	R	0
Bit 2	R	0
Bit 1	R	0
Bit 0	R	0

The Identification Register is provided at read address 2FH.

The revision number of this chip can be obtained by reading this register.

Register 3FH
Master Interrupt Status Register

Bit	Type	Function
Bit 7	R	0
Bit 6	R	0
Bit 5	R	0
Bit 4	R	INT4
Bit 3	R	INT3
Bit 2	R	INT2
Bit 1	R	INT1
Bit 0	R	0

The Master Interrupt Status Register is provided at read address 3FH.

The INT[n] bit is a logic 1 when Transceiver 'n' is producing an interrupt. For each Transceiver there are three possible sources of interrupt. These interrupts are TINT, RINT, and RBOC interrupt.

Bits 0,5,6,7 are read as logic 0 to facilitate an indirect jump to an interrupt handling routine.

XFDL Registers

Register x0H: XFDL Configuration/Control

Bit	Type	Function
Bit 7		Unused
Bit 6		Unused
Bit 5		Unused
Bit 4	R/W	EOM
Bit 3	R/W	INTE
Bit 2	R/W	ABT
Bit 1	R/W	CRC
Bit 0	R/W	EN

A Configuration/Control Register is provided for each of the four independent facility data link transmitters at read/write addresses 00H, 10H, 20H, and 30H.

The enable (EN) bit controls the overall operation of the XFDL. When the EN bit is set to logic 1, the XDFL is enabled. Flag sequences are sent until data is written into the Transmit Data Register. When the EN bit is set to logic 0, the XFDL is disabled and the ODL output is forced to logic 0. The TINT output and the interrupt (INTR) bit (bit 1 of the Status Register) remain active while the XFDL is otherwise disabled.

The CRC enable (CRC) bit controls the generation of the CRC-CCITT frame check sequence. Setting this bit to logic 1 enables the CRC generator and appends the 16-bit frame check sequence (FCS) to the end of each message. When the CRC bit is set to logic 0, the FCS is not appended to each message. The MSB of the FCS word is transmitted first.

The abort (ABT) bit controls the sending of the seven consecutive ones HDLC abort code. Setting the ABT bit to logic 1 causes the transmission of the "11111110" code after the transmission of the byte in the Transmit Data Register. Abort characters are continuously sent until this bit is set to logic 0.

The interrupt enable (INTE) bit masks the TINT output. When the INTE bit is a logic 0, the TINT output is disabled; however, the INTR bit in the Status Register is always

enabled. Also, neither the INTR bit nor the TINT output are disabled when the XFDL is disabled.

The end of message (EOM) bit is a control bit. Setting the EOM bit to logic 1 indicates to the XFDL that the most recent byte of data written for transmission is the last byte of the present data frame. If the CRC bit has the value logic 1, then the 16-bit CRC word will be transmitted after the last data byte, followed by the continuous transmission of flags. The EOM bit is automatically set to logic 0 before the transmission of the next data frame.

NOTE : For proper operation, the EOM bit should only be set to logic 1 in response to a request by the XFDL for an additional byte of data as indicated by the TINT output going high or the INTR bit being set to logic 1.

Register x1H:
XFDL Status

Bit	Type	Function
Bit 7		Unused
Bit 6		Unused
Bit 5		Unused
Bit 4		Unused
Bit 3		Unused
Bit 2		Unused
Bit 1	R	INTR
Bit 0	R/W	UDR

A Status Register is provided for each of the four independent facility data link transmitters at read/write addresses 01H, 11H, 21H, and 31H.

The interrupt (INTR) bit is set to logic 1 when the byte in the Transmit Data Register has been loaded into the Parallel-to-Serial Convertor and a new byte can be written into the Transmit Data Register. This bit is an indication to transfer more data into the Transmit Data Register.

The underrun (UDR) bit is set to logic 1 if the parallel-to-serial conversion of the byte in the Convertor is completed before the next data byte is written into the Transmit Data Register. The UDR bit must be set to logic 0 to clear the underrun condition. After the UDR bit is set to logic 1, the next byte transmitted is an abort character, followed by a flag character in readiness to transmit the next valid data. If the UDR bit is still set to logic 1 after the transmission of the flag, the XFDL continuously transmits the idle pattern of all ones.

Register x2H: XFDL Transmit Data

Bit	Type	Function
Bit 7	R/W	TD[7]
Bit 6	R/W	TD[6]
Bit 5	R/W	TD[5]
Bit 4	R/W	TD[4]
Bit 3	R/W	TD[3]
Bit 2	R/W	TD[2]
Bit 1	R/W	TD[1]
Bit 0	R/W	TD[0]

A Transmit Data Register is provided for each of the four independent facility data link transmitters at write addresses 02H, 12H, 22H, and 32H.

Data written to this register is transferred to the Parallel-to-Serial Convertor and is transmitted over the facility data link. When the Convertor is emptied, the INTR bit in the Status Register is set to logic 1, and the TINT output goes high (unless the TINT output has been disabled by setting the INTE bit in the Configuration/Control Register to logic 0). The INTR bit in the Status Register is set to logic 0 and TINT output goes low immediately following the transfer of data into the Transmit Data Register. The TINT output follows the INTR bit in the Status Register when INTE is logic 1. The data from the Transmit Data Register is transmitted LSB first. After the TINT output goes high, data must be written into the Transmit Data Register within four data bit periods to prevent an underrun error. At an OCLK frequency of 4 kbit/s, this time is 1.5 ms.

RFDL Registers

Register x4H: RFDL Configuration

Bit	Type	Function
Bit 7		Unused
Bit 6		Unused
Bit 5		Unused
Bit 4		Unused
Bit 3		Unused
Bit 2		Unused
Bit 1	R/W	TR
Bit 0	R/W	EN

A Configuration Register is provided for each of the four independent facility data link receivers at read/write addresses 04H, 14H, 24H, and 34H.

The enable (EN) bit controls the overall operation of the RFDL. When set to logic 1, the RFDL is enabled; when EN is set to logic 0, the RFDL is disabled. When the RFDL is disabled, the FIFO buffer and all interrupts are cleared. The programming of the Interrupt Status/Control Register is not affected. When the RFDL is enabled, it will immediately begin looking for flags.

Setting the terminate reception (TR) bit to logic 1 forces the RFDL to immediately terminate the reception of the current data frame, empty the FIFO buffer, clear the interrupts, and begin searching for a new flag sequence. The RFDL handles a terminate reception event in the same manner as it would the toggling of the EN bit from logic 1 to logic 0 and back to logic 1. Thus, the RFDL state machine will begin searching for flags. An interrupt will be generated when the first flag is detected. The TR bit in the Configuration Register will reset itself to logic 0 after a rising and falling edge have occurred on the ICLK input once the write strobe (CBI[9]) goes high. If the Configuration Register is read after this time, the TR bit value returned will be logic 0.

Register x5H: RFDL Interrupt Status/Control

Bit	Type	Function
Bit 7		Unused
Bit 6		Unused
Bit 5		Unused
Bit 4		Unused
Bit 3		Unused
Bit 2	R/W	INTC[1]
Bit 1	R/W	INTC[0]
Bit 0	R	INTR

An Interrupt Status/Control Register is provided for each of the four independent facility data link receivers at read/write addresses 05H, 15H, 25H, and 35H.

Bits 2 and 1 (INTC[1:0]) of this register control the assertion of interrupts in the following way:

INTC[1]	INTC[0]	Description
0	0	Disable interrupts (All sources)
0	1	Enable interrupt when FIFO receives data
1	0	Enable interrupt when FIFO has 2 bytes of data
1	1	Enable interrupt when FIFO has 3 bytes of data

The interrupt (INTR) bit reflects the status of the RINT output unless the INTC[1:0] bits are set to disable interrupts. In that case, the RINT output is forced low and the INTR bit of this register will reflect the state of the internal interrupt latch.

The contents of the Interrupt Status/Control Register should only be changed when the RFDL is disabled. This prevents any erroneous interrupt generation.

Register x6H:
RFDL Status

Bit	Type	Function
Bit 7	R	FE
Bit 6	R	OVR
Bit 5	R	FLG
Bit 4	R	EOMR
Bit 3	R	CRC
Bit 2	R	NVB[2]
Bit 1	R	NVB[1]
Bit 0	R	NVB[0]

A Status Register is provided for each of the four independent facility data link receivers at read/write addresses 06H, 16H, 26H, and 36H.

Bits 2, 1 and 0 (NVB[2:0]) indicate the number of valid bits in the Data Register byte. It is possible that not all of the bits in the Data Register are valid when the last data byte is read. The data frame can be any number of bits in length and not necessarily an integral number of bytes. The Data Register is filled from the MSB to the LSB position. Between one and eight data bits are valid. The number of valid bits is equal to one plus the value of NVB[2:0]. An NVB[2:0] value of zero indicates that only the MSB in the register is valid. NVB[2:0] is only valid when EOMR is logic 1, FLG is logic 1 and OVR is logic 0.

The CRC bit has a value of logic 1 if a CRC error was detected in the last received data frame. The CRC bit is only valid when EOMR is logic 1, FLG is logic 1 and OVR is logic 0.

Note that the NVB[2:0] and CRC bits will be invalid when the Status Register is read for the status of the data byte written due to the interrupt on the detection of first flag, even though both the EOMR and FLG bits are logic 1.

The End of Message (EOMR) status bit follows the EOM output signal. It is set to logic 1 when:

1) The last byte in the data frame (EOM) is being read from the Data Register,

2) An abort sequence is detected while the link is not idle, and the byte written to the FIFO buffer due to the detection of the abort sequence is being read from the buffer,

3) The first flag has been detected and the dummy byte written into the FIFO buffer when the RFDL moved from idle to active status (see RFDL Operation section) is being read from the buffer, or

4) Immediately on detection of FIFO buffer overrun.

The EOMR bit is passed through the FIFO buffer with the data so that the status will correspond to the data just read from the buffer.

The flag (FLG) bit is set to logic 1 if the RFDL has detected the presence of the HDLC flag sequence (01111110) in the data. The FLG bit is reset to logic 0 when the HDLC abort sequence (01111111) is detected in the data, or when the RFDL is disabled. The FLG bit is also passed through the FIFO buffer with the data so that the status will correspond to the data just read from the buffer. The reception of bit-oriented codes (see ANSI T1.403-1989) over the data link will also force an abort due to the eight ones pattern.

The overrun (OVR) bit is set to logic 1 when data is written over unread data in the FIFO buffer. This bit is not reset to logic 0 until after the Status Register is read. While the OVR bit is logic 1, the RFDL and FIFO buffer are held in the reset state, causing the FLG and EOMR bits in the Status Register to be reset to logic 0.

The FIFO buffer empty (FE) bit is set to logic 1 when the last FIFO buffer entry is read. The FE bit goes to logic 0 when the buffer is loaded with new data.

If the Data Register is read while there is no valid data, then a FIFO buffer underrun condition occurs. The underrun condition is reflected in the Status Register by forcing all bits to logic 0 on the first Status Register read following the Data Register read which caused the underrun condition.

Register x7H:
RFDL Data

Bit	Type	Function
Bit 7	R	RD[7]
Bit 6	R	RD[6]
Bit 5	R	RD[5]
Bit 4	R	RD[4]
Bit 3	R	RD[3]
Bit 2	R	RD[2]
Bit 1	R	RD[1]
Bit 0	R	RD[0]

A Data Register is provided for each of the four independent facility data link receivers at read addresses 07H, 17H, 27H, and 37H.

RD[0] corresponds to the first bit of the serial byte received on the DATA input.

This register is actually a 4-level FIFO buffer. If data is available, the FE bit in the Status Register is logic 0. If INTC[1:0] in the Interrupt Control/Status Register is set to binary 01, the Data Register must be read within 31 data bit periods to prevent an overrun. If INTC[1:0] is set to binary 11, the Data Register must be read within 15 data bit periods.

When an overrun is detected, an interrupt is generated and the FIFO buffer is held in a cleared state until the Status Register is read. When the HDLC abort sequence (01111111) is detected in the data, an interrupt is generated and the data that has been shifted into the serial-to-parallel convertor is written into the FIFO buffer.

XBOC Registers

Register x9H: XBOC Code Register

Bit	Type	Function
Bit 7		Unused
Bit 6		Unused
Bit 5	R/W	BC[5]
Bit 4	R/W	BC[4]
Bit 3	R/W	BC[3]
Bit 2	R/W	BC[2]
Bit 1	R/W	BC[1]
Bit 0	R/W	BC[0]

A Code Register is provided for each of the four independent facility data link bit-oriented code transmitters at read/write addresses 09H, 19H, 29H, and 39H.

This register selects the 6-bit BOC to be transmitted.

RBOC Registers

Register xAH: RBOC Enable

Bit	Type	Function
Bit 7		Unused
Bit 6		Unused
Bit 5		Unused
Bit 4		Unused
Bit 3		Unused
Bit 2	R/W	IDLE
Bit 1	R/W	AVC
Bit 0	R/W	INTE

An Enable Register is provided for each of the four independent facility data link bit-oriented code receivers at read/write addresses 0AH, 1AH, 2AH, and 3AH.

The IDLE bit position enables or disables the generation of an interrupt when there is a transition from a validated BOC to idle code. A logic 1 in this bit position enables generation of an interrupt; a logic 0 in this bit position disables interrupt generation.

The AVC bit position selects the validation criterion used in determining a valid BOC. A logic 1 in the AVC bit position selects the alternative validation criterion of 4 out of 5 matching BOCs; a logic 0 selects the validation criterion of 8 out of 10 matching BOCs.

The INTE bit position enables or disables the generation of an interrupt when a valid BOC is detected. A logic 1 in this bit position enables generation of an interrupt; a logic 0 in this bit position disables interrupt generation.

Register xBH:
RBOC Interrupt Status

Bit	Type	Function
Bit 7	R	IDLEI
Bit 6	R	BOCI
Bit 5	R	BOC[5]
Bit 4	R	BOC[4]
Bit 3	R	BOC[3]
Bit 2	R	BOC[2]
Bit 1	R	BOC[1]
Bit 0	R	BOC[0]

An Interrupt Status Register is provided for each of the four independent facility data link bit-oriented code receivers at read/write addresses 0BH, 1BH, 2BH, and 3BH.

The IDLEI bit position indicates whether an interrupt was generated by the detection of the transition from a valid BOC to idle code. A logic 1 in the IDLEI bit position indicates that a transition from a valid BOC to idle code has generated an interrupt; a logic 0 in the IDLEI bit position indicates that no transition from a valid BOC to idle code has been detected. IDLEI is cleared to logic 0 when the register is read.

The BOCI bit position indicates whether an interrupt was generated by the detection of a valid BOC. A logic 1 in the BOCI bit position indicates that a validated BOC code has generated an interrupt; a logic 0 in the BOCI bit position indicates that no BOC has been detected. BOCI is cleared to logic 0 when the register is read.

The bit positions BOC[5:0] contain the 6-bit code values currently being output on the BOC[5:0] output bus.

TEST FEATURES DESCRIPTION

Test mode registers are used to apply test vectors during production testing of the QFDL. Test mode registers (as opposed to normal mode registers) are selected when TRSB is low.

Simultaneously asserting the CSB, RDB and WRB inputs causes all output pins and the data bus to be held in a high-impedance state.

Test Mode Register Memory Map (TRSB=0)

FDL1	FDL2	FDL3	FDL4	REGISTER DESCRIPTION
00H	10H	20H	30H	XFDL, Test Register 0
01H	11H	21H	31H	XFDL, Test Register 1
02H	12H	22H	32H	Unused
03H	13H	23H	33H	Unused
04H	14H	24H	34H	RFDL, Test Register 0
05H	15H	25H	35H	RFDL,Test Register 1
06H	16H	26H	36H	Unused
07H	17H	27H	37H	Unused
08H	18H	28H	38H	XBOC, Test Register 0
09H	19H	29H	39H	XBOC, Test Register 1
0AH	1AH	2AH	3AH	RBOC, Test Register 0
0BH	1BH	2BH	3BH	RBOC, Test Register 1
0CH	1CH	2CH	3CH	Unused
0DH	1DH	2DH	3DH	Unused
0EH	1EH	2EH	3EH	Unused
0FH	1FH	2FH		Unused
			3FH	Master Test Register

Master Test Register, 3FH:

Bit	Type	Function
Bit 7		Unused
Bit 6		Unused
Bit 5		Unused
Bit 4		Unused
Bit 3	W	DBCTRL
Bit 2	W	IOTST
Bit 1	W	HIZDATA
Bit 0	W	HIZIO

This register is used to select the QFDL test features. All bits are reset to logic 0 by a hardware reset of the QFDL.

The DBCTRL bit is used to pass control of the data bus drivers to the CSB pin in test mode only. When the DBCTRL bit is set to logic 1 and TSTB is low, the CSB pin controls the output enable for the data bus. While the DBCTRL bit is set, holding the CSB pin high causes the QFDL to drive the data bus and holding the CSB pin low tri-states the data bus. The DBCTRL bit overrides the HIZDATA bit. The DBCTRL bit is used to measure the drive capability of the data bus driver pads during production test.

The IOTST bit is used to allow an external microprocessor to force the QFDL into test mode, regardless of the state of the TSTB pin. When IOTST is a logic 1, all of XFDL, XBOC, RFDL, and RBOC are held in test mode. If all zeros are written into test register 1 of each of XFDL, XBOC, RFDL, and RBOC, then QFDL inputs can be observed by reading test register 0 and outputs controlled by writing to test register 0.

The HIZIO and HIZDATA bits control the tri-state modes of the QFDL. While the HIZIO bit is a logic 1, all output pins in the QFDL are held in a high-impedance state. The microprocessor interface is still active. While the HIZDATA bit is a logic 1, the data bus is also held in a high-impedance state which inhibits microprocessor read cycles.

Test Mode 0

In Test Mode 0, the QFDL allows the logic levels on the device inputs to be read through the microprocessor interface, and allows the device outputs to be forced to either logic level through the microprocessor interface.

Notes on Test Mode Register Bits:

1. Writing values into unused register bits has no effect. Reading unused bits can produce either a logic 1 or a logic 0; hence unused register bits should be masked off by software when read.

2. Writeable test mode register bits are not initialized upon reset unless otherwise noted.

To enable Test Mode 0, the TSTB input must be set low (the IOTST bit in the Test Mode Select Register may be set to logic 1 in lieu of the TSTB line being asserted) and the following addresses must be written with 00H: 01H, 11H, 21H, 31H, 05H, 15H, 25H, 35H, 09H, 19H, 29H, 39H, 0BH, 1BH, 2BH, 3BH.

Reading the following address locations returns the values for the indicated inputs :

FDL1	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00H							1	OCLK[1]
04H							IDL[1]	ICLK[1]
08H	OCLK[1]		1	1	1	1	1	1
0AH							IDL[1]	ICLK[1]

FDL2	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
10H							1	OCLK[2]
14H							IDL[2]	ICLK[2]
18H	OCLK[2]		1	1	1	1	1	1
1AH							IDL[2]	ICLK[2]

FDL3	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
20H							1	OCLK[3]
24H							IDL[3]	ICLK[3]
28H	OCLK[3]		1	1	1	1	1	1
2AH							IDL[3]	ICLK[3]

FDL4	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
30H							1	OCLK[4]
34H							IDL[4]	ICLK[4]
38H	OCLK[4]		1	1	1	1	1	1
3AH							IDL[4]	ICLK[4]

Writing the following address locations forces the outputs to the value in the corresponding bit position:

FDL1	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00H						UDR[1]	TINT[1]	
04H							EOM[1]	RINT[1]
08H								ODL[1]

FDL2	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
10H						UDR[2]	TINT[2]	
14H							EOM[2]	RINT[2]
18H								ODL[2]

FDL3	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
20H						UDR[3]	TINT[3]	
24H							EOM[3]	RINT[3]
28H								ODL[3]

FDL4	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
30H						UDR[4]	TINT[4]	
34H							EOM[4]	RINT[4]
38H								ODL[4]

OPERATION

Transmit

Upon reset of the system, the XFDL should be disabled by setting the EN bit in the Configuration/Control Register to logic 0. If data is not ready to be transmitted, the TINT output should also be masked by setting the INTE bit to logic 0.

When a frame or frames are ready to be transmitted, the Configuration/Control Register should be initialized for transmission: if the FCS is desired, the CRC bit should be set to logic 1; if the block is to be used in interrupt driven mode, interrupts should be enabled by setting the INTE bit to logic 1. Finally, the XFDL can be enabled by setting the EN bit to logic 1.

The XFDL can be used in a polled, interrupt driven, or DMA controlled mode for the transfer of frame data. In the polled mode, the TINT and UDR outputs of the XFDL are not used, and the processor controlling the XFDL must periodically read the Status Register to determine when to write to the Transmit Data Register. In the interrupt driven mode, the processor controlling the XFDL uses the TINT output to determine when to write to the Transmit Data Register. In the DMA controlled mode, the TINT output of the XFDL is used as a DMA request input to the DMA controller, and the UDR output is used as an interrupt to the processor to allow handling of exceptions.

If the XFDL data transfer is operating in the polled mode, then a timer periodically starts up a service routine, which should process data as follows:

1) Read Status Register and check UDR and INTR bits.

2) If UDR=1, then clear the Status Register, set the UDR bit in the Configuration/Control Register to logic 0, and restart the current frame.

3) If INTR=1, then:

    a) If there is still data to send, then write the next data byte to the Transmit Data Register;

    b) If all bytes in the frame have been sent, then set the EOM bit in the Configuration/Control Register to logic 1, and set the INTE bit to logic 0.

4) Read Status Register and check UDR bit.

5) If UDR=1, then clear the Status Register, set the UDR bit (and EOM, if set) in the Configuration/Control Register to logic 0, and restart the current frame.

In the case of interrupt driven data transfer, the TINT output of the XFDL is connected to the interrupt input of the processor, and the interrupt service routine should process the data exactly as shown above for the polled mode.

The XFDL can also be used with a DMA controller to process the frame data. In this case, the UDR output is connected to the processor interrupt input. The TINT output of the XFDL is connected to the DMA request input of the DMA controller. The DMA controller writes a data byte to the XFDL whenever the TINT output is high. If there is a problem during transmission and an underrun condition occurs, then the UDR output goes high and the processor is interrupted. The processor can then halt the DMA controller, clear the problem condition, reset the frame data pointers, and restart the DMA controller to resend the data frame.

Receive

On power up of the system, the RFDL should be disabled by setting the EN bit in the Configuration Register to logic 0. The Interrupt Status/Control Register should then be initialized to select the FIFO buffer fill level at which an interrupt will be generated.

After the Interrupt Status/Control Register has been written to, the RFDL can be enabled at any time by setting the EN bit in the Configuration Register to logic 1. When the RFDL is enabled, it will assume that the link status is idle (all ones) and immediately begin searching for flags. When the first flag is found, an interrupt will be generated (if enabled), and the byte received before the first flag was detected will be written into the FIFO buffer. Because the FLG and EOMR bits are passed through the buffer, this dummy write allows the Status Register to accurately reflect the current state of the data link. A Status Register read after a Data Register read of the dummy byte will return EOMR is logic 1 and FLG is logic 1. The first interrupt and data byte read after the RFDL is enabled (or TR bit set to logic 1) is an indication of the link status, and the data byte should therefore be discarded. It is up to the controlling processor to keep track of the link state as idle (all ones or bit-oriented messages active) or active (flags received).

The RFDL can be used in a polled, interrupt driven, or DMA controlled mode for the transfer of frame data. In the polled mode, the RINT and EOM outputs of the RFDL are not used, and the processor controlling the RFDL must periodically read the Status Register to determine when to read the Data Register. In the interrupt driven mode, the processor controlling the RFDL uses the RINT output to determine when to read the Data Register. In the DMA controlled mode, the RINT output of the RFDL is used as a DMA request input to the DMA controller, and the EOM output is used as an interrupt to the processor to allow handling of exceptions and as an indication of when to process a frame.

In the case of interrupt driven data transfer from the RFDL to the processor, the RINT output of the RFDL is connected to the interrupt input of the processor. The processor interrupt service routine should process the data in the following order:

1) Read Data Register.

2) Read Status Register to check for, in order, underrun, OVR, FLG, EOMR, and FE.

3) If underrun (Status Register returns 00), then discard last byte and wait for next interrupt.

4) If OVR=1, then discard last frame and wait for next interrupt.

5) If FLG=0 (abort) and the link state was active, then set the link state to inactive, discard the last frame, and wait for the next interrupt.

6) If FLG=1 and the link state was inactive, then set the link state to active, discard the last byte, and wait for the next interrupt.

7) Otherwise, save the last data byte read.

8) If EOMR=1, then check the CRC, NVB and process the frame.

9) If FE=0, then go to step 1, else wait for the next interrupt.

The interrupt service routine can optionally read the Status Register first to check for an overrun condition, and then for available data, before advancing to step one above.

The link state is typically a local software variable. The link state is inactive if the RFDL is receiving all ones or receiving bit-oriented codes which contain a sequence of eight ones. The link state is active if the RFDL is receiving flags or data.

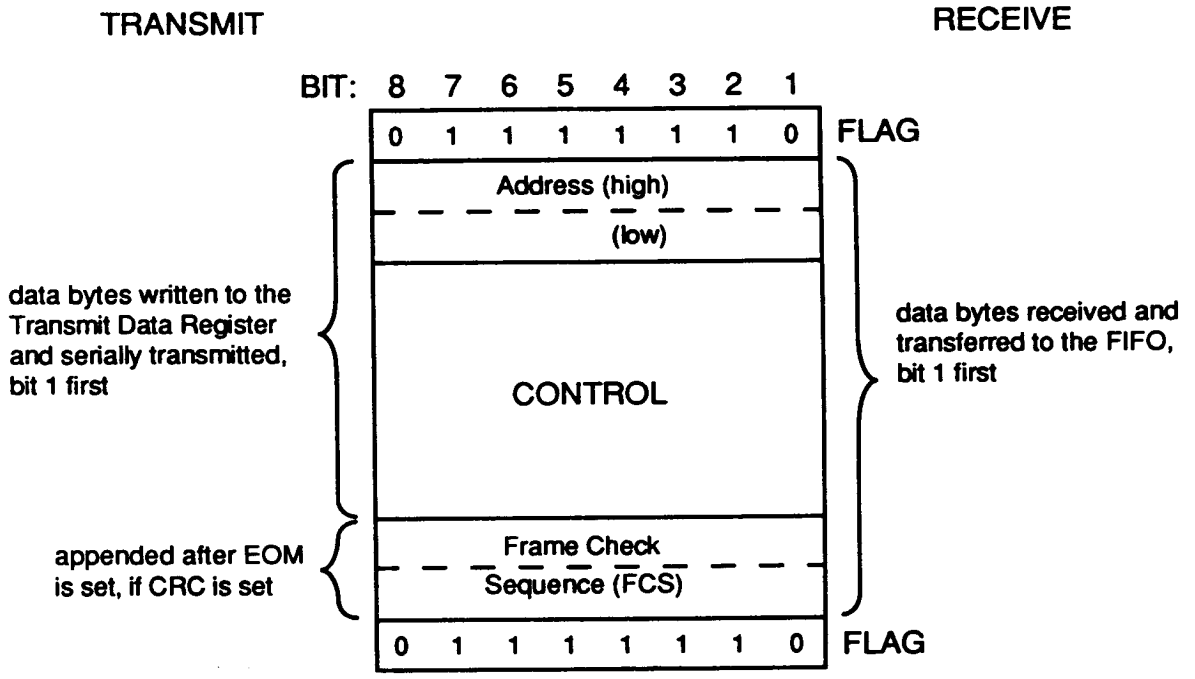
If the RFDL data transfer is operating in the polled mode, then processor operation is exactly as shown above for the interrupt driven mode, except that the entry to the service routine is from a timer, rather than an interrupt. In the polled mode, the option of reading the Status Register first should be used to avoid unnecessary reads of the Data Register.

The RFDL can also be used with a DMA controller to process the frame data. In this case, the EOM output is connected to the processor interrupt input. The RINT output of the RFDL is connected through a gate to the DMA request input of the DMA controller. The gate inhibits the DMA request if the EOM output is high. The DMA controller reads the data bytes from the RFDL whenever the RINT output is high. When the current byte read from the Data Register is the last byte in a frame (due to end-of-message or abort), or an overrun condition occurs, then the EOM output goes

high. The DMA controller is inhibited from reading any more bytes, and the processor is interrupted. The processor can then halt the DMA controller, read the Status Register, process the frame, and finally reset the DMA controller to process the data for the next frame.

FUNCTIONAL TIMING

Fig. 1 Typical Data Frame



Bit 1 is the first serial bit to be transmitted or received.

Both the address and control bytes must be supplied by an external processor and are shown for reference purposes only.

Key to Figures 2 & 3:

Flag	- flag sequence (01111110)
Abort	- abort sequence (01111111)
D1 - Dn	- n frame data bytes
R	- remainder bits (less than 8)
C1, C2	- CRC-CCITT information
B1, B2, B3	- groupings of 8 bits

Fig. 2 RFDL Normal Data and Abort Sequence

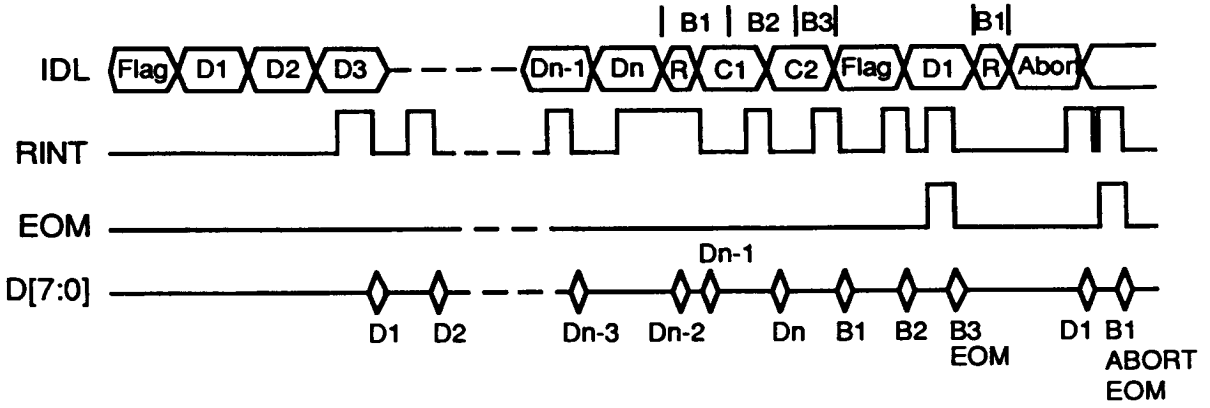


Figure 2 shows the relationship between RFDL inputs and outputs for the case where interrupts are programmed to occur when one byte is present in the FIFO buffer. The RFDL is assumed to be operating in the interrupt driven mode. Each read shown is composed of two register reads: first a read of the Data Register, followed by a read of the Status Register. A read of the Data Register sets the RINT output to low if no more data exists in the FIFO buffer. The status of the FE bit returned in the Status Register read will indicate the FIFO buffer fill status as well. The Data Register read Dn-2 is shown to occur after two bytes have been written into the buffer. The RINT output does not go low after the first Data Register read because a data byte still remains to be read. The RINT output goes low after Data Register read Dn-1. The FE bit will be logic 0 in Status Register read Dn-2 and logic 1 in Status Register read Dn-1.

The EOM output goes high as soon as the last byte in the frame is read from the Data Register. The RINT output will go low if the FIFO buffer is empty. The next Status Register read will return a value of logic 1 for the EOMR and FLG bits, and cause the EOM output of the RFDL to return low.

In the next frame, the first data byte is received, and after a delay of ten bit periods, it is written to the FIFO buffer, and read by the processor after the interrupt. When the

abort sequence is detected, the data received up to the abort is written to the FIFO buffer and an interrupt generated. The processor then reads the partial byte from the Data Register and the EOM output is set high. The processor then reads the Status Register which will return a value of logic 1 for the EOMR and FLG bits, and set the EOM output low. The FIFO buffer is not cleared when an abort is detected. All bytes received up to the abort are available to be read.

After an abort, the RFDL state machine will be in the receiving all ones state, and the data link status will be idle. When the first flag is detected, a new interrupt will be generated, with a dummy data byte loaded into the FIFO buffer, to indicate that the data link is now active.

Fig. 3 RFDL FIFO Overrun

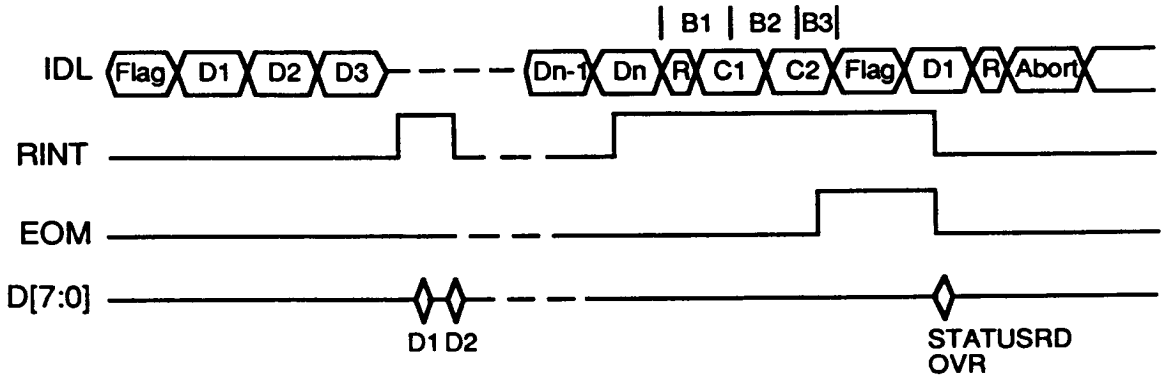


Figure 3 shows the relationship between RFDL inputs and outputs for the case where interrupts are programmed to occur when two data bytes are present in the FIFO buffer. Each read is composed of two register reads, as described above. In this example, data is not read by the end of B2. An overrun occurs since unread data (Dn-3) has been overwritten by B1. This sets the EOM output high, and resets both the RFDL and the FIFO buffer. The RFDL is held disabled until the Status Register is read. The start flag sequence is not detected since the RFDL is still held disabled when it occurs. Consequently, the RFDL will ignore the entire frame including the abort sequence (since it has not occurred in a valid frame or during flag reception, according to the RFDL).

Fig. 4 XFDL Normal Data Sequence

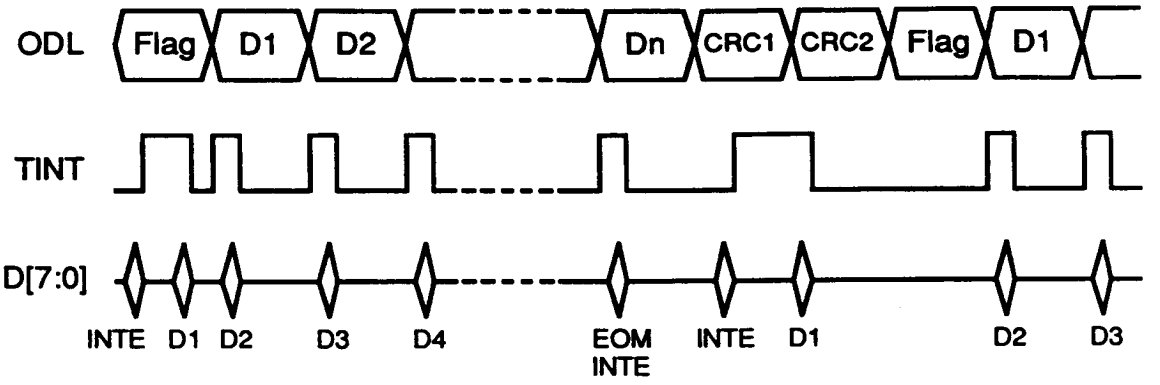


Figure 4 shows the relationship between XFDL inputs and outputs for the case where interrupts and CRC are enabled for regular data transmission. The process is started by setting the INTE bit in the Configuration/Control Register to logic 1, thus enabling the TINT signal. When TINT goes high, the interrupt service routine is started, which writes the first byte (D1) of the data frame to the Transmit Data Register. When this byte begins to be shifted out on the data link, TINT goes high. This restarts the interrupt service routine, and the next data byte (D2) is written to the Transmit Data Register. When D2 begins to be shifted out on the data link, TINT goes high again. This cycle continues until the last data byte (Dn) of the frame is written to the Transmit Data Register. When Dn begins to be shifted out on the data link, TINT again goes high. Since all the data has been sent, the interrupt service routine sets the EOM bit in the Configuration/Control Register to logic 1. The TINT interrupt should also be disabled at this time by setting the INTE bit to logic 0. The XFDL will then shift out the two-byte CRC word and closing flag, which ends the frame. Whenever new data is ready, the TINT signal can be re-enabled by setting the INTE bit in the Configuration/Control Register to logic 1, and the cycle starts again.

Fig. 5 XFDL Underrun Sequence

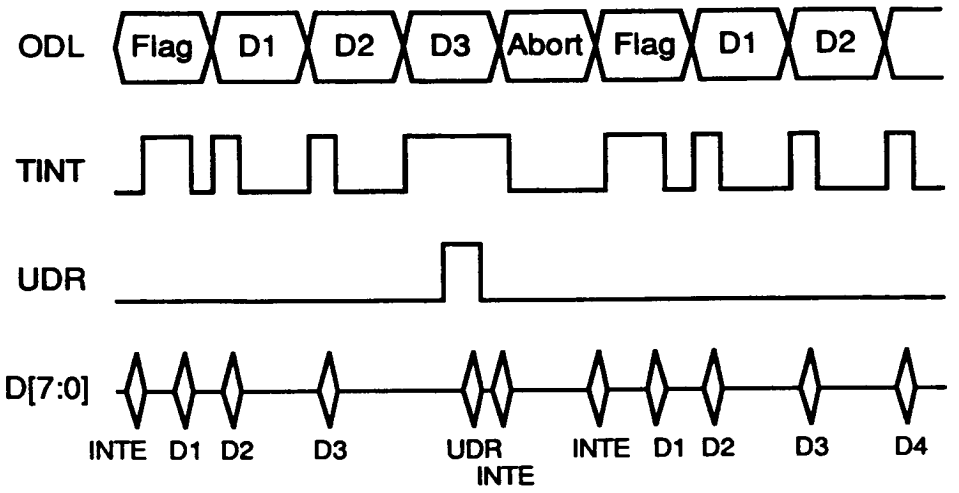


Figure 5 shows the relationship between XFDL inputs and outputs in the case of an underrun error. An underrun error occurs if the XFDL finishes transmitting the current message byte before the processor writes the next byte into the Transmit Data Register; that is, the processor fails to write data to the XFDL in time. In this example, data is not written to the XFDL within five rising clock edges after TINT goes high at the beginning of the transmission of byte D3. The UDR interrupt becomes active at this point, and an abort, followed by a flag, is sent out on the data link. Meanwhile, the processor must clear the UDR interrupt by setting the UDR bit in the Status Register to logic 0. The TINT interrupt should also be disabled at this time by setting the INTE bit in the Configuration/Control Register to logic 0. The data frame can then be restarted as usual, by setting the INTE bit logic to 1. Transmission of the frame then proceeds normally.

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on VDD with Respect to GND	-0.5V to +7.0V
Voltage on Any Pin	-0.5V to +7.0V
Output Current (all pins driving)	4 mA
Static Discharge Voltage	2000 V
Latch-Up Current (T_A = 0°C to +85°C)	400 mA

D.C. CHARACTERISTICS

(T_A = 0°C to +85°C, V_{DD} = 5 V ±10%)

Symbol	Parameter	Min	Max	Units	Conditions
V_{DD}	Power Supply	4.5	5.5	V	
V_{IL}	Input Low Voltage	-0.5	0.8	V	Guaranteed Input LOW Voltage
V_{IH}	Input High Voltage	2.0	V_{DD}	V	Guaranteed Input HIGH Voltage
V_{OL}	Output Low Voltage		0.4 0.4	V V	I_{OL}= 4 mA D[7:0], INTB I_{OL}= 2 mA all others
V_{OH}	Output High Voltage	2.4 2.4		V V	I_{OH}= -4 mA D[7:0] I_{OH}= -2 mA all others
I_{ILPU}	Input Low Current	-26	-110	µA	$V_{IL} \leq$ 1.65 V, Note 5
I_{IHPD}	Input High Current	48	110	µA	$V_{IH} \geq$ 3.85 V, Note 6
I_{IL}	Input Low Current	-10	0	µA	$V_{IL} \leq$ 1.65 V, Note 7
I_{IH}	Input High Current	-10	10	µA	$V_{IH} \geq$ 3.85 V, Note 7
V_T	Schmitt Trigger Voltage	2.3	2.8	V	RSTB input only
	Schmitt Trigger Hysteresis	0.5	1.2	V	RSTB input only
I_{DDOP}	Dynamic Current		11	mA / MHz	V_{DD} = 5.5 V, Outputs Unloaded, V_{IN} = 0.5 to 4.0 volts
I_{DDSB}	Static Current		1	mA	V_{DD} = 5.5 V, Outputs Unloaded

Notes on D.C. Characteristics:

1. All inputs and outputs are TTL-level compatible except the RSTB input which has a Schmitt trigger level translator.
2. Input voltage levels apply to all QFDL input pins and bidirectional pins.
3. Output voltage levels apply to all QFDL output pins and bidirectional pins.
4. Positive input current direction is into the device.
5. Inputs TSTB, TRSB, and RSTB have pull-ups. The negative sign indicates current flow out of the device.

6. Inputs DACK[4:1] and VCLK have pull-downs.
7. For inputs and bidirectionals without pull-ups.
8. The INTB output is open drain.
9. Additional supply current for TTL input levels:

   For V_{IN} = 2.0 volts, V_{DD} = 5.5 volts, T_A = 0°C

   Typical Process: I_{DD} = 3.7 mA per TTL input.
   Worst case: I_{DD} = 6.8 mA per TTL input.

   For V_{IN} = 0.8 volts, V_{DD} = 5.5 volts, T_A = 85°C

   Typical Process: I_{DD} = 0.33 mA per TTL input.
   Worst case: I_{DD} = 2.0 mA per TTL input.

CAPACITANCE

Symbol	Parameter	Min	Max	Unit	Conditions
CIN	Input Capacitance		10	pF	T_A = 25°C, f = 1 MHz (sampled only)
COUT	Output Capacitance		10	pF	T_A = 25°C, f = 1 MHz (sampled only)

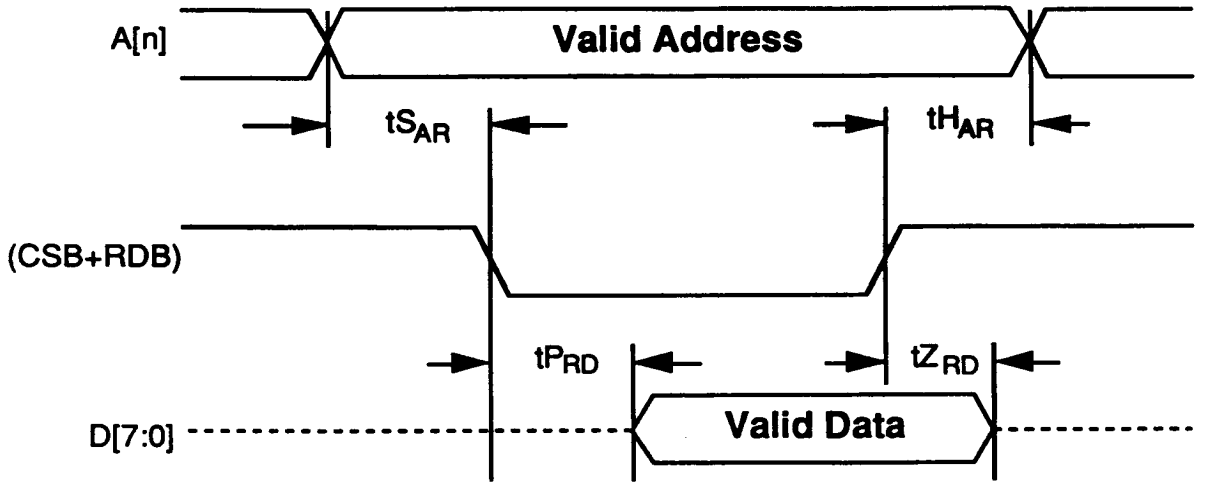
TIMING CHARACTERISTICS

(T_A = 0°C to +85°C, V_{DD} = 5 V ±10%)

Read Access (Fig. 6)

Symbol	Parameter	Min	Max	Units
tS_{AR}	Address to Valid Read Set-up Time	20		ns
tH_{AR}	Address to Valid Read Hold Time	20		ns
tP_{RD}	Valid Read to Valid Data Propagation Delay		100	ns
tZ_{RD}	Valid Read Deasserted to Output Tri-state		40	ns

Fig. 6 External Read Access Timing



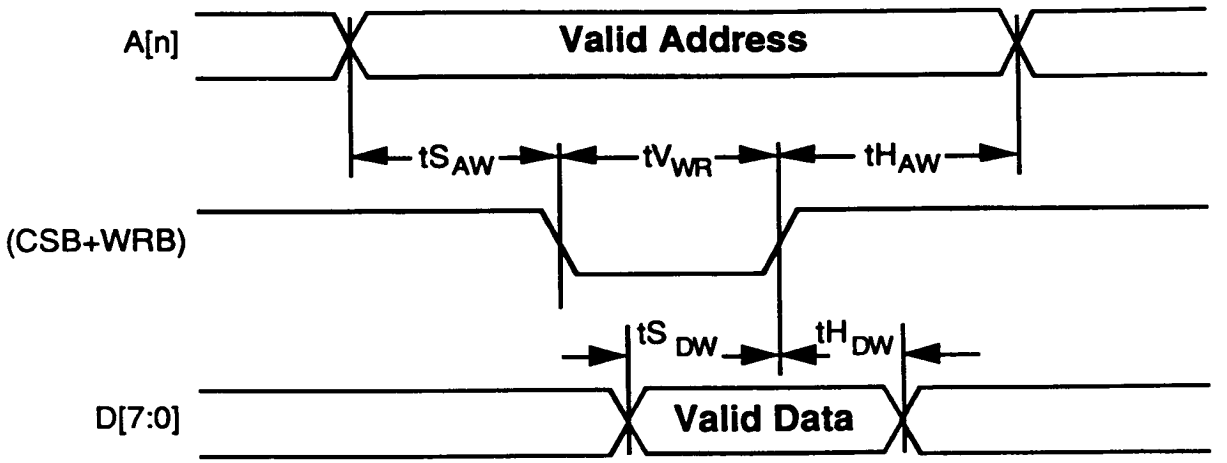
Notes on External Read Timing:

1. Output propagation delay time is the time in nanoseconds from TTL levels on the input signals (i.e., 0.8 and 2.0 volts) to the same TTL levels on the output signals.
2. Maximum output propagation delays are measured with a 50 pF load on the D[7:0] data bus.
3. A valid read cycle is defined as a logical OR of the CSB and the RDB signals.
4. Timing applies to normal mode register accesses only.

External Write Access (Fig. 7)

Symbol	Parameter	Min	Max	Units
tS_{AW}	Address to Valid Write Set-up Time	20		ns
tS_{DW}	Data to Valid Write Set-up Time	30		ns
tH_{DW}	Data to Valid Write Hold Time	40		ns
tH_{AW}	Address to Valid Write Hold Time	20		ns
tV_{WR}	Valid Write Pulse Width	40		ns

Fig. 7 External Write Access Timing



Notes on External Write Timing:

1. A valid write cycle is defined as a logical OR of the CSB and the WRB signals.
2. Timing applies to normal mode register accesses only.

QFDL TIMING CHARACTERISTICS

(T_A = 0°C to +85°C, V_{DD} = 5 V ±10%)

XFDL Timing Characteristics (Fig. 8, 9, 10)

Symbol	Description	Min	Max	Units
	OCLK Frequency (nominally 4 kHz)		2.1	MHz
	OCLK Duty Cycle (nominally 50%)	33	67	%
$tP1_{TINT}$	OCLK Low to TINT High Propagation Delay		60	ns
$tP2_{TINT}$	WRB Low to INT Low Propagation Delay		60	ns
$tP1_{TINTE}$	INTE Valid to TINT High Propagation Delay		60	ns
$tP2_{TINTE}$	INTE Valid to TINT Low Propagation Delay		60	ns
$tP1_{UDR}$	OCLK Low to UDR High Propagation Delay		70	ns
$tP2_{UDR}$	WRB High to UDR Low Propagation Delay		60	ns

Fig. 8 XFDL Interrupt Timing

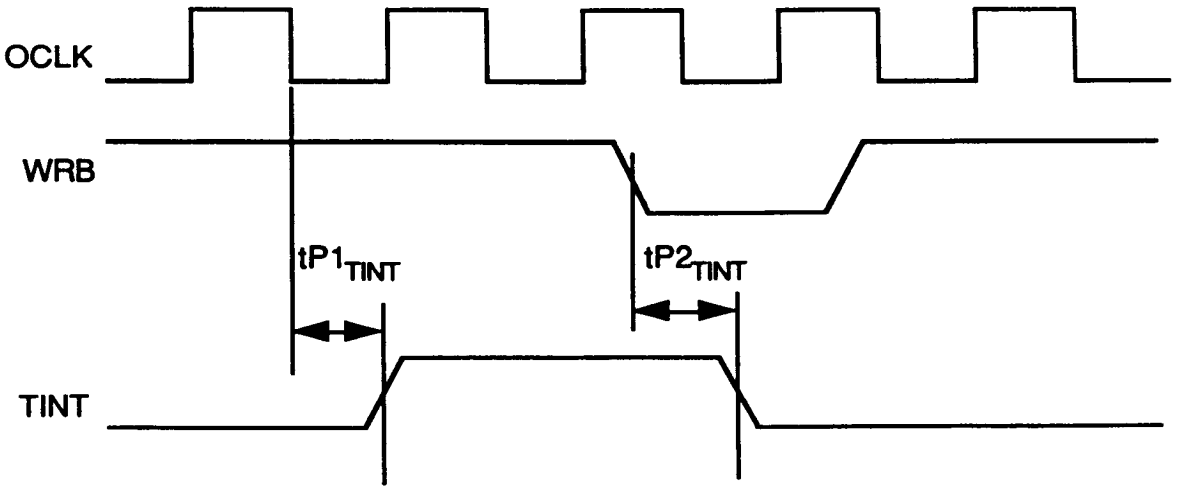


Fig. 9 XFDL Interrupt Timing (from INTE mask)

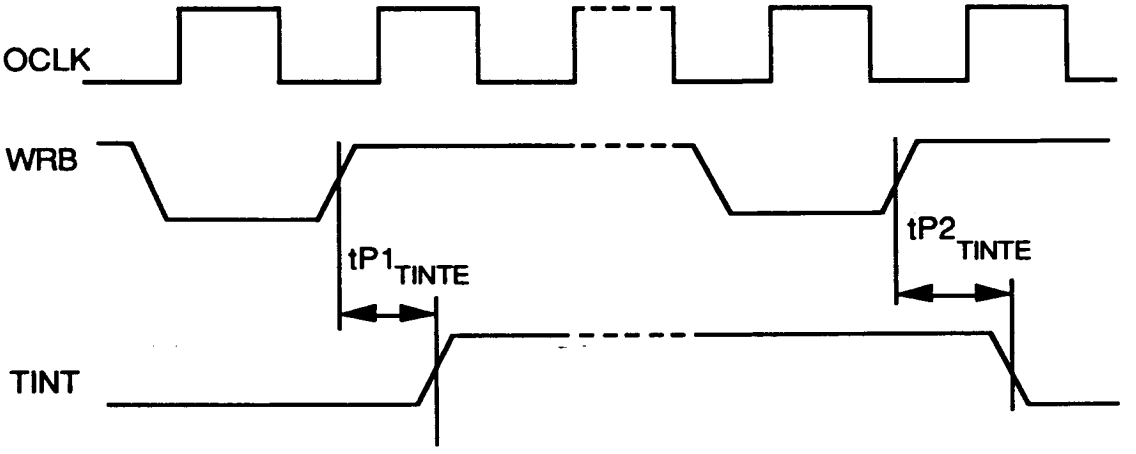
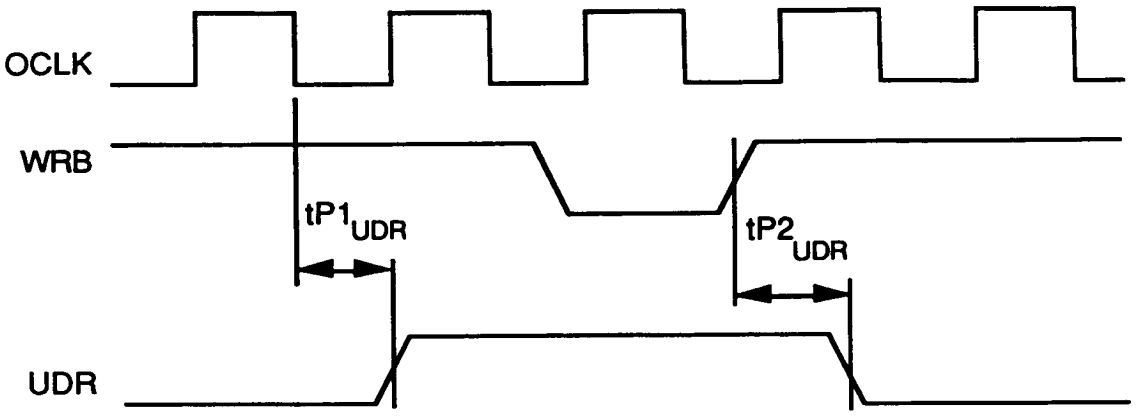


Fig. 10 XFDL Underrun Timing



RFDL Timing Characteristics (Fig. 11, 12, 13)

Symbol	Description	Min	Max	Units
	ICLK Frequency (nominally 4 kHz)		2.1	MHz
	ICLK Duty Cycle	33	67	%
tS_{IDL}	IDL Set-up time to ICLK	20		ns
tH_{IDL}	IDL Hold time to ICLK	20		ns
tP_{EOMH1}	ICLK Low to EOM High Propagation Delay		80	ns
tP_{EOMH2}	RDB Low to EOM High Propagation Delay		80	ns
tP_{RINTH}	ICLK Low to RINT High Propagation Delay		120	ns
tP_{RHEOML}	RDB High to EOM Low Propagation Delay		60	ns
tP_{RLEOML}	RDB Low to EOM Low Propagation Delay		75	ns
tP_{RINTL}	RDB Low to RINT Low Propagation Delay		75	ns

Fig. 11 RFDL Input Timing

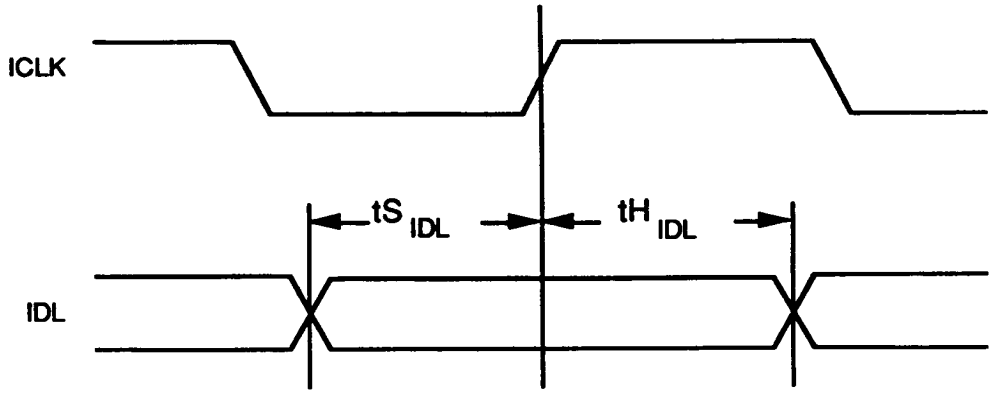


Fig. 12 RFDL Output Timing 1

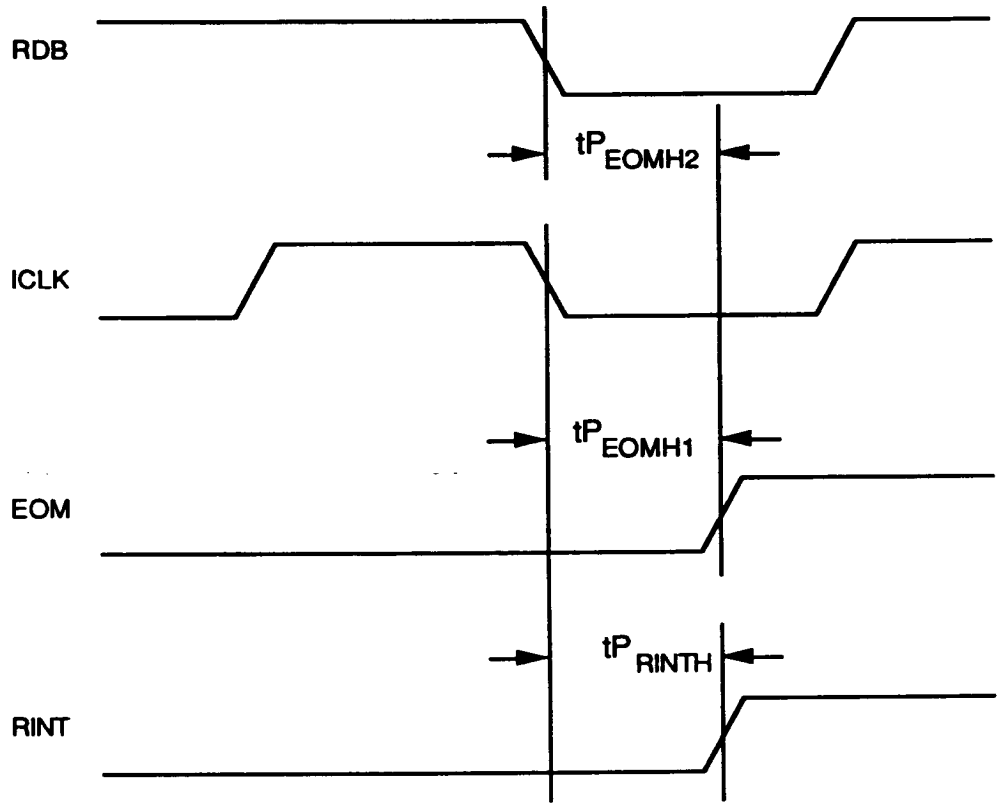
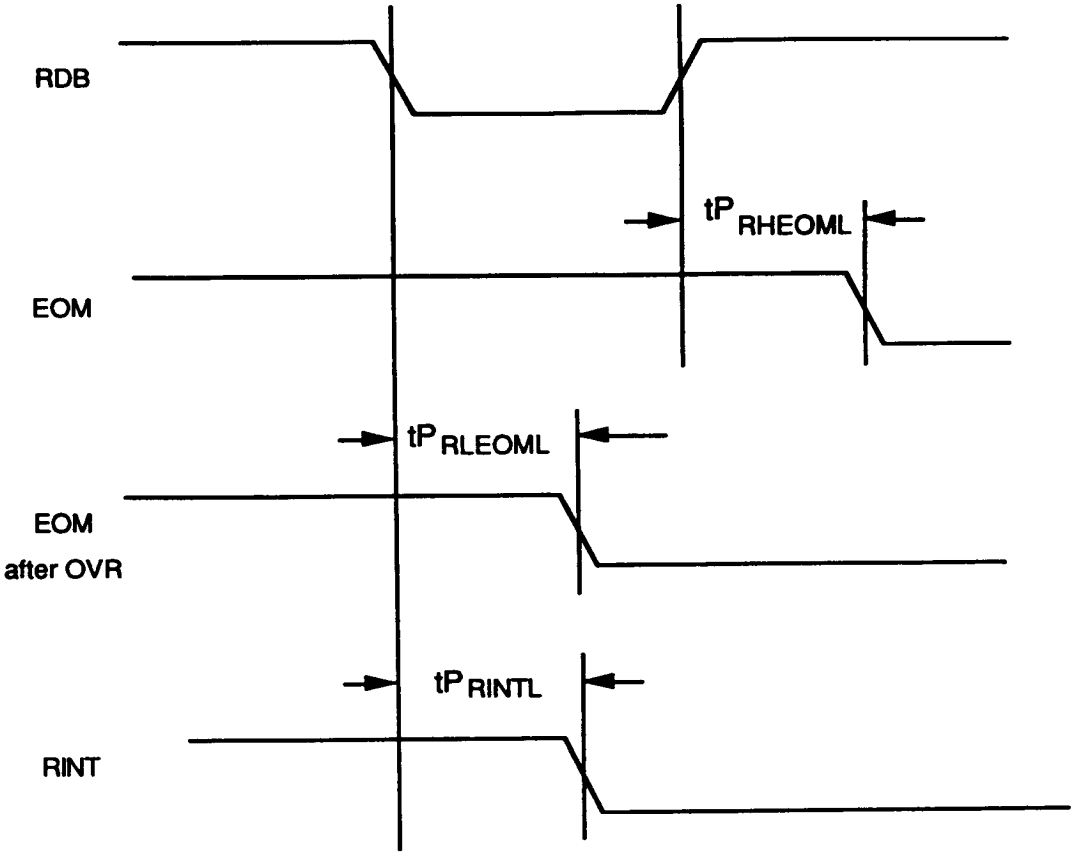


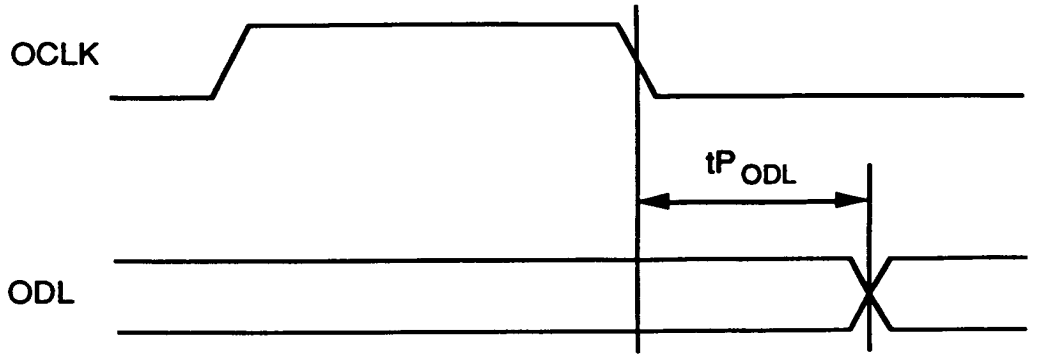
Fig. 13 RFDL Output Timing 2



XBOC Timing Characteristics (Fig. 14)

Symbol	Description	Min	Max	Units
	OCLK Frequency (nominally 4 kHz)	0	2.1	MHz
	OCLK Duty Cycle	33	67	%
tP_{ODL}	ODL Low to OCLK Valid Propagation Delay		70	ns

Fig. 14 XBOC Output Timing



RBOC Timing Characteristics (Fig. 15, 16)

Symbol	Description	Min	Max	Units
	ICLK Frequency (nominally 4 kHz)	0	2.1	MHz
	ICLK Duty Cycle	33	67	%
tS_{IDL}	IDL to ICLK Set-up	20		ns
tH_{IDL}	DATA to ICLK Hold	20		ns
tP_{RINTH}	Falling ICLK to RINT High Propagation Delay		80	ns

Fig. 15 RBOC Input Timing

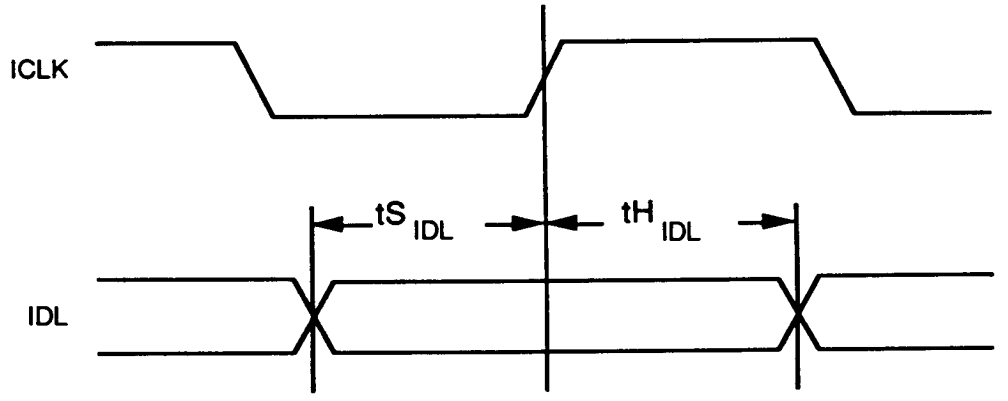
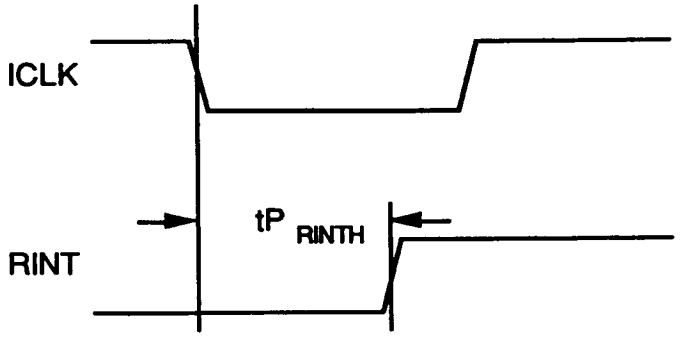


Fig. 16 RBOC Output Timing



Notes on Input Timing:

1. When a set-up time is specified between an input and a clock, the setup time is the time in nanoseconds from the TTL level input to the 2.0 Volt level of the clock.
2. When a hold time is specified between a clock and an input, the hold time is the time in nanoseconds from the 2.0 Volt level of the clock to the TTL level of the input.

Notes on Output Timing:

1. Output propagation delay time is the time in nanoseconds from TTL levels on the input signals (i.e., 0.8 and 2.0 Volts) to the same TTL levels on the output signals.
2. Maximum output propagation delays are measured with a 50 pF load on the outputs.

ORDER INFORMATION:

Description	Part Number	Package
T1 Quad Facility Data Link Interface	PM4374-QC	68 pin Plastic Leaded Chip Carrier (PLCC)

NOTES

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