FEATURES

- Integrates a SONET STS-12 compatible, duplex line interface circuit in a single compact module.
- Provides high speed clock recovery, serial-to-parallel conversion, processing of section level and line level overhead, byte interleaved demultiplexing, byte interleaved multiplexing, insertion of line level and section level overhead, high speed clock generation, and parallel-to-serial conversion.
- Supports an OC-12 compatible line interface when combined with a duplex electrical to optical converter device.
- Compact module that utilizes HDIC technology to integrate CMOS, ECL, GaAs. and discrete components in a single device.
- When used in conjunction with TSPP, will support both STS-12 and STS-12C (and STS3/3C) payload formats.
- 182-pin metalized flatpack package.
- 12 Watts typical power dissipation.

The receiver section

- Provides high speed clock recovery, frame synchronization, and serial-to-parallel conversion in the receiver.
- Descrambles received data and performs section and line level alarm and performance monitoring including loss of signal detection, loss of frame detection, alarm indication signal (AIS) detection, and accumulation of BIP-8 errors and far end block errors.
- Extracts and serializes section and line level order wire channels.
- Extracts and serializes user channel and automatic protection switching channel.
- Extracts and serializes section and line level data communication channels and allows optional termination of the section data communication channel using an on-board HDLC receiver.
- Performs byte interleaved demultiplexing to provide four byte-wide STS-3 data streams from a single STS-12 data stream.

The transmitter section

- Provides frame insertion, high speed clock generation, and parallel-to-serial conversion in the transmitter.
- Scrambles transmitted data after insertion of section and line level overhead including BIP-8 codes and alarm and status signals such as far end block error, far end receive failure, and alarm indication signal (AIS).
- Serially accepts and inserts user channel and automatic protection switching channel.
- Serially accepts and inserts section and line level data communication channels and allows optional sourcing of the section data communication channel using an on-board HDLC transmitter.
- Performs byte interleaved multiplexing to provide a single STS-12 data stream from four byte-wide STS-3 data streams.
- Testmode loopback to receiver section.

REFERENCES

- American National Standard for Telecommunications - Digital Hierarchy - Optical Interface Rates and Formats Specification, ANSI T1.105-1988.
- Bell Communications Research - SONET Transport Systems: Common Generic Criteria, TR-TSY-000253, Issue 1, September, 1989.

DESCRIPTION

The PM5712 SONET STS-12 Line Interface Module (SLIM-12) is an integrated subsystem that supports STS-12 compatible line level transmit and receive interfaces for a 622.08 Mbit/s duplex data stream on the network side and a byte parallel interface for the four constituent STS-3s on the equipment side. The module processes the bytes contained in the section and line overhead. The SLIM-12 is configured, controlled, and monitored using registers that are accessed via a generic microprocessor interface.

At the receive serial input, the module accepts a a single ended STS-12 signal from a number of industry standard optical interfaces, and utilizes a phase locked loop (PLL) to extract clock and data. Once frame synchronization is obtained on the incoming 622 MHz data stream, a serial to parallel conversion is performed prior to processing of section and line overhead bytes.

The section overhead processor confirms the frame synchronization of the serial-to-parallel converter and determines loss of frame and loss of signal states. Once frame synchronization are validated, the section orderwire, user channel, and data link from the section overhead data stream are extracted. These signals and their associated clocks are available at output pins of the SLIM-12 module. An on chip HDLC receiver monitors the receive data link outputs, and makes the data link payload available to a central CPU via a common CPU bus.

The receive line overhead processor extracts the receive line data link, the receive line order wire, and the receive line automatic protection switching signals. It also detects the line AIS and Far End Receive Failure signals. These signals and their associated clocks are available at output pins of the SLIM-12 module.

The final function in the receive direction is the demultiplexing of the STS-12 bytes into four streams of STS-3 bytes with data rates of 19.44 Mbytes/s and a frame pulse which indicates the first byte of the synchronous payload envelope.

To extract the constituent STS-1 payload data from each STS-3, an external payload processor, such as the PM5323 Triple STS-1 Payload Processor (TSPP) must be used.

At the transmit parallel input, the module accepts four byte-wide STS-3 streams with a rate of 19.44 Mbyte/s each, which it multiplexes into one byte-wide STS-12 stream, with a data rate of 77.76 Mbyte/s. A frame pulse is required to mark the first byte of the STS-12 payload envelope. This data and frame pulse could be provided by an external payload processor device such as the TSPP.

The byte wide STS-12 stream is fed into the transmit line overhead processor , which adds the transmit line data link, line order wire, far end receive failure indication, and automatic protection switching channel to the line overhead bit stream. Existing bytes which are allocated for the line overhead bit stream are overwritten with the new line overhead data, so that the output data rate is the same as its input rate. Overwriting of the line overhead stream can be disabled in four byte wide blocks, if desired. Data inputs and clock outputs for the order wire, automatic protection switching channel, and data link are accessible at pins of the SLIM-12 module.

The transmit section overhead processor adds the transmit section order wire, section user channel, and section data link. The line alarm indication signal (AIS) can also be inserted if desired. As with the line overhead, the section overhead data overwrites allocated bytes so that the output data rate is the same as the input rate. This overwriting can be disabled on a byte by byte basis if desired. Data inputs and clock outputs for the section order wire, data link, and user channel are accessible at pins of the SLIM-12 module. The input to the section data link can be switched from the external pins to an on chip HDLC transmitter, so that data destined for the data link can be written to the HDLC transmitter via the CPU interface.

The final function in the transmit direction is parallel-to-serial conversion. Data with a rate of 77.76 Mbyte/s is shifted out of the parallel-to-serial converter at 622.08 Mbit/s. The module contains a second PLL on the transmit side to synchronize outgoing data with a reference clock. The 622.08 MHz clock which drives the transmit functions is synchronized to a 19.44 MHz square wave at the REF input pin. The STS-12 serial data and associated 622.08 MHz clock exit the SLIM-12 module via differential ECL outputs designed to drive 50 Ω loads.

The SLIM-12 transmit output operates in conjunction with an external electrical to optical converter. For long haul applications, the optical transmitter would normally be a laser designed for single mode operation, which would convert the high/low ECL levels to on/off light pulses.

Suggested Optical Transmitters:

Company	Model Number	Max. Speed
AT&T	ASTROTEC 1218	1000 MB
Ortel	3510A	3000 MB
Ortel	3510B	6000 MB
BT&D	XMT 1300-1.2	1200 MB

The optical receiver module would be either a PIN diode, or an avalanche diode (depending on the application) with a low noise transconductance amplifier. The output of the amplifier would have an amplitude of between 0.6 and 2.0 Vpp, centred at -1.3V, and be designed to drive a 50Ω load. AGC would normally be required to keep the output within the operating range over the desired sensitivity range of the receiver. The Data Slicing Comparator in the SLIM-12 module has no hysteresis, so if hysteresis is desired to reduce noise, then data slicing comparators should be placed before the Receive Serial Data (RSD) input.

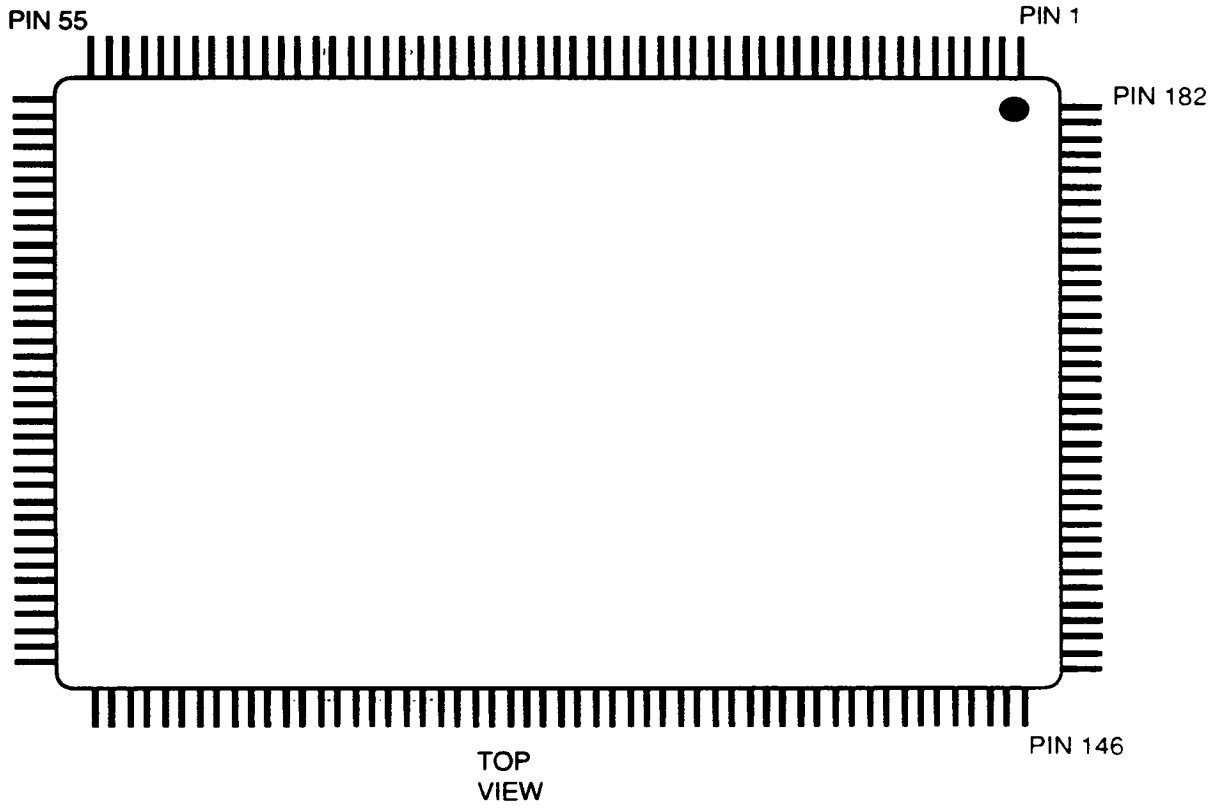
Suggested Optical Receivers:

Company	Model Number	Max. Speed
AT&T	ASTROTEC 1306A	1700 MB
Ortel	3510A	3000 MB
Ortel	3510B	6000 MB
BT&D	RCV1201-1.2	1200 MB

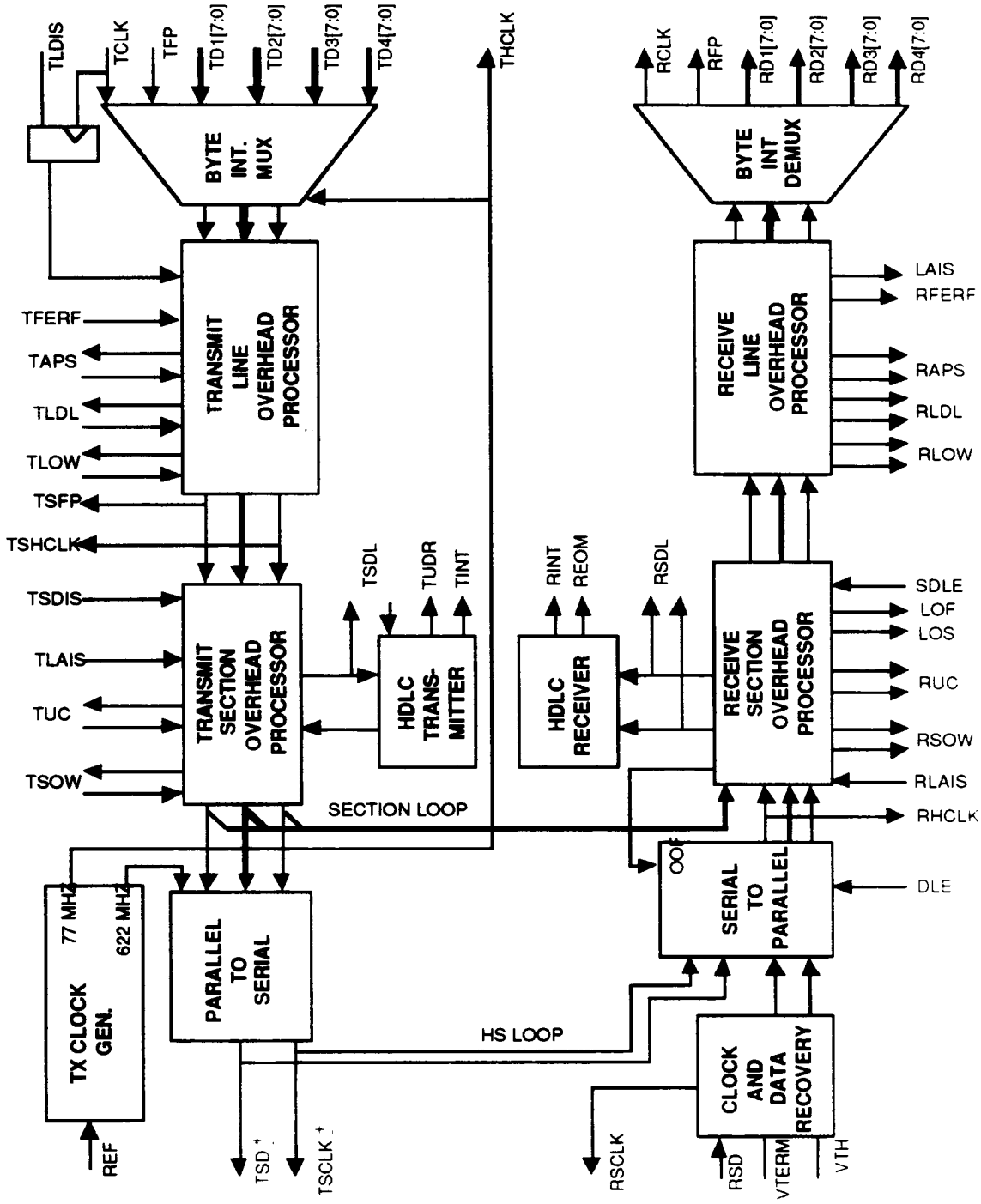
Both the transmit and receive circuitry have a high speed to low speed clock derivation structure. The clock outputs from the receive.side are derived from the recovered 622.08 MHz serial data clock, which is synchronized to the received STS-12 serial data. The clock outputs from the transmit side are derived from the 622 MHz transmit clock, which is synchronized to a 19.44 MHz reference. The STS-3 transmit clock inputs must be synchronous and should be stable in phase to the transmit clock outputs.

PIN DIAGRAM

The SLIM-12 is implemented with PMC's proprietary HDIC technology and is packaged in an 182 pin metalized kovar flatpack package, denoted by part number PM5712AU, shown below. Gull Wing lead forms and cavity down are standard Pin 1 is indicated by a dot on the top of the package. Pin numbering is counterclockwise when the package is viewed from the top with the dot indicator visible.



BLOCK DIAGRAM



PIN DESCRIPTION

Connector Name	Type	Pin No. Top Sink	Function
TD4[0] TD4[1] TD4[2] TD4[3] TD4[4] TD4[5] TD4[6] TD4[7]	CMOS Input	171 170 169 167 166 164 163 162	The transmit PCM data (TD4[7:0]) bus carries PCM data in byte serial format. TD4[7:0] carries the transmit PCM data of STS-1 #4, STS-1 #8, and STS-1 #12. TD4[7:0] is sampled on the rising edge of TCLK. TD4[7] is the most significant bit (corresponding to bit 1, the first bit transmitted of each serial PCM word). TD4[0] is the least significant bit (corresponding to bit 8, the last bit transmitted of each PCM word).
TD3[0] TD3[1] TD3[2] TD3[3] TD3[4] TD3[5] TD3[6] TD3[7]	CMOS Input	182 181 180 179 177 176 174 173	The transmit PCM data (TD3[7:0]) bus carries PCM data in byte serial format. TD3[7:0] carries the transmit PCM data of STS-1 #3, STS-1 #7, and STS-1 #11. TD3[7:0] is sampled on the rising edge of TCLK. TD3[7] is the most significant bit (corresponding to bit 1, the first bit transmitted of each serial PCM word). TD3[0] is the least significant bit (corresponding to bit 8, the last bit transmitted of each PCM word).
TD2[0] TD2[1] TD2[2] TD2[3] TD2[4] TD2[5] TD2[6] TD2[7]	CMOS Input	10 9 7 6 5 4 3 2	The transmit PCM data (TD2[7:0]) bus carries PCM data in byte serial format. TD2[7:0] carries the transmit PCM data of STS-1 #2, STS-1 #6, and STS-1 #10. TD2[7:0] is sampled on the rising edge of TCLK. TD2[7] is the most significant bit (corresponding to bit 1, the first bit transmitted of each serial PCM word). TD2[0] is the least significant bit (corresponding to bit 8, the last bit transmitted of each PCM word).
TD1[0] TD1[1] TD1[2] TD1[3] TD1[4] TD1[5] TD1[6] TD1[7]	CMOS Input	21 20 18 17 15 14 12 11	The transmit PCM data (TD1[7:0]) bus carries PCM data in byte serial format. TD1[7:0] carries the transmit PCM data of STS-1 #1, STS-1 #5, and STS-1 #9. TD1[7:0] is sampled on the rising edge of TCLK. TD1[7] is the most significant bit (corresponding to bit 1, the first bit transmitted of each serial PCM word). TD1[0] is the least significant bit (corresponding to bit 8, the last bit transmitted of each PCM word).

TSCLK+ TSCLK-	ECL Output	24 23	The transmit serial clock (TSCLK) balanced signals carry the clock signal generated for the TSD data stream by the SLIM-12 module. TSCLK is nominally a 622.08 MHz, 50% duty cycle clock.
TSD+ TSD-	ECL Output	27 26	The transmit serial data (TSD) balanced signals carry the 622.08 Mbit/s scrambled NRZ serial STS-12 data stream.
REF	TTL Input	29	Frequency reference input for the transmit clock generator. 19.44 MHz ±20 ppm, 50 ± 10% duty cycle.
TFP	CMOS Input	30	The transmit frame pulse (TFP) signal marks the transport frame alignment on the TD1, TD2, TD3, and TD4 byte serial busses. TFP is high to mark the first byte of the synchronous payload envelope of the first constituent STS-1 stream output on each of these busses. TFP is sampled on the rising edge of TCLK.
TCLK	CMOS Input	32	The transmit clock (TCLK) signal provides timing for processing the TD1, TD2, TD3, and TD4 byte serial busses. These busses are sampled on the rising edge of TCLK. TCLK is nominally a 19.44 MHz, 50% duty cycle clock.
TSHCLK	CMOS Output	33	The Transmit Section High Speed Clock (THSCLK) signal is a delayed version of THCLK, and provides timing for the transmit section overhead processor. TSDIS and TLAIS are sampled on the rising edge of TSHCLK.
TSFP	CMOS Output	34	The active high Transmit Section Frame Pulse (TSFP) is a delayed version of the Transmit Line Frame Pulse output, TFP. It is used to synchronise the Transmit Section Disable input , TSDIS. TSFP is high for one TSHCLK period each frame.
TSDLCLK	CMOS Output	35	The transmit section data link clock (TSDLCLK) signal is a 192 kHz clock for use by upstream circuitry that processes the section data communication channel. TSDLCLK is a gapped 216 kHz clock.

TSDL	CMOS Input	36	The transmit section data link (TSDL) signal carries the 192 kbit/s section data communication channel inserted into the STS-1 #1, D1-D3 section overhead bytes of the the STS-12 stream. TSDL is sampled on the rising edge of TSDLCLK.
TSOWCLK	CMOS Output	38	The transmit section order wire clock (TSOWCLK) signal is a 64 kHz clock for use by upstream circuitry that processes the section order wire channel. TSOWCLK is a gapped 72 kHz clock.
TSOW	CMOS Input	39	The transmit section order wire (TSOW) signal carries the 64 kbit/s section order wire channel inserted into the STS-1 #1 section overhead E1 byte of the STS-12 stream. TSOW is sampled on the rising edge of TSOWCLK. The byte boundaries on TSOW are identified by TFP.
TUCCLK	CMOS Output	40	The transmit section user channel clock (TUCCLK) signal is a 64 kHz clock for use by upstream circuitry that processes the section user channel. TUCCLK is a gapped 72 kHz clock.
TUC	CMOS Input	41	The transmit user channel (TUC) signal carries the 64 kbit/s section user channel inserted into the STS-1 #1 section overhead F1 byte of the STS-12 stream. TUC is sampled on the rising edge of TUCCLK. The byte boundaries on TUC are identified by TFP.
TLDLCLK	CMOS Output	42	The transmit line data link clock (TLDLCLK) signal is a 576 kHz clock for use by upstream circuitry that processes the line data communication channel. TLDLCLK is a gapped 2.16 MHz 67%(high)/33%(low) duty cycle clock.
TLDL	CMOS Input	44	The transmit line data link (TLDL) signal carries the 576 kbit/s line data communication channel inserted into the STS-1 #1, D4-D12 line overhead bytes of the the STS-12 stream. TLDL is sampled on the rising edge of TLDLCLK.
TFERF	CMOS Input	45	The active high Transmit Far End Receive Failure (TFERF) signal controls the insertion of the line Far End Receive Failure indication into the STS-12 overhead data. FERF is sampled on the rising edge of THCLK.

TLOWCLK	CMOS Output	46	The transmit line order wire clock (TLOWCLK) signal is a 64 kHz clock for use by upstream circuitry that processes the line order wire channel. TLOWCLK is a gapped 72 kHz clock.
TLOW	CMOS Input	47	The transmit line order wire (TLOW) signal carries the 64 kbit/s line order wire channel into the STS-1 line overhead E2 byte of the STS-12 stream. TLOW is sampled on the rising edge of TLOWCLK. The byte boundaries on TLOW are identified by TFP.
TAPSCLK	CMOS Output	48	The transmit automatic protection switch clock (TAPSCLK) signal is a 128 kHz clock for use by upstream circuitry that processes the line automatic protection switch channel. TAPSCLK is a gapped 144 kHz clock.
TAPS	CMOS Input	50	The transmit automatic protection switch (TAPS) signal carries the 128 kbit/s line automatic protection switch channel inserted into the STS-1 #1 line overhead K1 and K2 bytes of the STS-12 stream. TAPS is sampled on the rising edge of TAPSCLK. The byte boundaries on TAPS are identified by TFP.
TLAIS	CMOS Input	51	The active high transmit line alarm indication (TLAIS) signal controls the insertion of line AIS in the transmitted STS-12 stream. TLAIS is sampled on the rising edge of TSHCLK.
TSDIS	CMOS Input	52	The active high transmit section disable (TSDIS) signal selectively, on a byte by byte basis, disables overwriting the outgoing STS-12 stream with section overhead bytes. TSDIS is sampled on the rising edge of TSHCLK.
TLDIS	CMOS Input	53	The active high transmit line disable (TLDIS) signal selectively, on a byte by byte basis, disables overwriting the overhead bytes of all four of the incoming STS-3 streams. TLDIS is sampled on the rising edge of TCLK.

THCLK	ECL Test Point	54	The transmit high speed clock (THCLK) is a 77.76 MHz ECL level output which is used for production and diagnostic tests only. DO NOT TERMINATE THIS PIN, NOR CONNECT IT TO ANY INPUT.
LTE	Unused	56	Reserved for future loopback function.
SDLE	CMOS Input	57	The active high section diagnostic loopback enable (SDLE) signal controls the source of received data. When SDLE is high, the parallel transmit data is looped back to the receive side for diagnostic purposes just past the point where section overhead is inserted.
DLE	Unused	58	Reserved for future loopback function.
TUDR	CMOS Output	59	The active high Transmit HDLC Underrun (TUDR) signal is asserted when the data buffer of the transmit HDLC controller has underrun, and the current HDLC frame has been aborted.
TINT	CMOS Output	60	The active high Transmit HDLC Interrupt (TINT) signal is asserted when the transmit HDLC controller requests additional HDLC frame data.
REOM	CMOS Output	61	The active high Receive HDLC End of Message (REOM) signal is asserted when the last byte of an HDLC frame is read from the receive HDLC data register, or a FIFO overrun occurs in the HDLC receiver.
RINT	CMOS Output	62	The active high Receive HDLC Interrupt (RINT) signal is asserted when the receive HDLC controller detects a change in status of the receive section data communication channel.

LINTB	Open Drain	63	The interrupt (LINT) signal goes high when one of the various interrupting sources within the line overhead processor or byte interleaved multiplexor / demultiplexor circuits is active and enabled to generate interrupts.
SINT	TTL Output	64	The interrupt (SINT) signal goes high when one of the various interrupting sources within the section overhead processor or HDLC circuits is active and enabled to generate interrupts. The interrupt signals go low when the interrupt is acknowledged by reading a status register or masked by writing to an interrupt enable register.
D[0] D[1] D[2] D[3] D[4] D[5] D[6] D[7]	CMOS I/O	73 72 71 70 69 68 67 66	The bidirectional data bus (D[7:0]) is used during SLIM-12 register read and write accesses.
LCSB	CMOS Input	77	The active low Line Chip Select signal LCSB is low during register accesses of the SONET line overhead processor.
SCSB	CMOS Input	76	The active low Section Chip Select signal SCSB is low during register accesses of the SONET section overhead processor.
HSCSB	Unused	75	This pin is reserved for future mode selection of the high speed parallel-serial converter block.
RSTB	CMOS Input	78	The active low reset (RSTB) signal provides an asynchronous SLIM-12 reset. RSTB is a Schmitt triggered input with an integral pull up resistor.
WRB	CMOS Input	79	The active low write strobe (WRB) signal is low during a SLIM-12 register write access. The D[7:0] bus contents are clocked into the addressed register on the rising WRB edge while LCSB, SCSB, and HSCSB are low.

RDB	CMOS Input	80	The active low read enable (RDB) signal is low during a SLIM-12 register read access. The SLIM-12 drives the D[7:0] bus with the contents of the addressed register while RDB and LCSB, SCSB, and HSCSB are low.
TSTB	CMOS Input	81	Used only in production test to put the module into test mode.
TRSB	CMOS Input	83	The test register select (TRSB) signal discriminates between normal and test mode register accesses. TRSB is low during test mode register accesses, and is high during normal mode register accesses. This pad contains an internal pull up resistor.
A[0] A[1] A[2] A[3] A[4]	CMOS Input	88 87 86 85 84	The address bus (A[4:0]) selects specific registers during SLIM-12 register accesses.
LAIS	CMOS output	89	The line alarm indication Signal (LAIS) is high while Line AIS is detected in the STS-12 stream. LAIS is updated on the falling edge of RHCLK
RFERF	CMOS Output	90	The line Received Far End Receive Failure indication (RFERF) is high while a line Far End Receive Failure signal is detected in the incoming STS-12 stream. RFERF is updated on the falling edge of RHCLK.
RAPS	CMOS Output	91	The receive automatic protection switch (RAPS) signal carries the 128 kbit/s line automatic protection switch channel extracted from STS-1 #1 line overhead K1 and K2 bytes of the STS-12 stream. RAPS is updated on the falling edge of RAPSCLK. The byte boundaries RAPS signal are identified by RFP.
RAPSCLK	CMOS Output	93	The receive automatic protection switch clock (RAPSCLK) signal is a 128 kHz clock for use by downstream circuitry that processes the line automatic protection switch channel. RAPSCLK is a gapped 144 kHz clock.

RLOW	CMOS Output	94	The receive line order wire (RLOW) signal carries the 64 kbit/s line order wire channel extracted from STS-1 #1 line overhead E2 byte of the STS-12 stream. RLOW is updated on the falling edge of RLOWCLK. The byte boundaries on RLOW are identified by RFP.
RLOWCLK	CMOS Output	95	The receive line order wire clock (RLOWCLK) signal is a 64 kHz clock for use by downstream circuitry that processes the line order wire channel. RLOWCLK is a gapped 72 kHz clock.
RLDL	CMOS Output	96	The receive line data link (RLDL) signal carries the 576 kbit/s line data communication channel extracted from the STS-1 #1, D4-D12 line overhead bytes of the the STS-12 stream. RLDL is updated on the falling edge of RLDLCLK.
RLAIS	CMOS Input	97	The active high receive line alarm indication (RLAIS) signal controls the insertion of line AIS in the received STS-12 stream. RLAIS is sampled on the rising edge of RHCLK.
LOS	CMOS Output	98	The loss of signal (LOS) output is asserted when a loss of signal is declared. This occurs when a violating period (20 ± 3 µs) of consecutive all zeros patterns is detected in the incoming STS-12 stream. LOS is cleared when two valid framing words are detected and during the intervening time, no violating period of consecutive all zeros patterns is detected. LOS is updated on the falling edge of RHCLK.
LOF	CMOS Output	100	The loss of frame (LOF) output is asserted when a loss of frame is declared. This occurs when an out-of-frame condition persists for a period of 3 ms. LOF is cleared when an in-frame condition persists for a period of 3 ms. LOF is updated on the falling edge of RHCLK.
RLDLCLK	CMOS Output	101	The receive line data link clock (RLDLCLK) signal is a 576 kHz clock for use by downstream circuitry that processes the line data communication channel. RLDLCLK is a gapped 2.16 MHz 67%(high)/33%(low) duty cycle clock.

RUC	CMOS Output	102	The receive section user channel (RUC) signal carries the 64 kbit/s section user channel extracted from the STS-1 #1 section overhead F1 byte of the STS-12 stream. RUC is updated on the falling edge of RUCCLK. The byte boundaries on RUC are identified by RFP.
RUCCLK	CMOS Output	103	The receive section user channel clock (RUCCLK) signal is a 64 kHz clock for use by downstream circuitry that processes the section user channel. RUCCLK is a gapped 72 kHz clock.
RSOW	CMOS Output	105	The receive section order wire (RSOW) signal carries the 64 kbit/s section order wire channel extracted from the STS-1 #1 section overhead E1 byte of the STS-12 stream. RSOW is updated on the falling edge of RSOWCLK. The byte boundaries on RSOW are identified by RFP.
RSOWCLK	CMOS Output	106	The receive section order wire clock (RSOWCLK) signal is a 64 kHz clock for use by downstream circuitry that processes the section order wire channel. RSOWCLK is a gapped 72 kHz clock.
RSDL	CMOS Output	107	The receive section data link (RSDL) signal carries the 192 kbit/s section data communication channel extracted from the STS-1 #1, D1-D3 section overhead bytes of the the STS-12 stream. RSDL is updated on the falling edge of RSDLCLK.
RSDLCLK	CMOS Output	108	The receive section data link clock (RSDLCLK) signal is a 192 kHz clock for use by downstream circuitry that processes the section data communication channel. RSDLCLK is a gapped 216 kHz clock.
RHCLK	TTL Output	109	The receive high speed clock (RHCLK) signal provides timing for processing the internal receive high speed byte serial busses. RHCLK is nominally a 77.76 MHz, 50% duty cycle clock, and is internally generated by dividing down the recovered clock, RSCLK. RLAIS is sampled on the rising edge of RHCLK.

RCLK	CMOS Output	111	The receive clock (RCLK) signal provides timing for processing the RD1, RD2, RD3, and RD4 byte serial busses. These busses are updated on the falling edge of RCLK. RCLK is nominally a 19.44 MHz, 50% duty cycle clock, and is generated by dividing RHCLK.
RFP	CMOS Output	112	The receive frame pulse (RFP) signal marks the transport frame alignment on the RD1, RD2, RD3, and RD4 byte serial busses. RFP is high to mark the first byte of the synchronous payload envelope of the first constituent STS-1 stream output on each of these busses. RFP is updated on the falling edge of RCLK.
RD1[0] RD1[1] RD1[2] RD1[3] RD1[4] RD1[5] RD1[6] RD1[7]	CMOS Output	113 114 115 117 118 120 121 123	The receive PCM data (RD1[7:0]) bus carries PCM data in byte serial format. RD1[7:0] carries the receive PCM data of STS-1 #1, STS-1 #5, and STS-1 #9. RD1[7:0] is updated on the falling edge of RCLK. RD1[7] is the most significant bit (corresponding to bit 1, the first bit transmitted of each serial PCM word). RD1[0] is the least significant bit (corresponding to bit 8, the last bit transmitted of each PCM word).
RD2[0] RD2[1] RD2[2] RD2[3] RD2[4] RD2[5] RD2[6] RD2[7]	CMOS Output	124 126 127 129 130 131 132 134	The receive PCM data (RD2[7:0]) bus carries PCM data in byte serial format. RD2[7:0] carries the receive PCM data of STS-1 #2, STS-1 #6, and STS-1 #10. RD2[7:0] is updated on the falling edge of RCLK. RD2[7] is the most significant bit (corresponding to bit 1, the first bit transmitted of each serial PCM word). RD2[0] is the least significant bit (corresponding to bit 8, the last bit transmitted of each PCM word).
RD3[0] RD3[1] RD3[2] RD3[3] RD3[4] RD3[5] RD3[6] RD3[7]	CMOS Output	135 136 137 138 140 141 142 143	The receive PCM data (RD3[7:0]) bus carries PCM data in byte serial format. RD3[7:0] carries the receive PCM data of STS-1 #3, STS-1 #7, and STS-1 #11. RD3[7:0] is updated on the falling edge of RCLK. RD3[7] is the most significant bit (corresponding to bit 1, the first bit transmitted of each serial PCM word). RD3[0] is the least significant bit (corresponding to bit 8, the last bit transmitted of each PCM word).

RD4[0] RD4[1] RD4[2] RD4[3] RD4[4] RD4[5] RD4[6] RD4[7]	CMOS Output	144 145 147 148 150 151 153 154	The receive PCM data (RD4[7:0]) bus carries PCM data in byte serial format. RD4[7:0] carries the receive PCM data of STS-1 #4, STS-1 #8, and STS-1 #12. RD4[7:0] is updated on the falling edge of RCLK. RD4[7] is the most significant bit (corresponding to bit 1, the first bit transmitted of each serial PCM word). RD4[0] is the least significant bit (corresponding to bit 8, the last bit transmitted of each PCM word).
RSD	Analog or ECL input	156	The receive serial data (RSD) is the 50 Ω, unbalanced input for the 622.08 Mbit/s. scrambled NRZ serial STS-12 data stream.
VTERM	Analog	157	Terminating voltage for the RSD input signal terminating resistor. If RSD is dc coupled to an ECL output, then VTERM should be connected a to -2V supply with good ac coupling to the driver's ground. If RDSC is ac coupled to the output of a transconductance amplifier, then VTERM should be connected to VTH.
VTH	Analog	158	Threshold voltage for the data slicers. Nominally -1.3 V, it can be adjusted within a ± 0.2 V range if desired. VTH has an internal resistance of 1kΩ.If RDSC is ac coupled to its source, then VTH should be connected to VTERM.
RSCLK+	ECL Output	160	The recovered serial clock (RSCLK) signal carries the clock signal recovered from the RSD data stream by the SLIM-12 module. RSCLK is nominally a 622.08 MHz, 50% duty cycle clock.
VCCR	Power	149	+5V dc supply to the high speed receiver clock and data generator.
VCCT	Power	16	+5V dc supply to the transmit high speed clock generator.

VEER	Power	161	-5.2 V dc supply to the high speed receive clock and data generator.
VEET	Power	175 168	-5.2 V dc supply to the high speed transmit clock generator.
VDD	Power	128 116 104 92 74 55	+5V supply for the ECL-CMOS translators, section overhead transceiver, and line overhead transceiver and STS-12 to STS-3 muldems.
GND	Power	146 133 122 110 99 82 65 28 25 13 1 178 172 165 159 155 152	0V supply return for the STS-12 parallel-serial converter, ECL-CMOS translators, section overhead transceiver, line overhead transceiver, and STS-3 to STS-12 muldems.

VTT	Power	125 119 49 22	-2V for the internal high speed ECL pull down resistors.
VEE	Power	139 43 37 31 19 8	-5.2V For the STS-12 parallel-to-serial converter. and the ECL-CMOS translators.

Notes on Pin Description:

1. All SLIM-12 CMOS inputs and bidirectionals operate at CMOS logic levels
2. All SLIM-12 CMOS outputs and bidirectionals have 2 mA drive capability, except the SINT, LINT, and HSINT outputs and the D[7:0] bidirectionals which have 4 mA drive capability.
3. All SLIM-12 TTL inputs have 74F logic level and loading characteristics.
4. All SLIM-12 ECL inputs and outputs are compatible with 100K ECL

FUNCTIONAL DESCRIPTION

Clock and Data Recovery

The Clock and Data Recovery is implemented with a GaAs Phase Locked Loop integrated circuit which accepts an ECL compatible input signal, and produces ECL clock and data outputs to be used by the serial to parallel converter.

The receive signal at the RSD input is a serial non return to zero data stream with a peak to peak amplitude at least 0.6 V and at most 2.0 V which is centred at 1.3 V. RSD is a 50 Ω unbalanced input, terminated to the VTERM pin. If RSD is A.C. coupled to its source, then its termination point VTERM should be connected to the slicing threshold voltage VTH. If RSD is an ECL input, then VTERM should be connected to -2V. A comparator slices the data into logic levels.with respect to the voltage at VTH.

The receive clock recovery circuit is a PLL which synchronizes the 622.08 MHz output of a VCO to the incoming data stream by comparing the rising transitions of the VCO output with those of the incoming NRZ data. The greater the number of transitions in the data, the greater the stability of the recovered clock. The falling edge of the recovered clock strobes a data sampling flip-flop which regenerates the data at ECL levels for use by the down stream serial-to-parallel converter. The RSCLK output caries an unbalanced ECL version of the 622.08 MHz recovered clock to the outside world.

The jitter transfer function of the PLL attenuates jitter at 6 dB per octave for jitter frequencies above approxamately300 kHz. Jitter tolerance is greater than 0.2 UIpp for jitter frequencies above 250 kHz, 2 UIpp from 250 kHz to 25 kHz, and 20 UIpp below 2.5 kHz.

Serial-To-Parallel Conversion

The outputs of the Clock and Data Recovery circuit drives the ECL compatible inputs of the Serial-to-Parallel Converter. This converter searches for the A1 and A2 bytes in the STS-12 frame pattern. Three valid A1 bytes followed by three valid A2 bytes synchronize the byte-wide parallel output to the byte boundaries of the serial input signal. The framer searches for the last three of the 12 A1, and the first three of the 12 A2 bytes.

Once the STS-12 frame has been found, the frame search process halts, and the parallel output data continues to be partitioned according to the initially found frame position. Should the frame verification circuit in the down stream Receive Section Overhead Processor determine that the frame synchronization is incorrect, it reactivates the frame search process.

There are three outputs from the serial-to-parallel converter. The byte-wide data bus with a data rate of 77.76 Mbyte/s, the 77.76 MHz byte clock generated from the 622.08 MHz recovered clock, and the 8 kHz frame pulse indicating the transition from A1 bytes to A2 bytes in the STS-12 frame pattern are all transferred to the down stream section overhead processor. These signals are CMOS compatible in order to drive the Receive Section Overhead Processor.

Receive Section Overhead Processing

The Receive Section Overhead Processor (RSOP) is implemented using the PM5301 SONET Section Transceiver (SSTX) integrated circuit. The Section Overhead Processor descrambles the received data and extracts the data link channel, order wire channel, and user channel from the section overhead. The SSTX also contains a Byte Interleaved Parity (BIP-8) detector, and a microprocessor peripheral used to receive LAPD/HDLC frames from the section overhead data link. All configuring of the SSTX and monitoring of its alarms are performed via the SLIM-12 microprocessor bus.

The SSTX is is configured to process an STS-12 data stream that is presented in byte serial format at 77.76 Mbytes/s. Receive Section Overhead Processor descrambles the received data and extracts the data link channel, order wire channel and user channel from the section overhead, and provides them as lower rate bit serial outputs (RDL, ROW, RUC) together with associated clock signals (RDLCLK, ROWCLK, RUCCLK). The complete descrambled SONET data stream is then passed to the Receive Line Terminating Receiver in byte serial format. Line alarm indication signal may be inserted into this descrambled byte serial data stream by setting the RLAIS input high.

The Receive Section Overhead Processor verifies that the frame pulse provided by the upstream frame pattern detector in the serial-to-parallel converter by watching for the frame pattern to recur at the same position in the frame. It generates an out-of-frame signal (OOF) which causes the frame recovery process in the serial-to-parallel converter to engage if the frame pattern does not recur. Loss of frame (LOF), and loss of signal (LOS) outputs are provided at pins on the module. LOF is high after a 3 ms period without a valid frame pulse. LOS is high after a 20 ± 2.5 µs period of all zeros data at the input. LOS and LOF return low after a frame pattern has been detected and verified.

Microprocessor accessible registers hold the states of the OOF, LOF, or LOS alarms and count section level bit-interleaved parity (BIP-8) errors. BIP-8 accumulators are large enough to be read as infrequently as once per second. The section overhead interrupt, SINT may be activated by state transitions on the OOF, LOF, or LOS outputs, or by a single BIP-8 error event, depending on which is unmasked. Each interrupt source is individually maskable, and is cleared by reading the interrupting register.

The Receive Section Overhead Processor provides descrambled data, along with appropriate clock and frame alignment indication signals for use by downstream circuitry that processes the SONET line overhead, synchronous payload envelope.

Receive Section HDLC Receiver

The Section HDLC receiver is connected to the receive section data communications channel. The HDLC receiver is a microprocessor peripheral used to receive LAPD/HDLC frames.

The HDLC receiver detects the change from flag characters to the first data frame byte, removes stuffed zeros on the incoming data stream, receives frame data, and calculates the CRC-CCITT frame check sequence.

Received data is placed into a 4-level FIFO buffer. A status register contains the Overrun, End of Message, Flag, and Data Available flags.

On End of Message, the status register also indicates the FCS status and the number of valid bits in the final byte. An interrupt (RINT) may be generated when 1, 2, or 3 (programmable count) bytes are stored in the FIFO. An interrupt may also be generated when the terminating flag sequence, abort sequence, or FIFO overrun are detected.

An external DMA controller may be used to transfer packets from the HDLC Receiver to external memory.

Receive Line Overhead Processing

The Receive Line Overhead Processing function is performed by the PM5311 SONET Line Transceiver integrated circuit (RLOP). All performance monitoring information, alarm states, and option controls are accessible via the SLIM-12 microprocessor bus. Note that after a reset, the SLTX is not optioned for STS-12 operation. **03H must be written to register 00H of the SLTX to set it for STS-12.**

The Receive Line Overhead Processor comprises the following seven functional blocks:

1. Timing Block: interfaces the data inputs with the other blocks of the RLOP.

2. FERF Detect Block: detects the presence of Line Far End Receive Failure in the STS-12 stream.

3. Line AIS Block: detects the presence of a Line Alarm Indication Signal (AIS) in the STS-12 stream.

4. APS Extract Block: extracts the Automatic Protection Switch Channel.

5. Data Link Extract Block: extracts the line data communications channel.

6. Order Wire Extract Block: extracts the line order wire channel.

7 The Error Monitor Block calculates the received line BIP-8 error detection codes

The Timing Block provides timing for the other RLOP blocks using the parallel data clock, and frame pulse inputs as reference sources. The Timing Block maintains counters which identify channels and bytes within channels. Identified bytes along with generated clocks are provided to other RLOP blocks.

The FERF Detect Block detects the presence of Line Far End Receive Failure in the STS-12 stream. Output FERF is asserted when a 110 binary pattern is detected in bits 6, 7, and 8 of the STS-1 #1 K2 line layer byte, for five consecutive frames. FERF is deasserted when any pattern other than 110 is detected in bits 6, 7, and 8 of the K2 byte for five consecutive frames. The Received FERF alarm is available at the RFERF output pin, and is updated on the falling edge of RHCLK.

The Line AIS Block detects the presence of a Line Alarm Indication Signal (LAIS) in the STS-12 stream. Output LAIS is asserted when a 111 binary pattern is detected in bits 6,7,8 of the K2 byte, contained in the line layer of STS-1 #1, for five consecutive frames. LAIS is deasserted when any pattern other than 111 is detected in bits 6, 7, and 8 of the K2 byte for five consecutive frames. LAIS is updated with timing aligned to RHCLK.

The APS Extract Block extracts the Automatic Protection Switch Channel (bytes K1 and K2) from STS-1 #1 of the STS-12 stream. The extracted bytes are serialized and output on signal RAPS at a nominal 128 kbit/s rate. Timing for downstream processing of the APS channel is provided by the RAPSCLK output. RAPSCLK is derived from a 144 kHz clock that is gapped to yield an average frequency of 128 kHz. APS is updated with timing aligned to RAPSCLK. In turn, RAPSCLK is updated with timing aligned to RHCLK.

The Data Link Extract Block extracts the line data communication channel (bytes D4 to D12) from STS-1 #1 of the STS-12 stream. The extracted bytes are serialized and output on signal DL at a nominal 576 kbit/s rate. Timing for downstream processing of the data communication channel is provided by the DLCLK output. DLCLK is derived from a 2.16 MHz 67%(high)/33%(low) clock that is gapped to yield an average frequency of 576 kHz. DL is updated with timing aligned to DLCLK. In turn, DLCLK is updated with timing aligned to RHCLK.

The Order Wire Extract Block extracts the line order wire channel (byte E2) from STS-1 #1 of the STS-12 stream. The extracted bytes are serialized and output on signal OW at a nominal 64 kbit/s rate. Timing for downstream processing of the order wire channel is provided by the OWCLK output. OWCLK is derived from an 72 kHz clock that is gapped to yield an average frequency of 64 kHz. RLOW is updated with

timing aligned to RLOWCLK. In turn, RLOWCLK is updated with timing aligned to RHCLK.

The Error Monitor Block calculates the received line BIP-8 error detection codes based on the line overheads and synchronous payload envelopes of each of the constituent STS-1s in the STS-12 stream. The line BIP-8 code is a bit interleaved parity calculation using even parity. Details are provided in the references. The calculated BIP-8 codes are compared with the BIP-8 codes extracted from each constituent STS-1 of the following frame. Any differences indicate that a line layer bit error has occurred. Up to 768000 (12 x 8 x 8000) bit errors can be detected per second.

The Error Monitor Block accumulates these line layer bit errors in a 20 bit saturating counter that can be read via the microprocessor interface. The counter's contents are transferred to the read register, then cleared to 0 by a write command. Note, this counter should be polled at least once per second to avoid saturation which in turn may result in missed bit error events.

Byte Interleaved Demultiplexing

Byte Interleaved Demultiplexing is located on the PM5311 SLTX integrated circuit along with the Receive Line Overhead Processor. Once the SLTX has been optioned for STS-12, this demultiplexor will separate a byte-serial STS-12 data stream into 4 byte serial STS-3 streams with a common 19.44 MHz clock (RCLK) and a common 8 kHz frame pulse (RFP).

The high speed input clock, RHCLK, is divided by four to produce the RCLK signal. The falling edge of RCLK updates the low speed output streams. RFP signal indicates the location of the first byte of the transport overhead in the low speed output streams.

A demultiplex block controls the demultiplexing of the high speed byte serial input stream from the receive line overhead processor. The high speed clock, RHCLK, loads the byte wide input stream into one of four demultiplexor registers. The demultiplex block loads these registers sequentially, so that outputs RD1[7:0], RD2[7:0], RD3[7:0], and RD4[7:0] receive data for STS-3 #1, STS-3 #2, STS-3 #3, STS-3 #4, etc.

A retiming block contains registers which sample the demultiplexed byte serial stream on the falling edge of the low speed output clock, RCLK. Thus, RD1[7:0], RD2[7:0], RD3[7:0], and RD4[7:0] are updated on the falling edge of RCLK.

Byte Interleaved Multiplexing

The STS-3 to STS-12 Byte Interleaved Multiplexing is located on the PM5311 SLTX. It is comprised of a timing interface block, and a sample and mux block.

The Timing Block provides timing signals necessary for the operation of the multiplexer. Its high speed input clock, THCLK, is divided by four to produce a data sample clock. The phase alignments of the sample clock, and the 19.44 MHz input clock, TCLK, are compared in order to monitor for violations of set-up or hold times. These violations may occur during the transfer of the low speed input data from TCLK based timing to THCLK based timing. If the two clocks are aligned such that set-up or hold times may be violated , a phase alignment error event is generated, and the phase alignment of the sample clock is modified to avoid timing errors. A jitter tolerance between the sample clock and the nominal phase alignment of TCLK is up to ±0.375 unit intervals for STS-3 to STS-12 multiplexing.

The Sample and Mux Block contains registers used to sample the low speed input data using TCLK. The sampled data is then transferred to THCLK based timing using the data sample clock, and multiplexed onto the high speed data output bus to the transmit line overhead processor.

Transmit Line Overhead Insertion

Line overhead is inserted into the transmit signal by the Transmit Line Overhead Processor, (TLOP) which is located on the PM5311 SLTX integrated circuit. The Transmit Line Overhead Processor is composed of six functional blocks.

1. Timing Block: provides timing for the other blocks within the Transmit Line Overhead Processor.

2. APS Insert Block inserts the Automatic Protection Switch channel data into the STS-12 stream.

3. Data Link Insert Block inserts the line data communication channel into the STS-12 stream.

4. Order Wire Insert Block inserts the line order wire channel data into the STS-12 stream.

5. BIP-8 Calculate and Insert Block: calculates the line BIP-8 error detection code for each of the constituent STS-1s.

6 The input to the data link can be connected to the HDLC Transmitter so that it can be written to directly from a microprocessor.

The Timing Block provides timing for the other blocks within the Transmit Line Overhead Processor. The PICLK and FPIN inputs are the source of timing. The timing is preset for the STS-12 byte serial format. A channel counter is maintained, allowing individual bytes to be identified as required for the other blocks within the Transmit Line Overhead Processor. The channel counter skips the section overhead byte locations. The Timing Block regenerates the input clock and frame pulses from

the Byte Interleaved MUX block, and provides them to the Transmit Section Overhead processor

The APS Insert Block inserts the automatic protection switch channel (bytes K1 and K2) into STS-1 #1 of the STS-12 stream when enabled by an internal register. The data in the K1 and K2 slots is passed transparently while APS insertion is disabled. The K1 and K2 bytes are input serially using the TAPS signal at a nominal 128 kbit/s rate. Timing for processing of the TAPS channel is provided by the TAPSCLK output. TAPSCLK is derived from a 144 kHz clock that is gapped to yield an average frequency of 128 kHz. TAPS is sampled on the rising edge of TAPSCLK. APS insertion, when enabled, may be disabled by the TLDIS input.

The Data Link Insert Block inserts the line data communication channel (bytes D4 to D12) into STS-1 #1 of the STS-12 stream when enabled by an internal register. The data on PIN[7:0] is passed transparently while data link insertion is disabled. The D4 to D12 bytes are input serially using the TLDL signal at a nominal 576 kbit/s rate. Timing for processing of the line data communication channel is provided by the TLDLCLK output, which is derived from a 1.728 MHz clock that is gapped to yield an average frequency of 576 kHz. TLDL is sampled on the rising edge of TLDLCLK. Line data communication channel insertion, when enabled, may be disabled by the TLDIS input.

The Order Wire Insert Block inserts the line order wire channel (E2 byte) into STS-1 #1 of the STS-12 stream when enabled by an internal register. The data in the order wire time slots is passed transparently while order wire insertion is disabled. The E2 byte is input serially using the TLOW signal at a nominal 64 kbit/s rate. Timing for processing of the line order wire is provided by the TLOWCLK output, which is derived from a 72 kHz clock that is gapped to yield an average frequency of 64 kHz. TLOW is sampled on the rising edge of TLOWCLK. Line order wire insertion, when enabled, may be disabled by the TLDIS input.

The BIP-8 Calculate and Insert Block calculates the line BIP-8 error detection codes based on the line overheads and synchronous payload envelopes of each of the constituent STS-1s in the STS-12 stream. The line BIP-8 code is a bit interleaved parity calculation using even parity. Details are provided in the references. The calculated BIP-8 codes are inserted into the B2 byte positions of the constituent STS-1s of the following frame. Line BIP-8 insertion may be disabled by the TLDIS input. A diagnostic register bit may be set high to force a single bit error continuously in the least significant bit (bit 8) of each of the B2 bytes inserted in the STS-12 stream.

Transmit Section Overhead Insertion

Section overhead is inserted into the transmit signal by the Transmit Section Overhead Processor, (TSOP) which is located in the PM5301 SSTX. The Transmit Section Overhead Processor inserts the section overhead into the transmit SONET

The Transmit Section Overhead Processor accepts an unscrambled SONET data stream in byte serial format. It optionally inserts the data communication channel, the order wire channel, and the user channel into the section overhead of the unscrambled data stream. These section overhead channels are separately fed to the TSOP as bit serial inputs (TSDL, TSOW, TSUC). The Transmit Section Overhead Processor provides the bit serial clock for each section overhead channel (TSDLCLK, TSOWCLK, TSUCCLK). Line alarm indication signal may optionally be inserted into the data stream under the control of an external input (TLAIS), or a microprocessor writeable register.

The section BIP-8 error detection code is calculated by the TSOP and is optionally inserted into the section overhead of the SONET data stream. Framing and identity bytes are also optionally inserted. Finally, the complete SONET data stream is optionally scrambled and output by the Transmit Section Overhead Processor in byte serial format on outputs TSC_POUT[7:0].

The Transmit Section Overhead Processor operates with the downstream parallel-to-serial converter that accepts the SONET data stream in byte serial format and serializes it at the STS-12 line rate. The TSOP accepts data and appropriate clock and frame alignment indication signals supplied by the upstream line overhead processor.

Transmit Section HDLC Transmitter

The HDLC Transmitter is connected to the transmit section data communications channel. The HDLC Transmitter is a microprocessor peripheral used to transmit LAPD/HDLC frames. It performs all of the data serialization, CRC generation, zero-bit stuffing, as well as flag, idle, and abort sequence insertion. Transmit data is provided on an interrupt-driven basis by writing to a double-buffered transmit data register. Upon completion of the frames, a CRC-CCITT frame check sequence is transmitted, followed by idle flag sequences. If the transmit data register under flows, an abort sequence is automatically transmitted.

When enabled, the HDLC Transmitter continuously transmits the flag (01111110). Data to be transmitted is written into the Transmit Data Register. After the parallel-to-serial conversion of each data byte, (TINT) goes high to signal the microprocessor to write the next byte into the Transmit Data Register. After writing the last data frame byte, the EOM bit in the HDLC Transmitter Control Register must be set to transmit the CRC word (if CRC insertion bit is high), or to transmit a flag (if the CRC insertion bit is low). The HDLC Transmitter then returns transmitting flag characters.

An underrun situation can occur if data is not written to the HDLC Transmitter Transmit Data Register before the previous byte has been shifted out. In this case, the UDR bit in the Status Register is set to 1, TUDR is asserted, and an abort sequence is transmitted. An abort sequence can also be continuously transmitted by setting the ABT bit in the HDLC Transmitter Control Register.To free up CPU time

and avoid underruns, an external DMA controller may be used to transfer data from external memory to the HDLC Transmitter.

When the HDLC Transmitter is disabled, the external serial TSDL input is inserted in the section data communication channel. TSDL is sampled on the rising edge of TSDLCLK.

Parallel-To-Serial Conversion

The parallel-to-serial (8:1) multiplexor accepts the byte-wide transmit data at 77.76 Mbyte/s from the Transmit Section Overhead processor, and transmits a single 622.08 Mbit/s data stream at the balanced ECL outputs, TSD+/-. It is implemented with a GaAs integrated circuit which has ECL compatible inputs and outputs. CMOS to ECL level translators interface the up stream circuits with this IC.

The parallel data is clocked into the converter by the 77.76 MHz parallel output clock from the section overhead insertion block. The 622.08 MHz clock from the Transmit Clock Generator is divided by 8 to create a clock that is used to synchronize the input data to the internal timing of the multiplexor.

The parallel output clock loads the data into a buffer register, then the internal 77.76 MHz clock transfers the data from the buffer into another register. A transfer verification circuit monitors the two registers for discrepancies caused by setup and hold violations during the transfer. If there are discrepancies, the internal 77.76 MHz clock will invert at the beginning of the next frame, in order to correct the phase relationship between it and up stream 77.76 MHz clock. This corrective action will provide a phase difference between the two clocks that is sufficiently large to prevent further corrections.

The parallel data from the second register is then clocked into a parallel in, serial out shift register by the internal 77.76 MHz clock. The output data at the balanced ECL outputs,TSD+/- is updated by the falling edge of the 622 MHz clock provided at the balanced ECL outputs, TSCLK+/-. This clock is driven from the output of the Transmit Clock Generator.

Transmit Clock Generation

The 622.08 MHz transmit clock is generated by a VCO which is phase locked to the reference input , REF. The frequency of this input must be 19.44 MHZ ± 20 ppm. and must have phase noise of less than 0.01 UI pp in a 12 KHz to 2.5 MHz pass band.

The phase locked loop is implemented with a GaAs circuit which is similar to the receive clock regenerator. It aligns the low to high transitions of a 19.44 MHz signal, derived by dividing the transmit clock by 32, to those of the reference input REF. The transmit clock generator drives the transmit parallel to serial converter's

The phase locked loop is implemented with a GaAs circuit which is similar to the receive clock regenerator. It aligns the low to high transitions of a 19.44 MHz signal, derived by dividing the transmit clock by 32, to those of the reference input REF. The transmit clock generator drives the transmit parallel to serial converter's 622.08 MHz clock input. It also provides the 77.76 MHz THCLK for the transmit multiplexor and overhead processors.

Microprocessor Interface

The Microprocessor Interface Block provides the logic required to interface the normal mode and test mode registers within the SLIM-12 to a generic microprocessor bus. The normal mode registers are used during normal operation to configure and monitor the SLIM-12 and the test mode registers are used to enhance the testability of the SLIM-12 during production. The register set is accessed as shown in the following Register Map tables.

SECTION REGISTER MAP (SCSB = Low)

A[4:0]	Register
00H	RSOP Control
01H	RSOP Interrupt Status
02H	RSOP Lower Error Count
03H	RSOP Upper Error Count
04H	HDLC Receiver Control
05H	HDLC Receiver Interrupt Status/Control
06H	HDLC Receiver Status
07H	HDLC Receiver Receive Data
08H	TSOP Control
09H	TSOP Diagnostic
0AH-0BH	TSOP Reserved
0CH	HDLC Transmitter Control
0DH	HDLC Transmitter Status
0EH	HDLC Transmitter Transmit Data
0FH	HDLC Transmitter Reserved
10H	Reserved
11H-1FH	Unused

LINE REGISTER MAP (LCSB = Low)

A[4:0]	Register
00H	Master Configuration
01H	Master Interrupt Enable
02H	Master Interrupt Status
03H	Master Reset and Identity
04H	TLOP Control
05H	TLOP Diagnostic
06H - 07H	Reserved
08H	RLOP Control/Status
09H	RLOP Interrupt
0AH	Line BIP-8 Error Count #1
0BH	Line BIP-8 Error Count #2
0CH	Line BIP-8 Error Count #3
0DH	Reserved
0EH	BIMX Interrupt
0FH	Reserved
1XH	Reserved for Test

NORMAL MODE REGISTER DESCRIPTION

Normal mode registers are used to configure and monitor the operation of the SLIM-12. Normal mode registers (as opposed to test mode registers) are selected when TRSB is high.

Notes on Normal Mode Register Bits:

1. Writing values into unused register bits has no effect. Reading back unused bits can produce either a logic 1 or a logic 0; hence unused register bits should be masked off by software when read.

2. All configuration bits that can be written into can also be read back. This allows the processor controlling the SLIM-12 to determine the programming state of the block.

3. Writeable normal mode **register bits are cleared to logic 0 upon reset unless otherwise noted.**

4. Writing into read-only normal mode register bit locations does not affect SLIM-12 operation unless otherwise noted.

Line Overhead Registers

Address 00H
Master Configuration

Bit	Type	Function
Bit 7		Unused
Bit 6		Unused
Bit 5	R/W	PLE
Bit 4	R/W	DXB
Bit 3	R/W	MXB
Bit 2	R/W	PCS
Bit 1	R/W	MODE[1]
Bit 0	R/W	MODE[0]

The MODE[1:0] bus selects the operating mode of the transmit and receive line overhead processors as follows:

00	selects	STS-1
01	selects	STS-3
10	selects	STS-9
11	selects	STS-12

Mode[1:0] must be set for STS-12 after reset for the SLIM-12 to operate.

the Byte Interleaved Mux, BIMX and Byte Interleaved Demux, BIDX are configured as a 1:4 and 4:1 multiplexer/demultiplexer pair when STS-12 mode is selected. BIMX and BIDX may also be bypassed while in STS-12 mode using the MXB and DXB bits respectively.

The parallel clock select (PCS) bit selects the timing mode for the transmit and receive line overhead processors as follows:

0	selects	STS-12 timing
1	selects	line overhead timing

The MXB and DXB bits control the bypassing of the multiplexer and demultiplexer blocks respectively. When MXB is set to a logic 0, the multiplexer block is enabled, and the three or four byte serial input streams are multiplexed to a single byte serial stream before the line overhead is inserted. When MXB is set to a logic 1, the multiplexer block is bypassed, and one byte serial input stream is processed. Similarly, when DXB is set to a logic 0, the demultiplexer block is enabled, and the byte serial input stream is demultiplexed into three or four byte serial output streams. When DXB is set to a logic 1, the demultiplexer block is bypassed, and one byte serial output stream is available.

The payload loopback enable bit (PLE) controls the payload loopback of the SLTX. When PLE is a logic 1, payload loopback is enabled, and the receive byte serial STS-12 stream (RPIN[7:0] is passed directly to the Transmit Line Overhead Processor block where new line overhead may be inserted, and the resulting byte serial stream is output on TPOUT[7:0]. When PLE is a logic 0, payload loopback is disabled.

Address 01H
Master Interrupt Enable

Bit	Type	Function
Bit 7		Unused
Bit 6		Unused
Bit 5		Unused
Bit 4		Unused
Bit 3		Unused
Bit 2		Unused
Bit 1	R/W	BIMXE
Bit 0	R/W	RLOPE

This register provides an interrupt enable bit for each of the blocks in the SLTX. Interrupts may still be masked within each block. Interrupts enabled at the block level, but masked by this register are reported in the Master Interrupt Status Register. Interrupts disabled at the block level are not reported by the Master Interrupt Status Register.

Address 12H
Master Interrupt Status

Bit	Type	Function
Bit 7		Unused
Bit 6		Unused
Bit 5		Unused
Bit 4		Unused
Bit 3		Unused
Bit 2		Unused
Bit 1	R/W	BIMXI
Bit 0	R/W	RLOPI

This register identifies the block that is the source of a pending interrupt. It may be necessary to read the Interrupt Status/Diagnostic Register of the interrupting block to determine the event that caused the interrupt. Interrupts disabled at the block level by the Master Interrupt Enable Register are not reported by this register.

Address 03H
Master Reset and Identity

Bit	Type	Function
Bit 7	R/W	RESET
Bit 6	R	ID[6]
Bit 5	R	ID[5]
Bit 4	R	ID[4]
Bit 3	R	ID[3]
Bit 2	R	ID[2]
Bit 1	R	ID[1]
Bit 0	R	ID[0]

This register allows software to asynchronously reset the SLTX. The software reset is equivalent to setting the RSTB input pin low. Setting the RESET bit to logic 1 causes the SLTX to be reset. Setting the RESET bit to logic 0 causes reset to be removed. The RESET bit must be explicitly set and cleared by writing the corresponding logic value to this register.

The version identification bits ID[6:0], are set to a fixed value representing the version number of the SLTX. These bits can be read by software to determine the version number.

Address 04H
TLOP Control

Bit	Type	Function
Bit 7	R/W	ACCEL
Bit 6		Unused
Bit 5		Unused
Bit 4	R/W	DGROWTH
Bit 3	R/W	DAPS
Bit 2	R/W	DDL
Bit 1	R/W	DOW
Bit 0	R/W	FERF

The FERF bit controls the insertion of transmit line Far End Receive Failure (FERF). When FERF is set to a logic one, line FERF is inserted into the STS-N stream on TPOUT[7:0]. Line FERF is inserted by transmitting the code 110 (binary) in bit positions 6, 7, and 8 of the K2 byte contained in STS-1 #1 of the STS-N stream.

The DGROWTH, DOW, DDL, and DAPS bits control the overwriting of the line growth bytes, the line order wire channel, the line data communication channel, and the automatic protection switch channel. When DGROWTH is set to a logic one the growth byte positions in all STS-1s are not overwritten with zero bytes. When DOW is set to a logic one, the line order wire channel byte position in STS-1 #1 is not overwritten by the data shifted in on input TOW. When DDL is set high, the data communication channel byte positions in STS-1 #1 are not overwritten by the data shifted in on input TDL. When DAPS is set high, the APS byte positions in STS-1 #1 are not overwritten by the APS channel data shifted in on input TAPS.

The ACCEL bit is used for simulation purposes and must be written with a logic 0 for proper operation.

Address 05H
TLOP Diagnostic

Bit	Type	Function
Bit 7		Unused
Bit 6		Unused
Bit 5		Unused
Bit 4		Unused
Bit 3		Unused
Bit 2		Unused
Bit 1		Unused
Bit 0	R/W	DBIP8

The DBIP8 bit controls the insertion of a single bit error continuously in each of the line BIP-8 bytes (B2 bytes). When DBIP8 is set high, the least significant bit of each of the B2 bytes is inverted.

Address 08H
RLOP Control/Status

Bit	Type	Function
Bit 7	R/W	ACCEL
Bit 6		Unused
Bit 5		Unused
Bit 4		Unused
Bit 3		Unused
Bit 2		Unused
Bit 1	R	LAIS
Bit 0	R	FERF

The LAIS, and FERF bits reflect the current state of the RLAIS and RFERF outputs respectively.

The ACCEL bit is used for simulation purposes and must be written with a logic 0 for proper operation.

Address 09H
RLOP Interrupt

Bit	Type	Function
Bit 7		Unused
Bit 6	R/W	BIPEE
Bit 5	R/W	LAISE
Bit 4	R/W	FERFE
Bit 3		Unused
Bit 2	R	BIPEI
Bit 1	R	LAISI
Bit 0	R	FERFI

The BIPEE, LAISE, and FERFE bits are interrupt enables. When a 1 is written to these locations, the occurrence of the corresponding event will activate the interrupt output, INTB (if the Master Interrupt Enable Register is programmed to enable RLOP interrupts). INTB is removed when the RLOP Interrupt register is read.

The BIPEI, LAISI, and FERFI bits are set high when a transition occurs on the BIPE. TLAIS, or TFERF outputs respectively. These bits are cleared when the RLOP Interrupt register is read.

Address 0AH
RLOP Line BIP-8 Error Count #1

Bit	Type	Function
Bit 7	R	BE7
Bit 6	R	BE6
Bit 5	R	BE5
Bit 4	R	BE4
Bit 3	R	BE3
Bit 2	R	BE2
Bit 1	R	BE1
Bit 0	R	BE0

Address 0BH
RLOP Line BIP-8 Error Count #2

Bit	Type	Function
Bit 7	R	BE15
Bit 6	R	BE14
Bit 5	R	BE13
Bit 4	R	BE12
Bit 3	R	BE11
Bit 2	R	BE10
Bit 1	R	BE9
Bit 0	R	BE8

Address 0CH
RLOP Line BIP-8 Error Count #3

Bit	Type	Function
Bit 7		Unused
Bit 6		Unused
Bit 5		Unused
Bit 4		Unused
Bit 3	R	BE19
Bit 2	R	BE18
Bit 1	R	BE17
Bit 0	R	BE16

Bits BE0 through BE19 represent the number of line bit-interleaved parity errors that have been detected since the last time the error count was polled. To poll the error count one must write to any of the Line BIP-8 Error Count register addresses. Such a write transfers the the internally accumulated error count to the Error Count registers within 3 BIPECLK cycles (max ~ 1µs) and simultaneously resets the internal counter to begin a new cycle of error accumulation. After the 1µs period has elapsed, the Line BIP-8 Error Count registers may be read.

Address 0EH
BIMX Interrupt

Bit	Type	Function
Bit 7		Unused
Bit 6		Unused
Bit 5		Unused
Bit 4		Unused
Bit 3		Unused
Bit 2		Unused
Bit 1	R/W	PAEE
Bit 0	R	PAEI

The PAEE bit is an interrupt enable. When a 1 is written to this location, the occurrence of the corresponding event will activate the interrupt output, INTB (if the Master Interrupt Enable Register is programmed to enable BIMX interrupts). INTB is removed when the BIMX Interrupt register is read.

The PAE bit is set high when a phase alignment error is detected between the low rate multiplex clock (TLPICLK), and an internal sampling signal generated by the high rate multiplex clock (TPICLK) . This bit is cleared when the BIMX Interrupt register is read.

Section Overhead Registers

Register 00H
RSOP Control/Status

Bit	Type	Function
Bit 7	R/W	ACCEL
Bit 6	R/W	DDS
Bit 5	R/W	FOOF
Bit 4		Unused
Bit 3	R/W	BIPEE
Bit 2	R/W	LOSE
Bit 1	R/W	LOFE
Bit 0	R/W	OOFE

The OOFE, LOFE, LOSE, and BIPEE bits are interrupt enables. When a 1 is written to these locations, an occurrence of the corresponding event will activate the interrupt (R_INT) output. The interrupt is cleared by reading the RSOP Interrupt Status register.

When a 1 is written to the Force Out-of-Frame (FOOF) bit location, the SSTX is forced out-of-frame at the next frame boundary. The FOOF bit is a write only bit; a Control register read may yield a 1 or a 0 in this bit position.

The active high Disable Descrambling (DDS) bit is set to disable the descrambling of the receive STS-1/3/9/12 stream.

The ACCEL bit is used for simulation purposes and must be written with a logic 0 for proper operation.

Register 01H
RSOP Interrupt

Bit	Type	Function
Bit 7		Unused
Bit 6	R	BIPEI
Bit 5	R	LOSI
Bit 4	R	LOFI
Bit 3	R	OOFI
Bit 2	R	LOSS
Bit 1	R	LOFS
Bit 0	R	OOFS

The OOFS, LOFS, and LOSS bits reflect the current state of outputs OOF, LOF, and LOS respectively

The OOFI, LOFI, LOSI, and BIPEI bits are set high when a transition occurs on the corresponding output. If the corresponding interrupt enable bit is set in the RSOP Control register, then the interrupt (R_INT) output is activated These bits are cleared when the Interrupt Status register is read.

Register 02H
RSOP Error Count1

Bit	Type	Function
Bit 7	R	BE7
Bit 6	R	BE6
Bit 5	R	BE5
Bit 4	R	BE4
Bit 3	R	BE3
Bit 2	R	BE2
Bit 1	R	BE1
Bit 0	R	BE0

The Error Count1 Register is provided at RSOP read/write address 2.

Register 03H
RSOP Error Count2

Bit	Type	Function
Bit 7	R	BE15
Bit 6	R	BE14
Bit 5	R	BE13
Bit 4	R	BE12
Bit 3	R	BE11
Bit 2	R	BE10
Bit 1	R	BE9
Bit 0	R	BE8

The Error Count2 Register is provided at RLOP read/write address 3.

Register 04H
HDLC Receiver Control

Bit	Type	Function
Bit 7		Unused
Bit 6		Unused
Bit 5		Unused
Bit 4		Unused
Bit 3		Unused
Bit 2		Unused
Bit 1	W	TR
Bit 0	R/W	EN

The enable bit (EN) controls the overall operation of the HDLC Receiver. When set, the HDLC Receiver is enabled; when reset the HDLC Receiver is disabled. When the PM4206 is disabled, the FIFO and interrupts are cleared. The programming of the HDLC Receiver Interrupt Status/Control Register is not affected. When the HDLC Receiver is enabled, it will immediately begin looking for flags.

Setting the terminate reception bit (TR) forces the HDLC Receiver to immediately terminate the reception of the current frame, empty the FIFO, clear the interrupts, and begin searching for a new flag sequence. The HDLC Receiver handles the TR input in the same manner as if the EN bit had been cleared and then set.

Register 05H
HDLC Receiver Interrupt Status/Control

Bit	Type	Function
Bit 7		Unused
Bit 6		Unused
Bit 5		Unused
Bit 4		Unused
Bit 3		Unused
Bit 2	W	INTC1
Bit 1	W	INTC0
Bit 0	R	INT

Bit positions INTC1 and INTC0 control when the interrupt output (RHDLC_INT) is asserted in the following way:

INTC1	INTC0	Description
0	0	Disable interrupt (All sources)
0	1	Enable interrupt when FIFO receives data
1	0	Enable interrupt when FIFO has 2 bytes of data
1	1	Enable interrupt when FIFO has 3 bytes of data

Bit position INT reflects the status of the interrupt output, unless the INTC1 and INTC0 bits are set to disable interrupts. In that case, the interrupt output is forced to 0 and the INT bit of the Interrupt Status/Control Register will reflect the state of the internal interrupt latch.

In addition to the FIFO fill status, interrupts are also generated for EOM (end of message), OVR (FIFO overrun), detection of the abort sequence while not receiving all ones and on detection of the first flag while receiving all ones. The interrupt is reset by an HDLC Receiver Receive Data Register read that empties the FIFO, unless the cause of the interrupt was due to a FIFO overrun. The interrupt due to a FIFO overrun is cleared on a Status Register read, by disabling the TSB, or by setting TR high.

The contents of the HDLC Receiver Interrupt Status/Control Register should only be changed when the HDLC Receiver is disabled to prevent any erroneous interrupt generation.

Register 06H
HDLC Receiver Status

Bit	Type	Function
Bit 7	R	FE
Bit 6	R	OVR
Bit 5	R	FLG
Bit 4	R	EOM
Bit 3	R	CRC
Bit 2	R	NVB2
Bit 1	R	NVB1
Bit 0	R	NVB0

The NVB[2:0] bit positions indicate the number of valid bits in the HDLC Receive Data Register. It is possible that not all of the bits in the HDLC Receive Data Register are valid when the last data byte is read. The data frame can be any number of bits in length and not necessarily an integral number of bytes. The Receive Data Register is filled from the MSB to the LSB bit position. One to eight data bits are valid. The number of valid bits is equal to 1 plus the value of NVB[2:0]. A NVB[2:0] value of 000B indicates that only the MSB in the register is valid. NVB[2:0] is only valid when EOM is a logic 1 and FLG is a logic 1 and OVR is a logic 0.

The CRC bit is set if a CRC error was detected in the last received frame. The CRC bit is only valid when EOM is logic 1 and FLG is a logic 1 and OVR is a logic 0.

If the status register is read for the status of the data byte written due to the interrupt on the detection of first flag, then the NVB[2:0] and CRC bits will be invalid, even though the EOM bit is logic 1 and the FLG bit is logic 1.

The End of Message bit (EOM) follows the RHDLC_EOM output. It is set when:

1) The last byte in the frame (EOM) is being read from the HDLC Receive Data Register,

2) An abort sequence is detected while not in the receiving all ones state and the byte written to the FIFO due to the detection of the abort sequence is being read from the FIFO

3) The first flag has been detected and the dummy byte written into the FIFO when the HDLC Receiver has moved from the receiving all ones state to the receiving flags state is being read from the FIFO.

4) Immediately on detection of FIFO overrun.

The EOM bit is passed through the FIFO with the data so that the status will correspond to the data just read from the FIFO.

The flag bit (FLG) is set if the HDLC Receiver has detected the presence of the LAPD flag sequence (01111110) in the data. FLG is reset only when the LAPD abort sequence (01111111) is detected in the data or when the PM4206 is disabled. This bit is passed through the FIFO with the Data so that the Status will correspond to the Data just read from the FIFO.

The Receiver Overrun bit (OVR) is set when data is written over unread data in the FIFO. This bit is not reset until after the Status Register is read. While OVR is high, the HDLC Receiver and FIFO are held in the reset state, causing the FLG and EOM bits in the status register to be reset also.

The FIFO Empty bit (FE) is high when the last FIFO entry is read and goes low when the FIFO is loaded with new data.

If the Receive Data Register is read while there is no valid data, then a FIFO underrun condition occurs. The underrun condition is reflected in the Status Register by forcing all bits to logic zero on the first Status register read following a Received Data Register Read which caused the underrun condition.

Register 07H
HDLC Receive Data

Bit	Type	Function
Bit 7	R	RD7
Bit 6	R	RD6
Bit 5	R	RD5
Bit 4	R	RD4
Bit 3	R	RD3
Bit 2	R	RD2
Bit 1	R	RD1
Bit 0	R	RD0

RD0 corresponds to the first bit of the serial byte received on the DATA input.

This register is actually a 4-level FIFO. If data is available the FE bit in Register 2 is low. If INTC[1:0] (in the Interrupt Control/Status Register) is set to 01 the Receiver Data register must be read within 31 data bit periods to prevent an overrun. If

INTC[1:0] is set to 11 the Receiver Data register must be read within 15 data bit periods.

When an overrun is detected, an interrupt is generated and the FIFO is held cleared until the status register is read. When the LAPD abort sequence (01111111) is detected in the data an ABORT interrupt is generated and the data that has been shifted into the serial-to-parallel converter is written into the FIFO.

A read of the Data Register increments the FIFO pointer at the end of the read. If the Data register read causes an FIFO underrun, then the pointer is inhibited from incrementing. The underrun condition will be signalled in the next status read by returning all zeros.

Register 08H
TSOP Control

Bit	Type	Function
Bit 7	R/W	ACCEL
Bit 6	R/W	DS
Bit 5		Unused
Bit 4	R/W	DC1
Bit 3	R/W	DUC
Bit 2	R/W	DDL
Bit 1	R/W	DOW
Bit 0	R/W	LAIS

The LAIS bit controls the insertion of line alarm indication signal (AIS). When LAIS is set high, the TSOP will insert AIS into the outgoing SONET stream. Activation or deactivation of line AIS insertion is synchronized to frame boundaries. Line AIS insertion results in all bits of the SONET frame being set to logic 1 prior to scrambling except for the section overhead.

The DOW, DDL, and DUC bits control the overwriting of the order wire channel, data communication channel, and user channel section overhead bytes respectively. When DOW is set high, the order wire channel byte position in STS-1 #1 is not overwritten by the data shifted in on input TOW. When DDL is set to logic 1, the data communication channel byte positions in STS-1 #1 are not overwritten by the data shifted in on input TDL. When DUC is set to logic 1, the user channel byte position in STS-1 #1 is not overwritten by the data shifted in on input TUC.

The DC1 bit controls the overwriting of the identity byte in the STS-12 stream. When DC1 is set to logic 0, the identity bytes of the constituent STS-1s in the STS-12 stream are programmed as specified in the references: STS-1 #1 C1 = 01

hexadecimal, STS-1 #2 C1 = 02 hexadecimal,..., STS-1 #N C1 = N hexadecimal. When DC1 is set to logic 1, the identity byte positions in each of the constituent STS-1s are not overwritten.

The active high ACCEL bit is asserted to enable an accelerated mode where the SONET STS-12 frame is "shortened" to consist of 90N bytes rather than 810N bytes (arranged as N times three 9 byte columns of transport overhead and N times seven 9 byte columns of synchronous payload envelope). **The accelerated mode** is provided only as a convenience for simulation and **must not be used during actual application**.

The active high Disable Scrambling (DS) bit is set high to disable scrambling of the byte serial STS-12 stream.

Register 09H
TSOP Diagnostic

Bit	Type	Function
Bit 7		Unused
Bit 6		Unused
Bit 5		Unused
Bit 4		Unused
Bit 3		Unused
Bit 2	R/W	DLOS
Bit 1	R/W	DBIP8
Bit 0	R/W	DFP

The DLOS bit controls the insertion of all zeros on the output . When DLOS is set to logic 1 the output data register is held reset and all output data is forced to 00H.

The DBIP8 bit controls the insertion of a single bit error continuously in the B1 section overhead byte. When DBIP8 is set high the least significant bit of the STS1 #1 B1 byte is inverted.

The DFP bit controls the insertion of a single bit error continuously in the most significant bit (bit 1) of the A1 section overhead framing byte. IF DFP is set high the A1 bytes of STS1 #1 to STS1 #N are set to 76H instead of F6H.

Register 0CH
HDLC Transmitter Control

Bit	Type	Function
Bit 7		Unused
Bit 6		Unused
Bit 5		Unused
Bit 4	R/W	EOM
Bit 3	R/W	INTE
Bit 2	R/W	ABT
Bit 1	R/W	CRC
Bit 0	R/W	EN

The enable (EN) bit controls the overall operation of the HDLC Transmitter. When the EN bit is set , the HDLC Transmitter is enabled. Flag sequences are sent until data is written into the HDLC Transmitter Transmit Data Register. When the EN bit is reset, the HDLC Transmitter is disabled and the TDL input is inserted in the section data communication channel. The THDLC_INT output and the interrupt (INT) bit (bit 1 of the HDLC Transmitter Status Register) remain active while the HDLC Transmitter is disabled.

The CRC enable (CRC) bit controls the generation of the CRC-CCITT frame check sequence. Setting this bit to logic 1 enables the CRC generator and appends the 16-bit frame check sequence (FCS) to the end of each frame. When the CRC bit is set to logic 0, the FCS is not appended to each frame.

The abort (ABT) bit controls the sending of the seven consecutive ones HDLC abort code. Setting the ABT bit to logic 1 causes the transmission of the "11111110" code after the transmission of the byte in the HDLC Transmitter Transmit Data Register. Abort characters are continuously sent until this bit is set to logic 0.

The interrupt enable (INTE) bit masks the interrupt output, TINT. When the INTE bit is a logic 0, the interrupt output is disabled; however, the INT bit in the Status Register is always enabled.

The end of message (EOM) bit is a control bit. Setting the EOM bit to logic 1 indicates to the HDLC Transmitter that the most recent byte of data written for transmission is the last byte of the present frame. If the CRC bit has the value logic 1, then the 16-bit CRC word will be transmitted after the last data byte, followed by the continuous transmission of flags. The EOM bit is automatically set to logic 0 before the transmission of the next data frame .

Register 0DH
HDLC Transmitter Status

Bit	Type	Function
Bit 7		Unused
Bit 6		Unused
Bit 5		Unused
Bit 4		Unused
Bit 3		Unused
Bit 2		Unused
Bit 1	R	INT
Bit 0	R/W	UDR

The interrupt (INT) bit is set to logic 1 when the byte in the HDLC Transmit Data Register has been loaded into the Parallel-to-Serial Convertor and a new byte can be written into the HDLC Transmitter Transmit Data Register.

The underrun (UDR) bit is set to logic 1 if the parallel-to-serial conversion of the byte in the Convertor is completed before the next data byte is written into the HDLC Transmit Data Register. The UDR bit must be reset to logic 0 by the controlling microprocessor to clear the underrun condition. After the UDR bit is set to logic 1, the next byte transmitted is an abort character, followed by a flag character in readiness to transmit the next valid data. If the UDR bit is still set to logic 1 after the transmission of the flag, the TSB continuously transmits the all ones idle pattern.

Register 0EH
HDLC Transmit Data

Bit	Type	Function
Bit 7	W	TD7
Bit 6	W	TD6
Bit 5	W	TD5
Bit 4	W	TD4
Bit 3	W	TD3
Bit 2	W	TD2
Bit 1	W	TD1
Bit 0	W	TD0

Data written to this register is transferred to the parallel-to-serial convertor. When the convertor is emptied, the INT bit in the Status Register is set to logic 1, and the TINT output goes high (unless the TINT output has been disabled by setting the INTE bit in the Configuration/Control Register to logic 0). The INT bit in the HDLC Transmitter Status Register is reset and the TINT output goes low immediately following the transfer of data into the HDLC Transmit Data Register. The data from the HDLC Transmit Data Register is transmitted LSB first.

After the INT output goes high, data must be written into the Transmit Data Register within six TSDLCLK periods to prevent an underrun error. At a TSDLCLK burst frequency of 216 kbit/s, this time is 27.7 µs.

TEST FEATURES DESCRIPTION

Test Mode Register Description

Test mode registers are used to apply test vectors during production testing of the SLIM-12. Test mode registers (as opposed to normal mode registers) are selected in the SSTX when TRSB is low, and in the SLTX when A[4] is high.

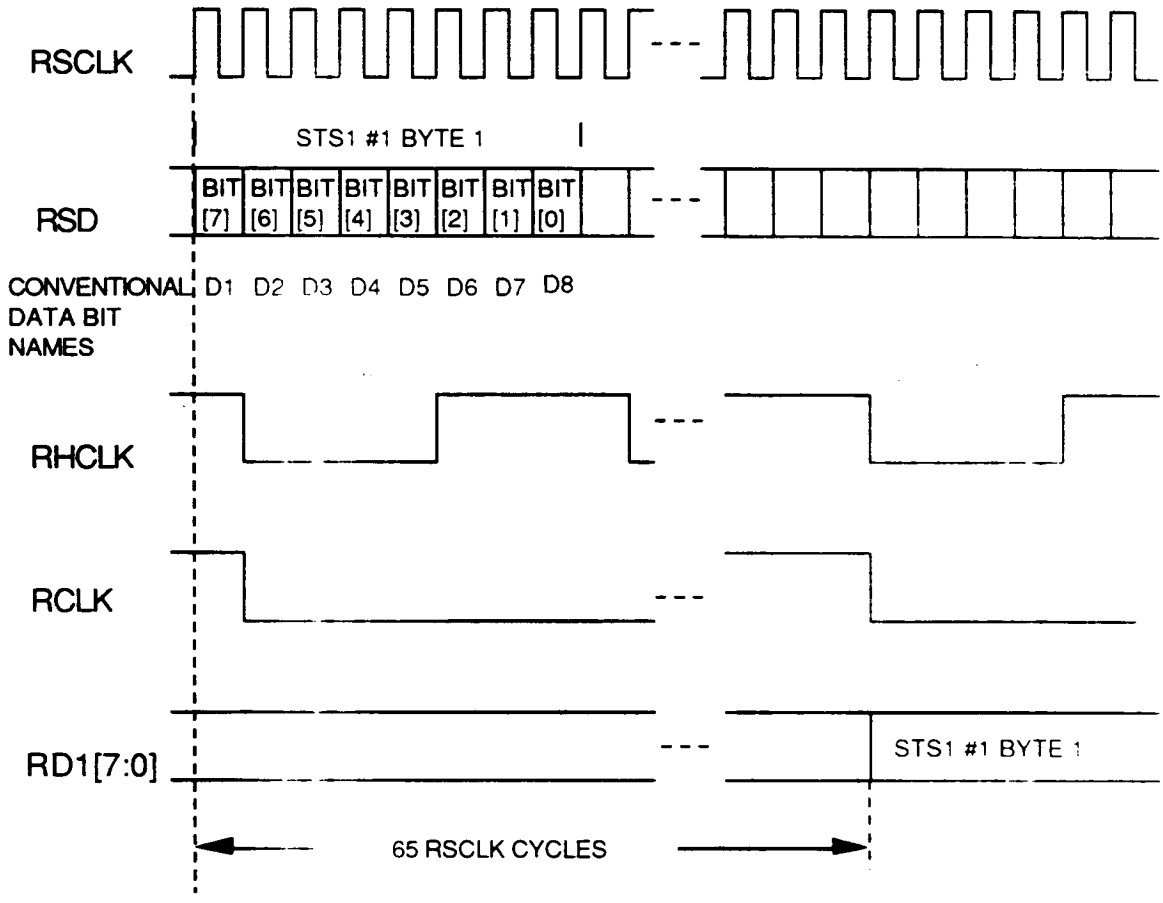
Various test modes are activated by writing the desired test mode number to a register. Test mode 0 verifies the inter TSB connections within the SSTX and SLTX chips as well as the connections between the chips themselves. Test modes other than test mode 0 test the TSBs individually.

No access to the test mode registers is required for normal applications of the SLIM-12.

FUNCTIONAL TIMING

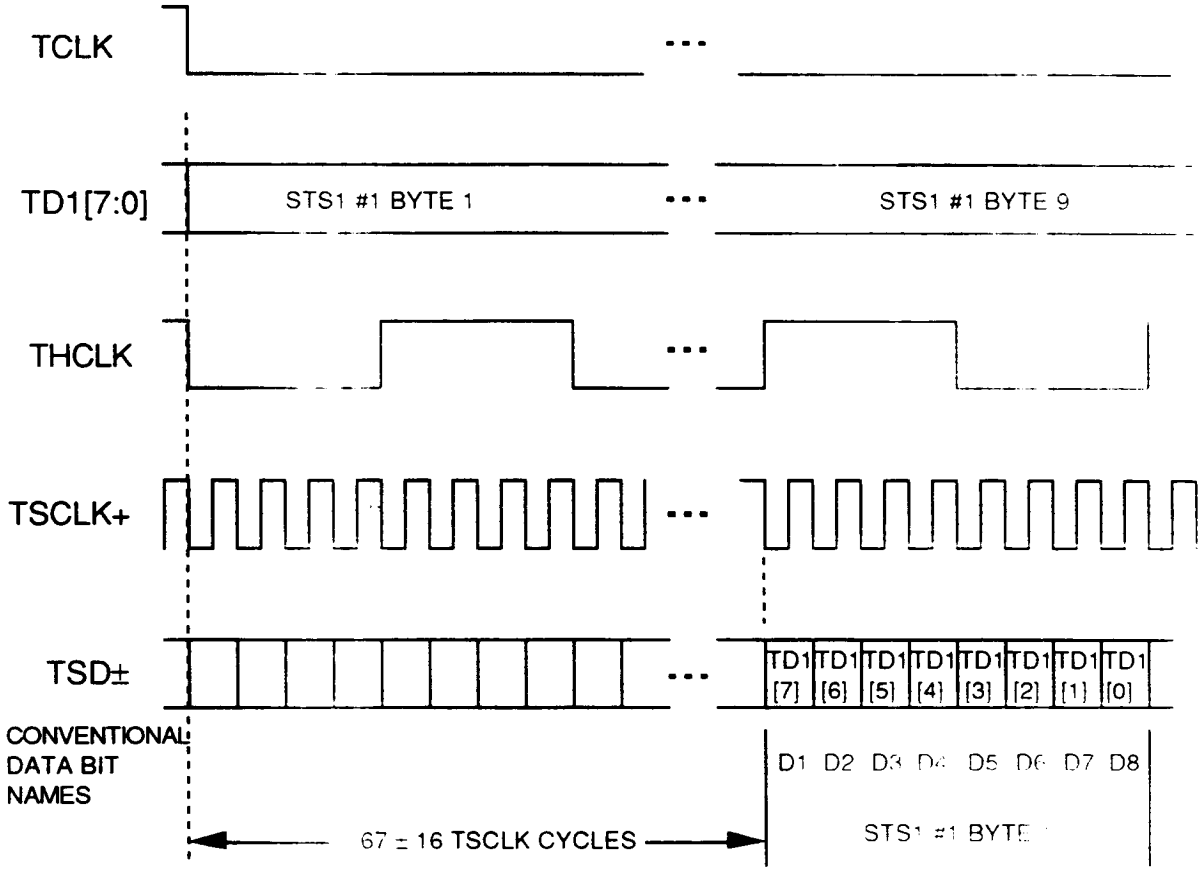
STS-12 Interface Timing Characteristics

Fig. 1 Receive Input/Output Timing



The Receive Serial Input timing diagram, (Figure 1) shows the functional timing relationship between the incoming data at RSD, and the recovered receive clock output RSCLK. It shows RHCLK changing state on the rising edge of RSCLK. The diagram also shows the delay, measured in RSCLK cycles, for data flowing through the SLIM-12. The delays for outputs RD2[7:0], RD3[7:0], and RD4[7:0] are 8, 16 and 24 RSCLK cycles less than shown.

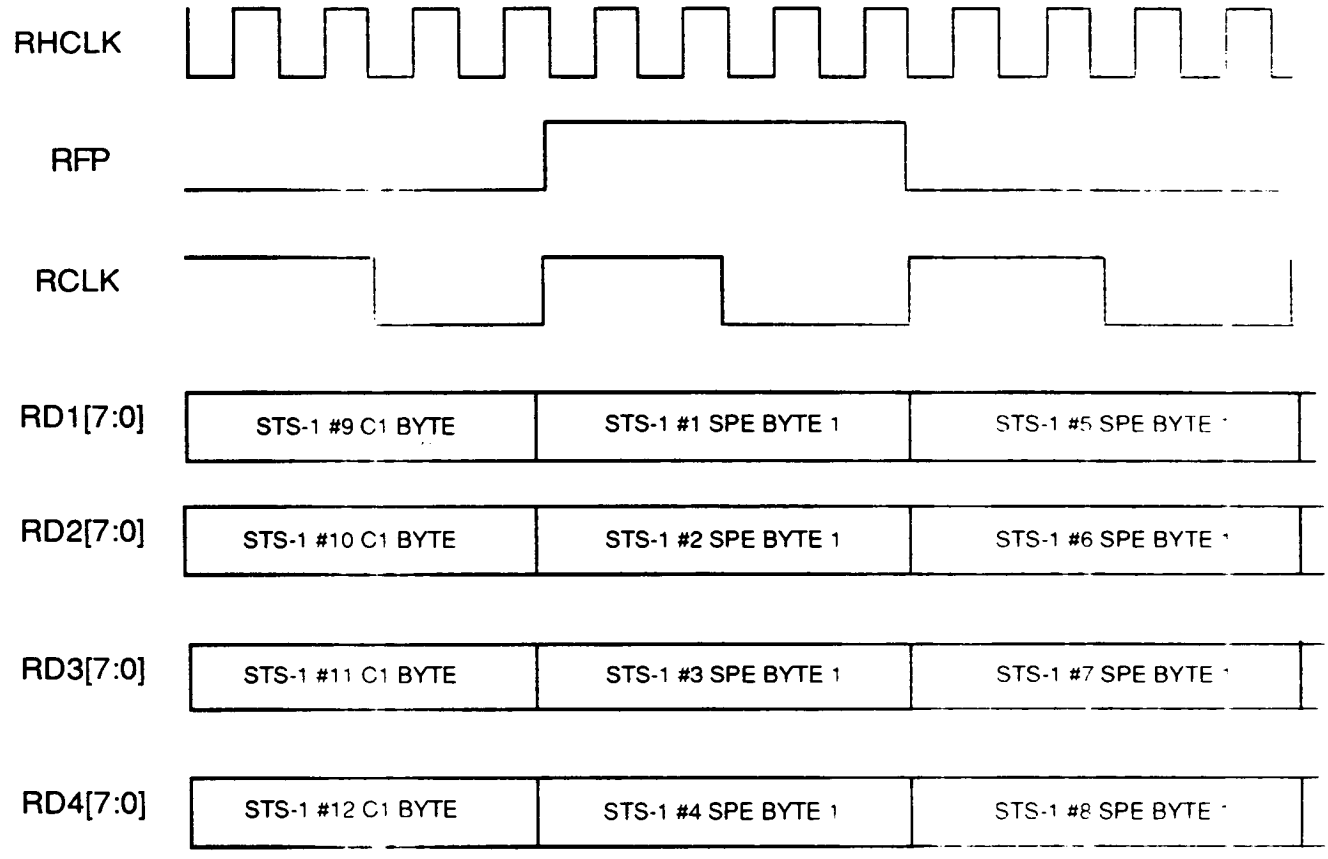
Fig. 2 Transmit Input/Output



The Transmit Serial Output functional timing diagram, (Figure 2) shows the serial output data changing on the falling edge of TSCLK+. It also shows the delay, measured in TSCLK cycles, between the TD1[7:0] input data and the output data. The data delay for TD2[7:0], TD3[7:0], and TD4[7:0] is 8, 16, and 24 TSCLK cycles longer than shown. The ± 16 cycle variation in these delays is caused by the two multiplexing steps, STS-3 to STS-12 and parallel to serial. This variable delay is dependant on the alignment of clock edges on each side of the multiplexing boundaries.

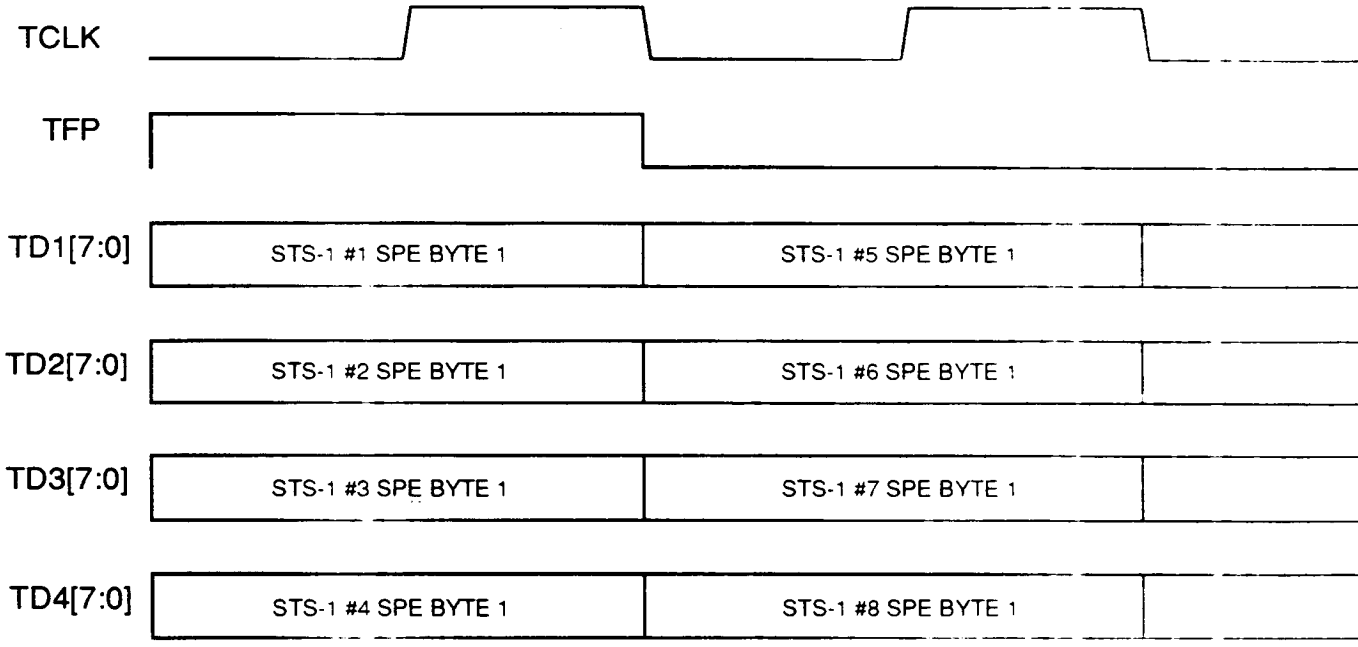
STS-3 Interface Timing Characteristics

Fig. 3 Receive Output Parallel Interface



The STS-12 to STS-3 Demultiplex Timing Diagram (Figure 3) illustrates the demultiplexing of a byte serial STS-12 stream into four byte serial STS-3 streams (on RD1[7:0], RD2[7:0], RD3[7:0], and RD4[7:0]). The STS-3 streams are broken into the constituent STS-1 streams in the timing diagram. The FPIN signal is high during the first SPE byte of STS-1 #1 in the STS-12 input stream. FPOUT is set high during the first SPE byte of STS-1 #1 in the STS-3 output streams. FPOUT is generated from FPIN; if FPIN is not present. FPOUT is not generated.

Fig. 4 Transmit Input Parallel Interface



The STS-3 streams are broken into the constituent STS-1 streams in the timing diagram. The FPIN signal is high during the first SPE byte of STS-1 #1 in the STS-3 input streams.

Receive Section Overhead Timing Characteristics

Fig. 5 In Frame Declaration

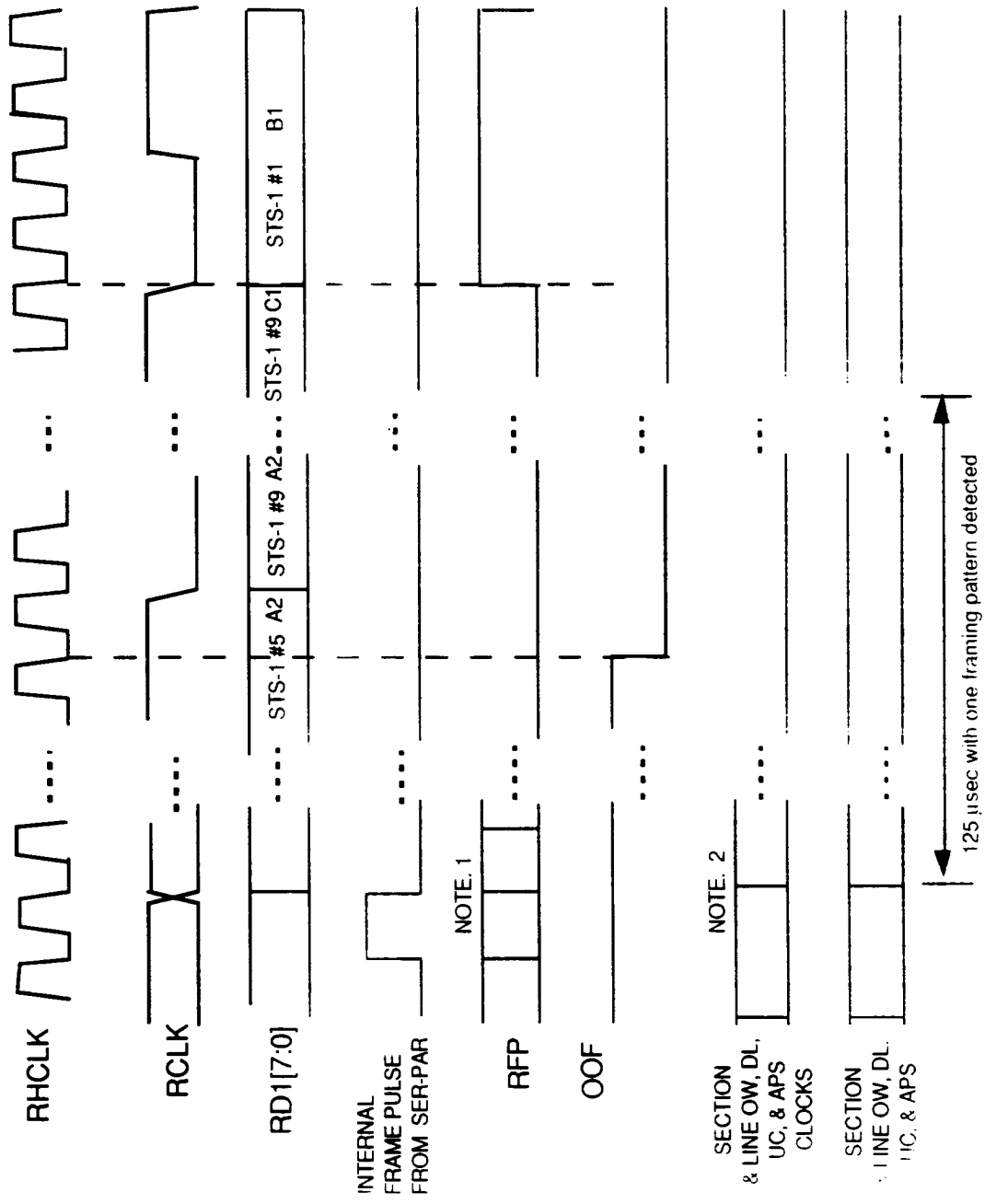
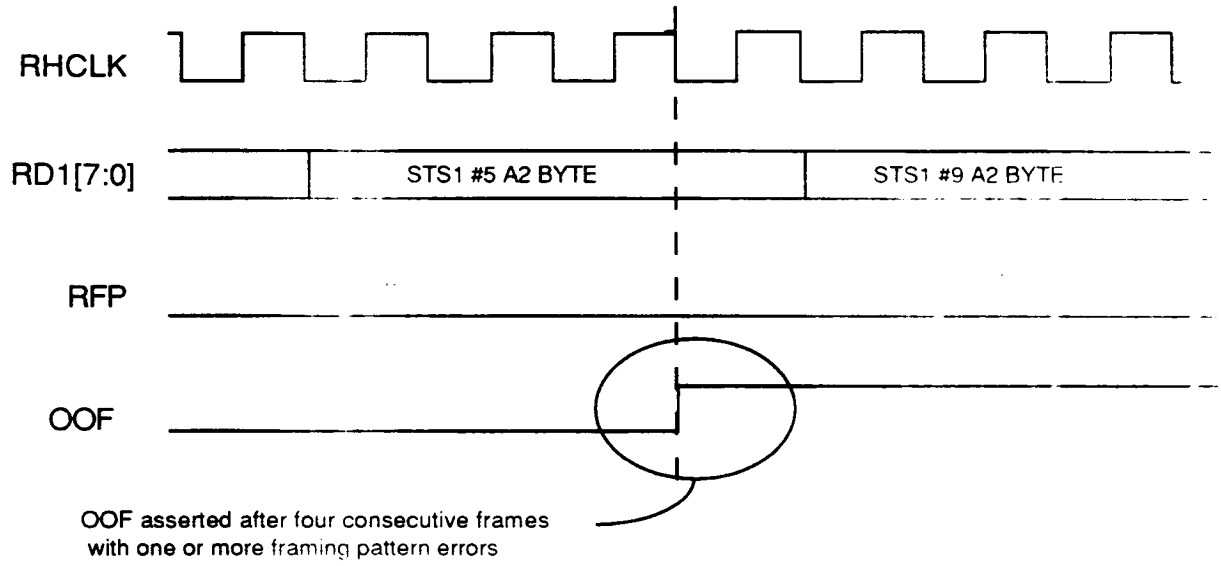


Figure 5 In Frame Declaration

The In-frame Declaration timing diagram (Figure 5) shows the interaction between the frame detector in the Receive Section Overhead Processor (RSOP) and the upstream serial to parallel converter / pattern detector during frame

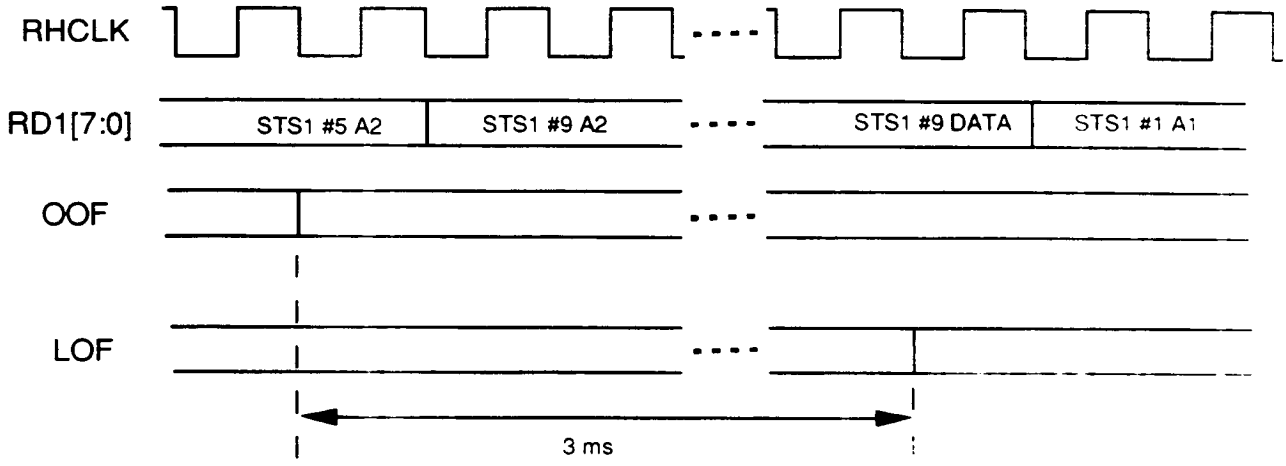
upstream serial to parallel converter / pattern detector during frame search. The internal frame pulse is asserted by the pattern detector during the first byte of the synchronous payload envelope, and initializes the Timing Block in RSOP. One frame (125 µs) later, the framing bytes in the STS12 stream are verified and in-frame is declared when the OOF output goes low. The RFP output is now synchronized to the new frame frame alignment.

Fig. 6 Out of Frame Declaration



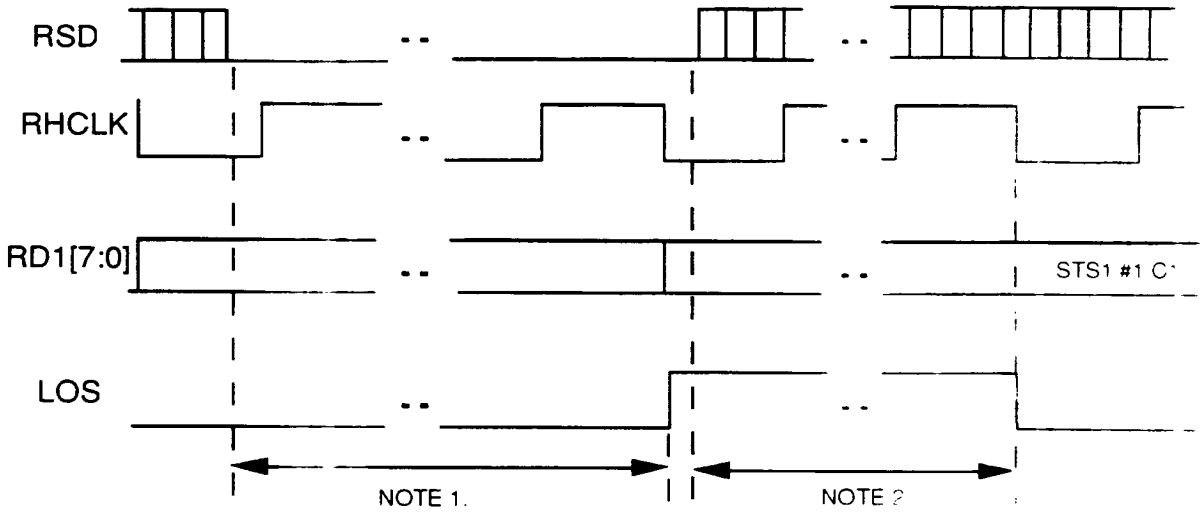
The out of frame detection timing diagram (Figure 6) shows the assertion of OOF upon the detection of framing pattern errors in the previous four consecutive frames. The pattern detector in the Serial to Parallel converter initiates a search for frame when OOF is high. Once it has found frame, the RSOP block verifies the frame alignment as shown in figure 5.

Fig. 7 Loss of Frame Assertion / Deassertion



The assertion of the Loss of Frame, shown in Figure 7, is the result of an integration of the OOF state. OOF being continually asserted / deasserted for 3 ms after a transition will assert / deassert LOF.

Fig. 8 Loss of Signal Assertion / Deassertion

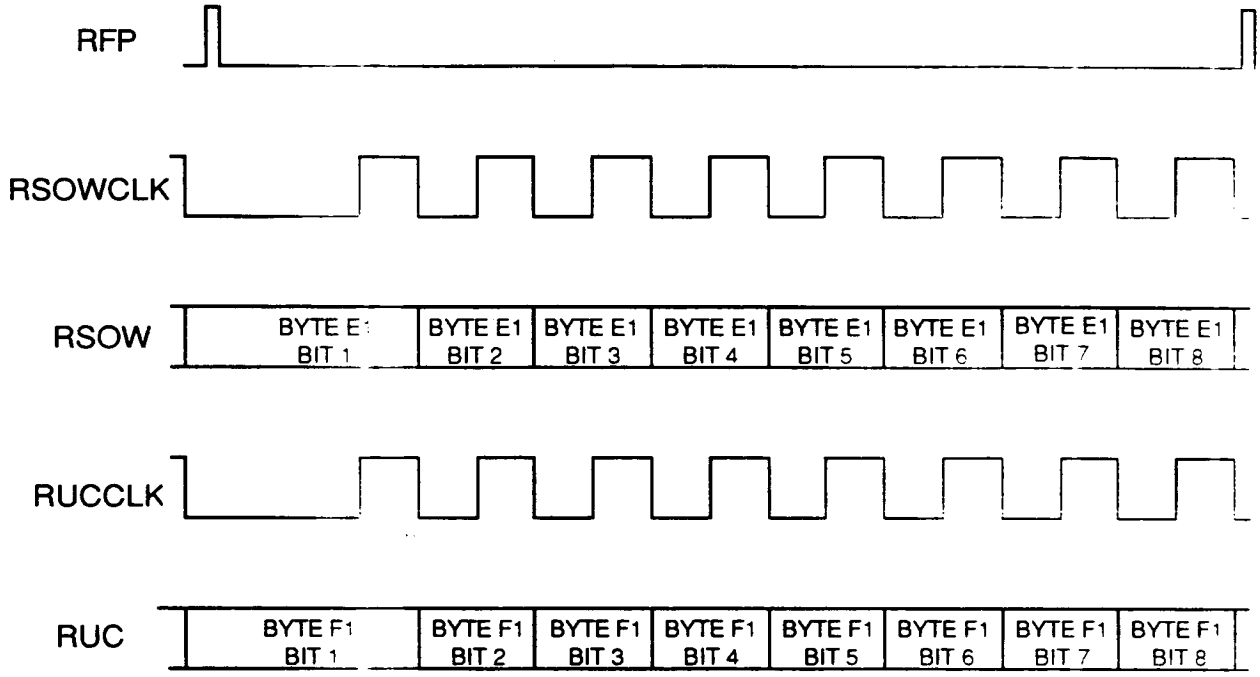


NOTES: 1. LOS is asserted after ~ 20 µs of all zero

2. LOS is deasserted after two valid framing patterns and no violating consecutive all zeros periods

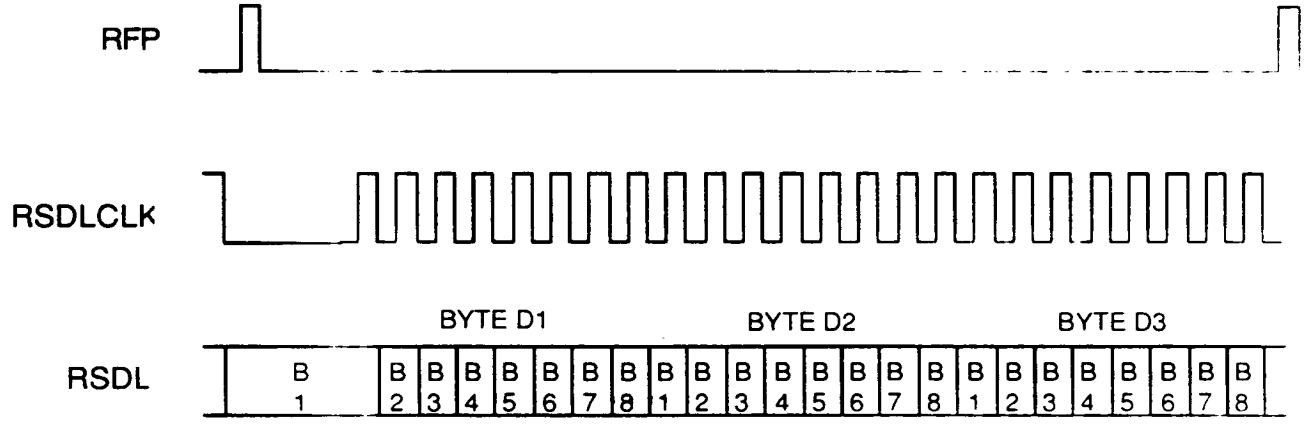
The Loss of Signal Assertion/Deassertion timing diagram (Figure 8) shows the operation of the LOS output. LOS is asserted after observing a violating period of consecutive all zeros in the RSD stream. A violating period is 20 ± 2.5 µs of consecutive all zeros bytes for STS-12 line rates. LOS is deasserted when two consecutive valid frame alignment patterns have been detected, and during the intervening time no violating periods of consecutive all zeros bytes were detected.

Fig. 9 Receive Section Order Wire and User Channel Extraction.



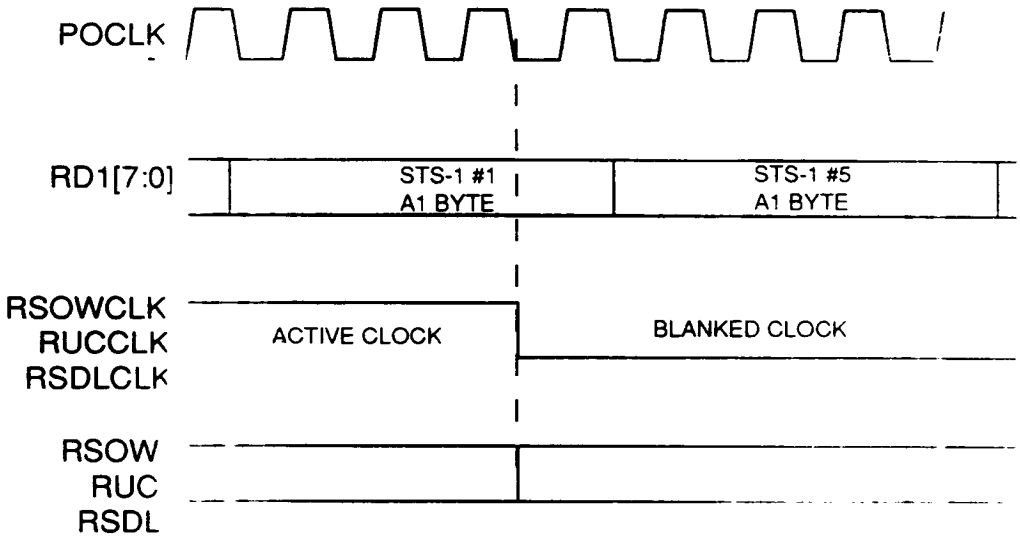
The Order Wire and User Channel Extraction timing diagram (Figure 9) shows the relationship between the RSOW and RSUC serial data outputs and their associated clocks, RSOWCLK and RUCCLK. Note that the timing of these signals is based on a 72 kHz, 50% duty cycle clock, that is gapped to produce a 64 kHz nominal rate that is aligned with the STS-N frame as shown in the Order Wire, User Channel, Data Link Alignment timing diagram (Figure 11).

Fig. 10 Receive Section Data Link Extraction.



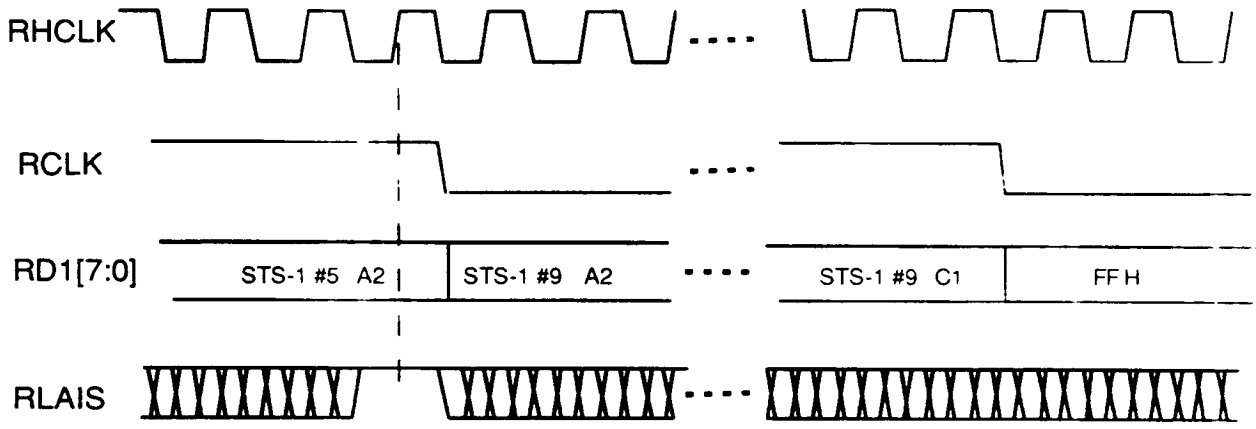
The Data Link Extraction timing diagram (Figure 10) shows the relationship between the DL serial data output and its associated clock, DLCLK. Note that the timing of this signal is based on a 216 kHz, 50% duty cycle clock, that is gapped to produce a 192 kHz nominal rate that is aligned with the STS-N frame as shown in the Order Wire, User Channel, Data Link Alignment timing diagram (Figure 11).

Fig. 11 Receive Section Order Wire and User Channel Alignment.



The clocks for the Receive Section Overhead Order wire, User Channel, and Data Link outputs are blanked for at least the first 90 byte row of the synchronous payload envelope. This blanking starts as shown in Figure 11. Each clock starts again at the appropriate time during the frame, as previously shown. The Receive Frame Pulse (RFP) occurs during this blanked period, and should be used to synchronize external circuitry to the byte boundaries of the overhead data.

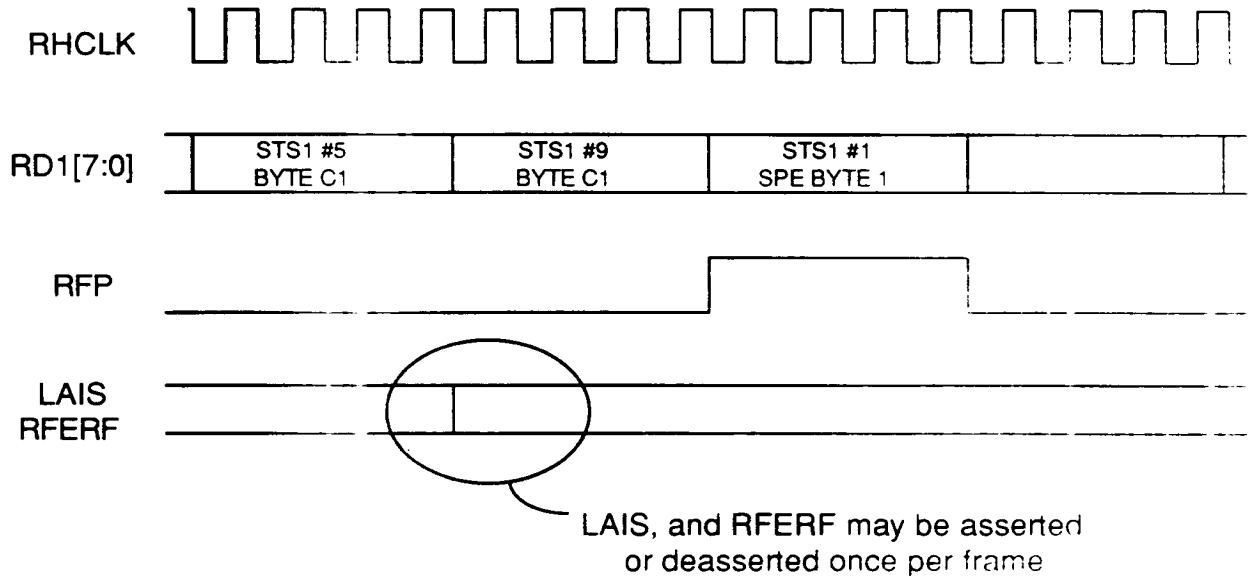
Fig. 12 RLAIS Insertion



The Receive Line AIS timing diagram, Figure 12. shows the RLAIS input sampled once per frame by the rising edge of RHCLK. If RLAIS is sampled high, line AIS is inserted into the same frame by forcing the line overhead and synchronous payload envelope bytes to FF H. The Line Overhead Processor will detect the AIS signal in the line overhead envelope and assert its LAIS output. The RD1 through RD4 outputs will be forced to FF H.

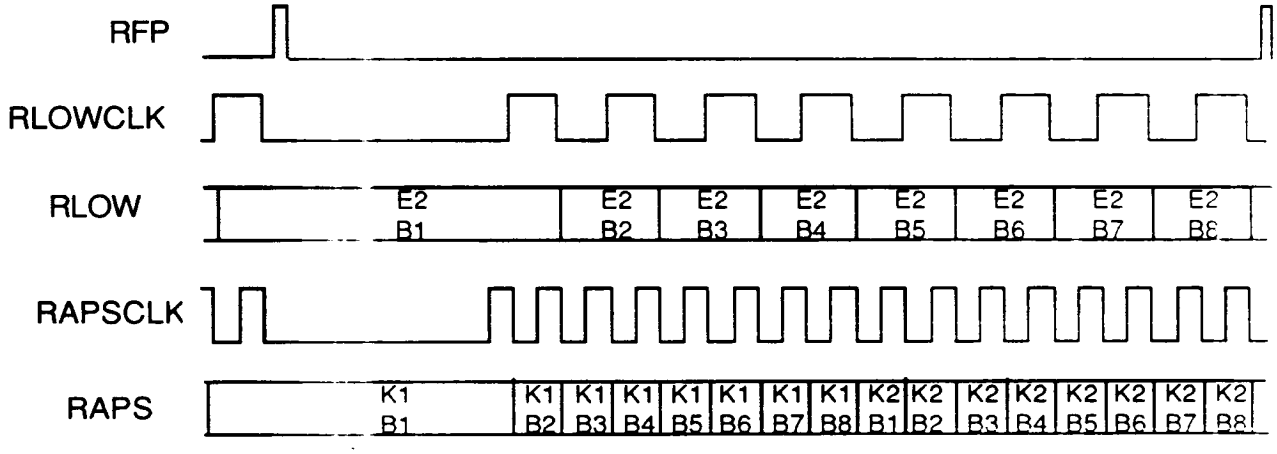
Receive Line Overhead Timing Characteristics

Fig. 13 FERF and LAIS Declaration and Removal



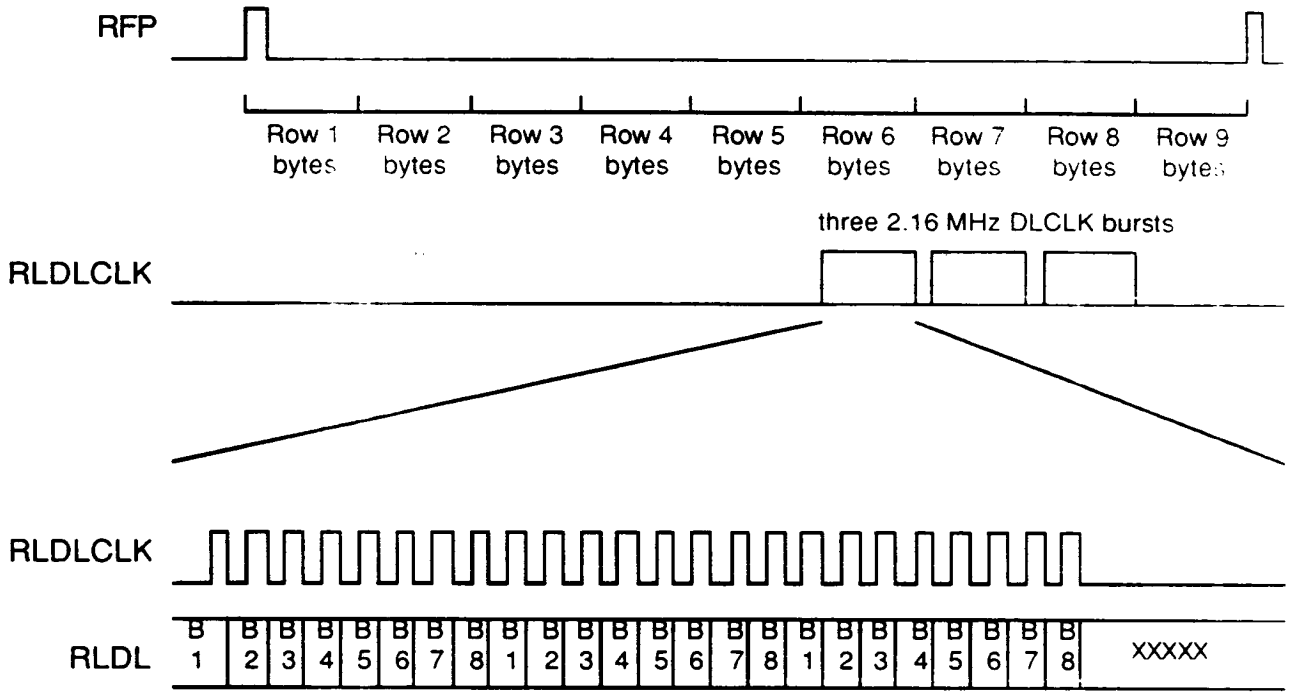
The RFERF and LAIS Declaration and Removal timing diagram (Figure 13) shows the assertion and deassertion timing of outputs RFERF and LAIS. RFERF or LAIS may be declared, or removed once per frame as indicated.

Fig. 14 Receive Line Order Wire and APS Extraction



The Order Wire and APS Extraction timing diagram (Figure 14) shows the relationship between the OW and APS serial data output and their associated clocks, RLOWCLK and RAPSCLK respectively. RLOWCLK is a 72 kHz, 50% duty cycle clock, that is gapped to produce a 64 kHz nominal rate and is aligned with RFP as shown in the timing diagram. RAPSCLK is a 144 kHz, 50% duty cycle clock, that is gapped to produce a 128 kHz nominal rate and is aligned with RFP as shown above.

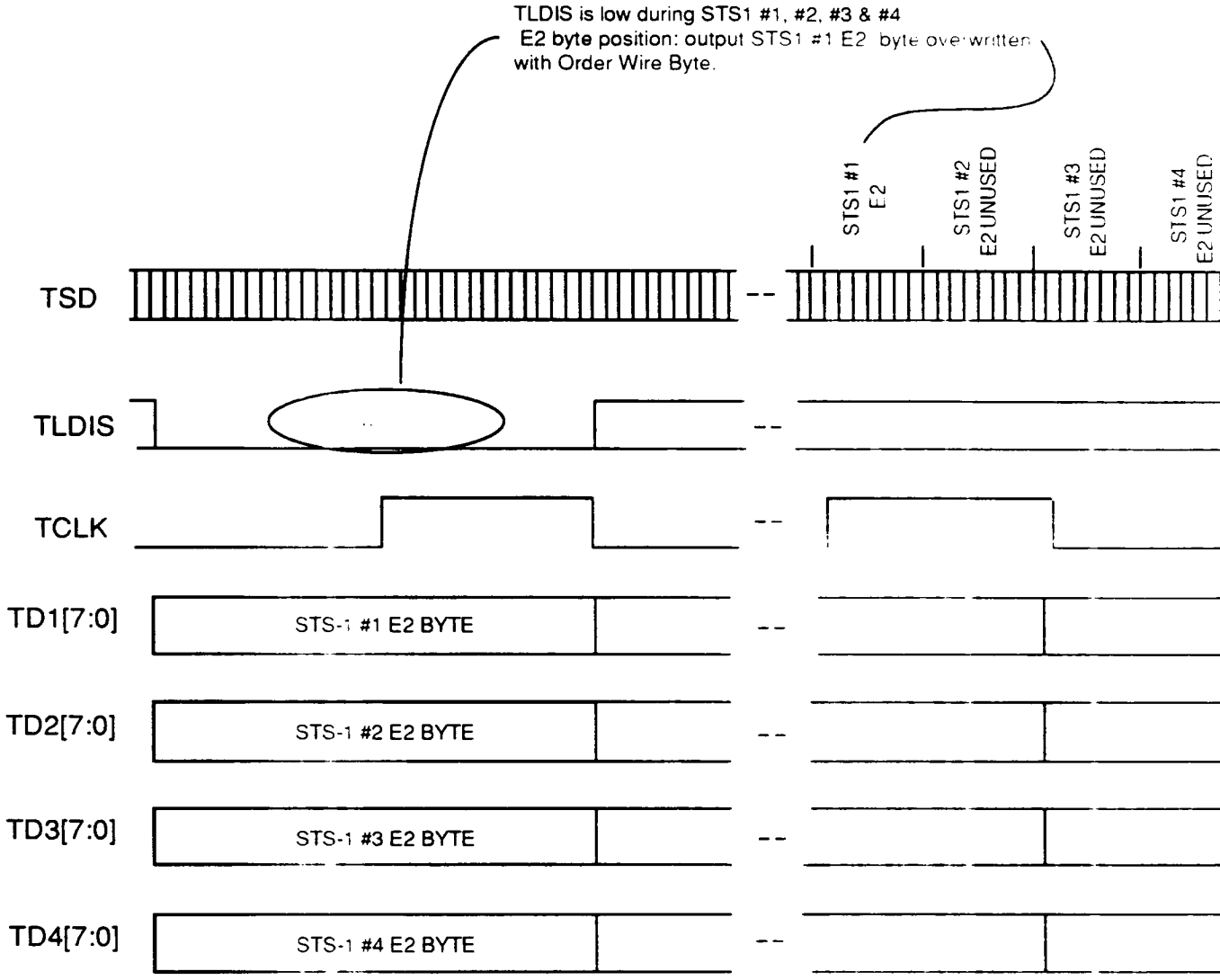
Fig. 15 Receive line Data Link Extraction



The Data Link Extraction timing diagram (Figure 15) shows the relationship between the RLDL serial data output, its associated clock, RLDLCLK and RFP. RLDLCLK is a 2.16 MHz, 67%/33% (high)/(low) duty cycle clock, that is gapped to produce a 576 kHz nominal rate that is aligned with RFP as shown in the timing diagram. RLDL is updated on the falling RLDLCLK edge.

Transmit Line Overhead Timing Characteristics

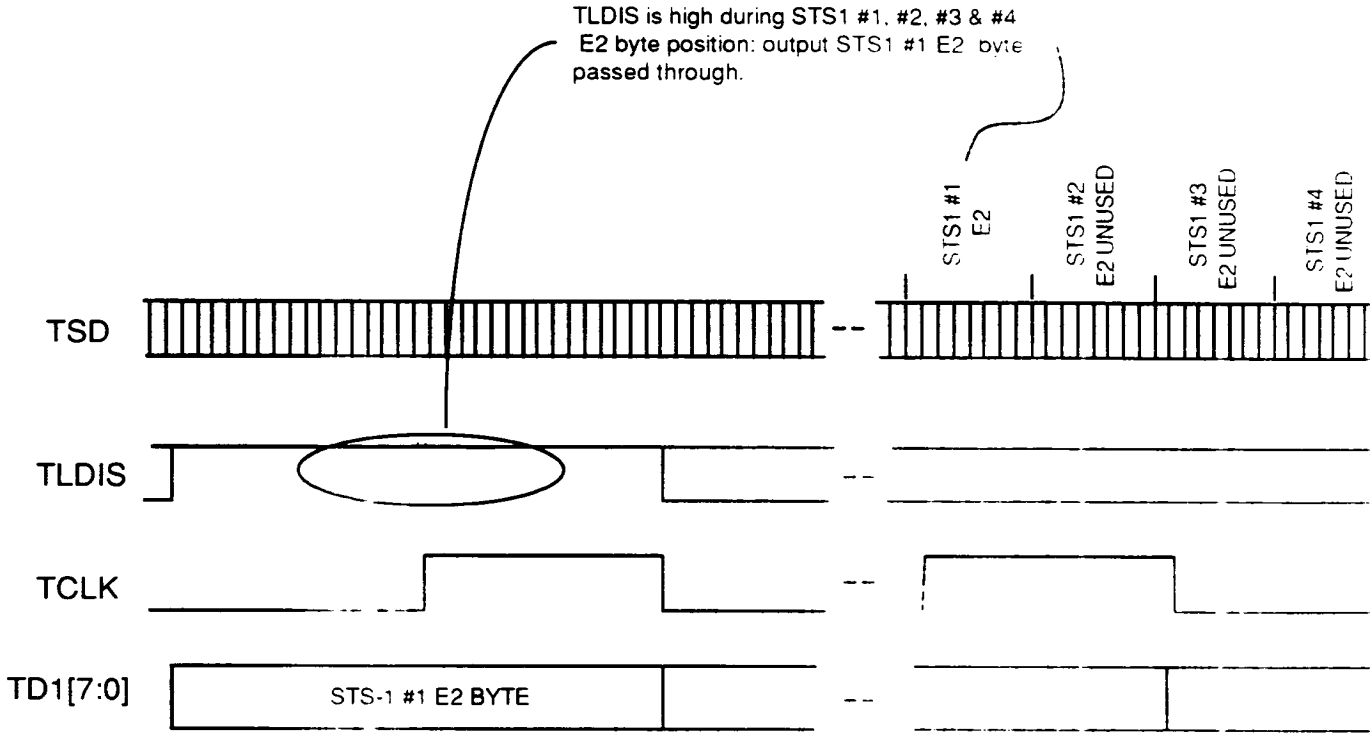
Fig. 16 Line Layer Overwrite Enabled



The Line Layer Overwrite Enabled timing diagram (Figure16) illustrates the operation of the Transmit Line Overhead Processor when line overhead bytes overwrite their allocated time slots in the data stream. The example diagram shows input DIS sampled low during a line order wire channel byte on the Internal Transmit Line Bus. It is assumed that the DOW bit in the Control Register is low, thereby enabling order wire byte overwrite. The line order wire channel byte in the TSD stream is written with the byte previously shifted in on input TLOW by the TLOWCLK

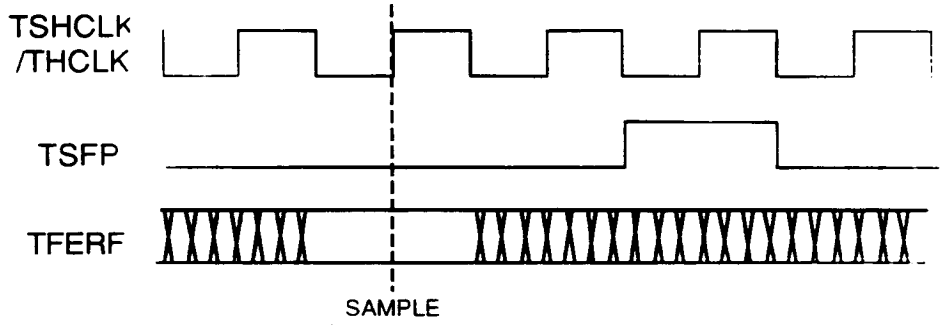
clock. For information on the alignment of the internal Transmit Line Bus with the frame pulses, see Figure 18.

Fig. 17 Transmit Line Layer Overwrite Disabled



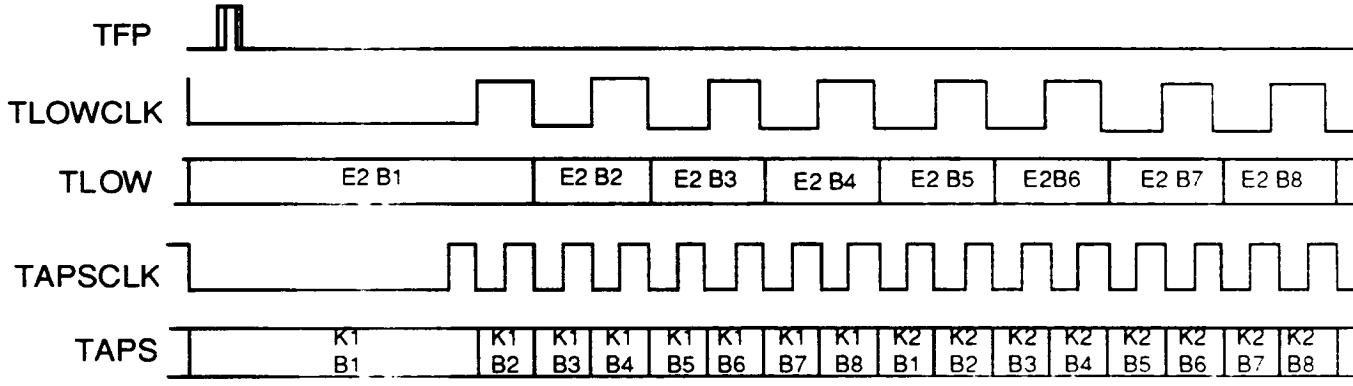
The Transmit Line Layer Overwrite Disabled timing diagram (Figure 17) illustrates the operation of the Transmit Line Overhead Processor when line overhead bytes do not overwrite their allocated time slots. The example diagram shows input TLDIS sampled high during a line order wire channel byte position of the Internal Transmit Line Bus stream. The line order wire channel byte of the TSD stream is the same as the value input at the associated STS-3 port, TD2[7:0]. For information on the alignment of the internal Transmit Line Bus with the frame pulses, see Figure 18.

Fig. 18 FERF Insertion



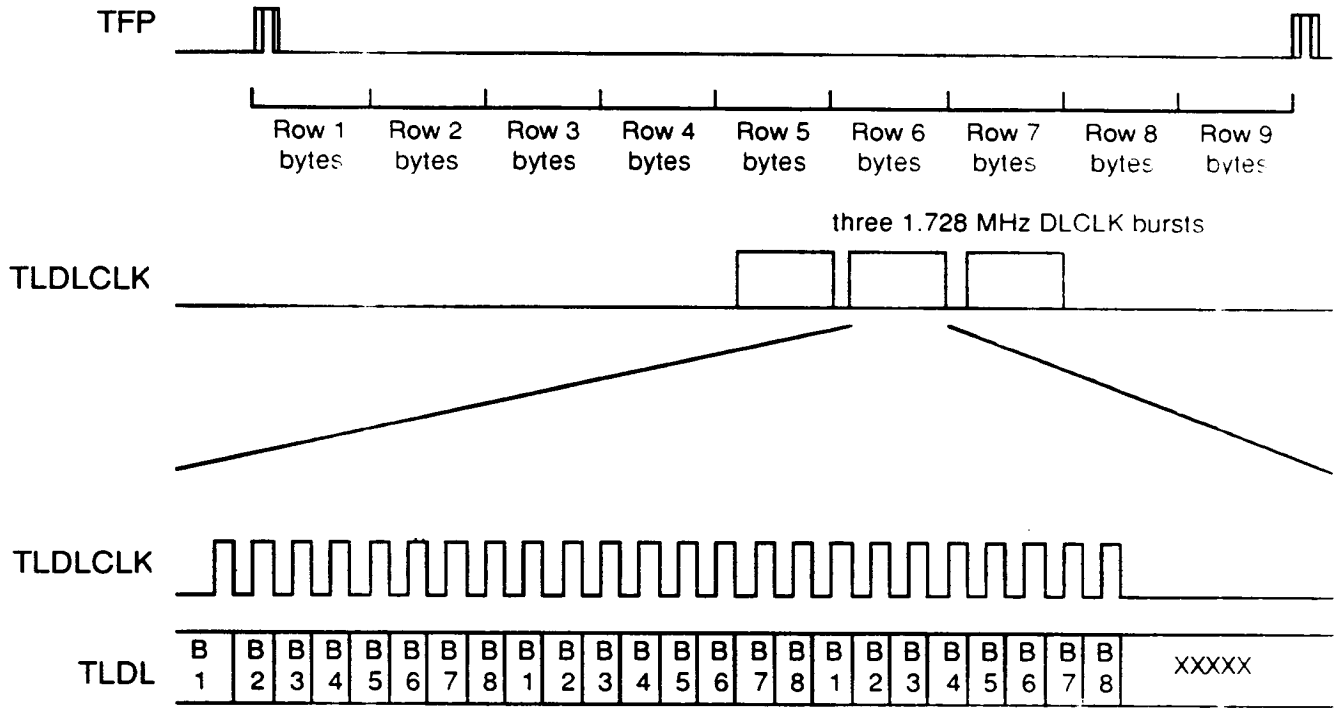
The FERF Insertion timing diagram (Figure 18) shows the TFERF input sampled once per frame. It illustrates TFERF sampled high by the rising edge of THCLK one and a half THCLK cycles before the rising edge of TSFP. If FERF is high, the Far End Receive Failure (FERF) indication is inserted in the line overhead of the STS-12 stream.

Fig. 19 Transmit Line Order Wire and APS Insertion



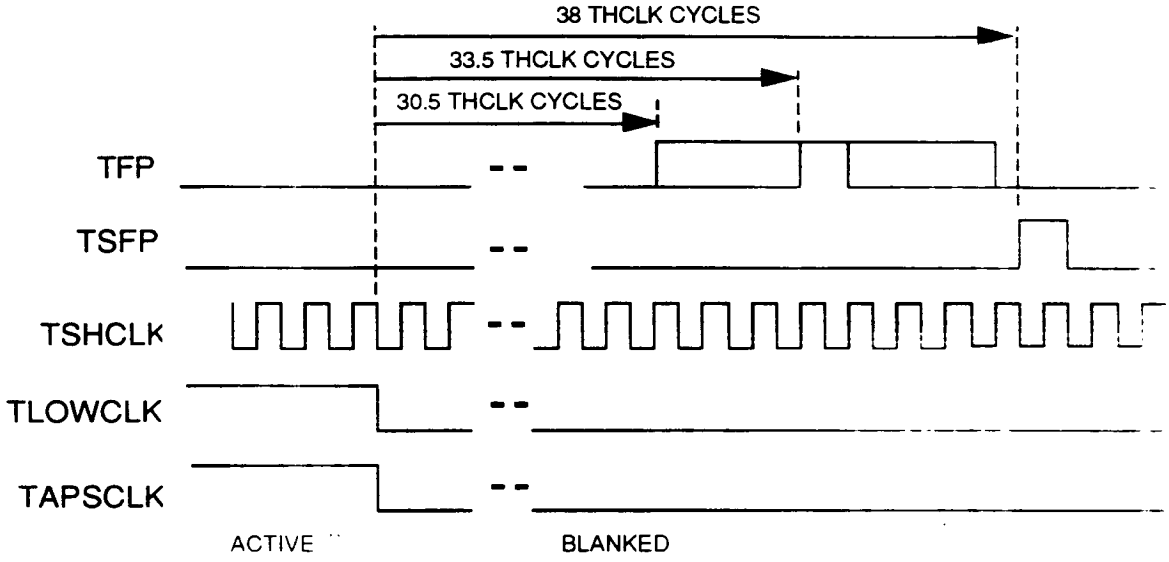
The Transmit Line Order Wire and APS Insertion timing diagram (Figure 19) shows the relationship between the TLOW serial data input and its associated clock, TLOWCLK, and the TAPS serial data input, and its associated clock, TAPSCLK. The timing of TLOWCLK (TAPSCLK) is based on a 72 kHz (144 kHz), 50% duty cycle clock, that is gapped to produce a 64 kHz (128 kHz) nominal rate that is aligned with TFP as shown in this timing diagram.

Fig. 20 Transmit Line Data Link Insertion



The Data Link Extraction timing diagram (Figure 20) shows the relationship between the TLDL serial data input, its associated clock, TLDLCLK and TFP. TLDLCLK is a 1.728 MHz, 50% duty cycle clock, that is gapped to produce a 576 kHz nominal rate that is aligned with TFP as shown in the timing diagram. TLDL is sampled on the rising TLDLCLK edge

Fig. 21 TLOWCLK and TAPSCLK Alignment



The TLOWCLK and TAPSCLK alignment timing diagram (Figure 21) shows the relationship between the frame pulses, TLOWCLK, and TAPSCLK. The Order Wire and APS clocks are blanked for the first SPE row, and return to the active state as shown previously. The falling edges of TLOWCLK and TAPSCLK are aligned to the falling THCLK edge.

Transmit Section Overhead Timing Characteristics

Fig. 22 Transmit Section Internal Bus Alignment

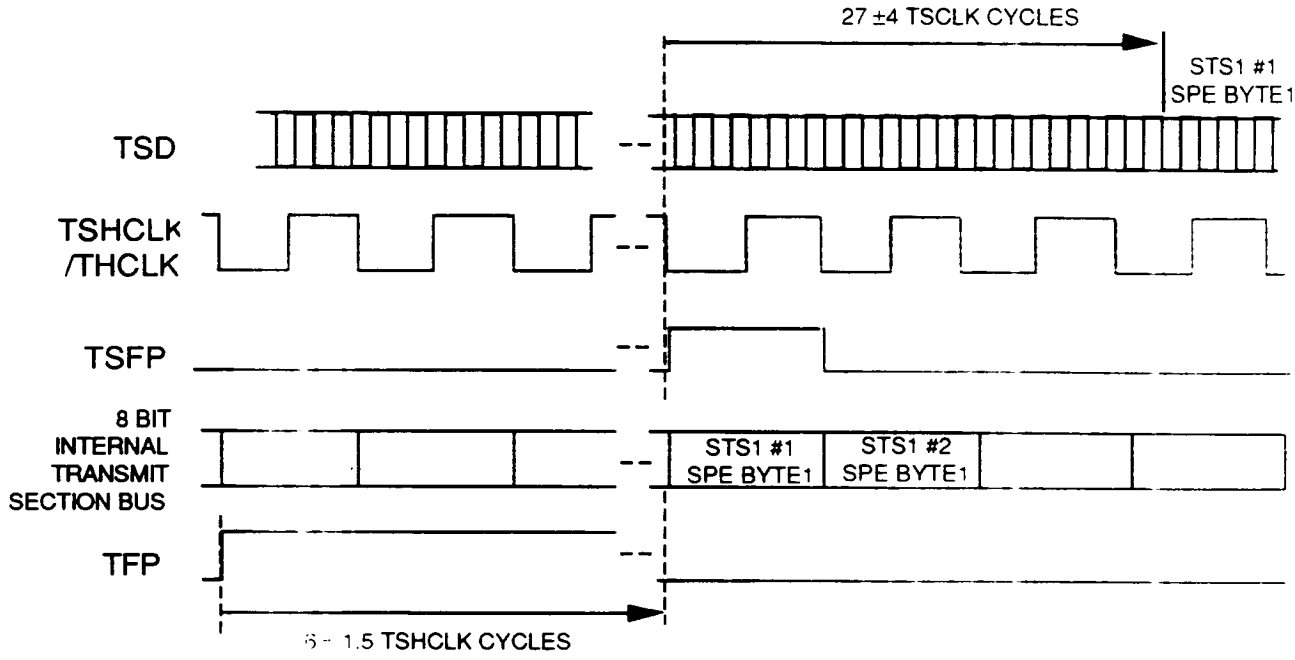
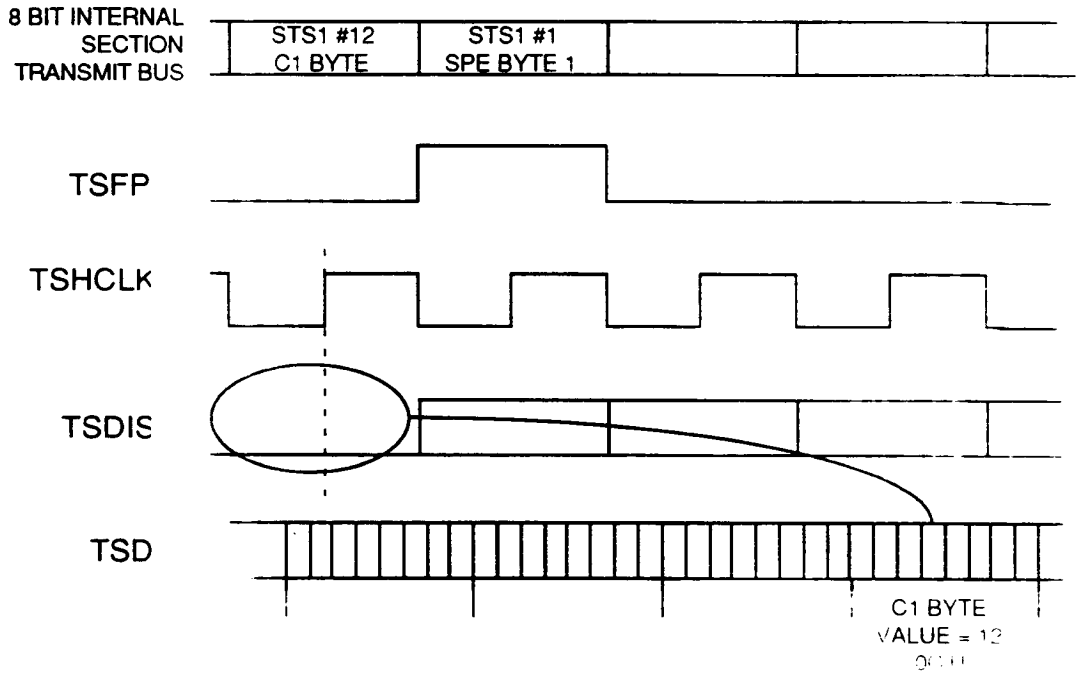


Figure 22 shows the Transmit Section Frame Pulse, (TSFP) high during the first SPE byte of the internal transmit section 8 bit bus, which connects the line overhead processor to the section overhead processor. This frame pulses is required to align the TSDIS inputs to the internal bus timing. The TFP STS-3 frame pulse input precedes TSFP by 6 ± 1.5 section byte clock cycles, (TSHCLK cycles). Output data from TSD appears 27 ±4 transmit serial clock (TSCLK) cycles, or 3.375 ± 0.5 TSHCLK cycles after it passes through the internal transmit section bus

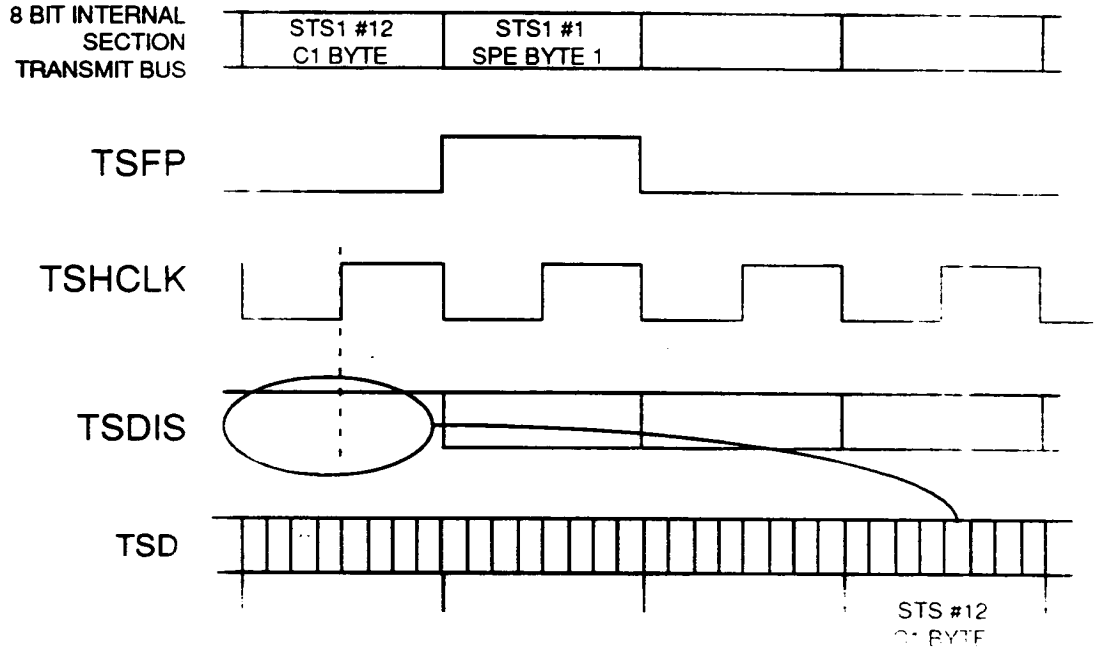
Fig. 23 Transmit Section Layer Overwrite Enabled



DIS is low during C1 byte position. STS1 #N
C1 byte value is overwritten with 'N' hexadecimal

The Transmit Section Layer Overwrite Enable timing diagram (Figure 23.) illustrates the section layer bytes overwriting the data in the allocated time slots. In the example diagram, TSDIS is sampled low while the C1 identity byte for STS1 #12 is on the internal transmit section data bus. Assuming that the DC1 bit in the control register is low, 12 (0C H) is written into this time slot before being serialized and output at TSD.

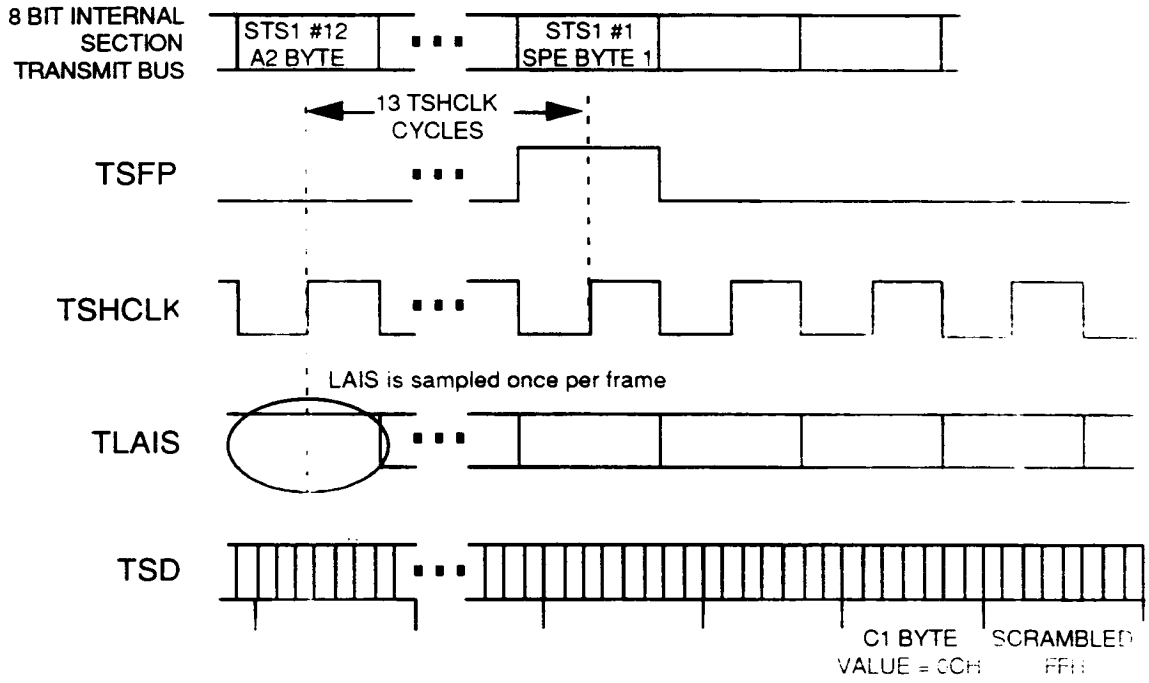
Fig. 24 Transmit Section Layer Overwrite Disable



DIS is high during C1 byte position: STS1 #12
C1 byte value is not overwritten

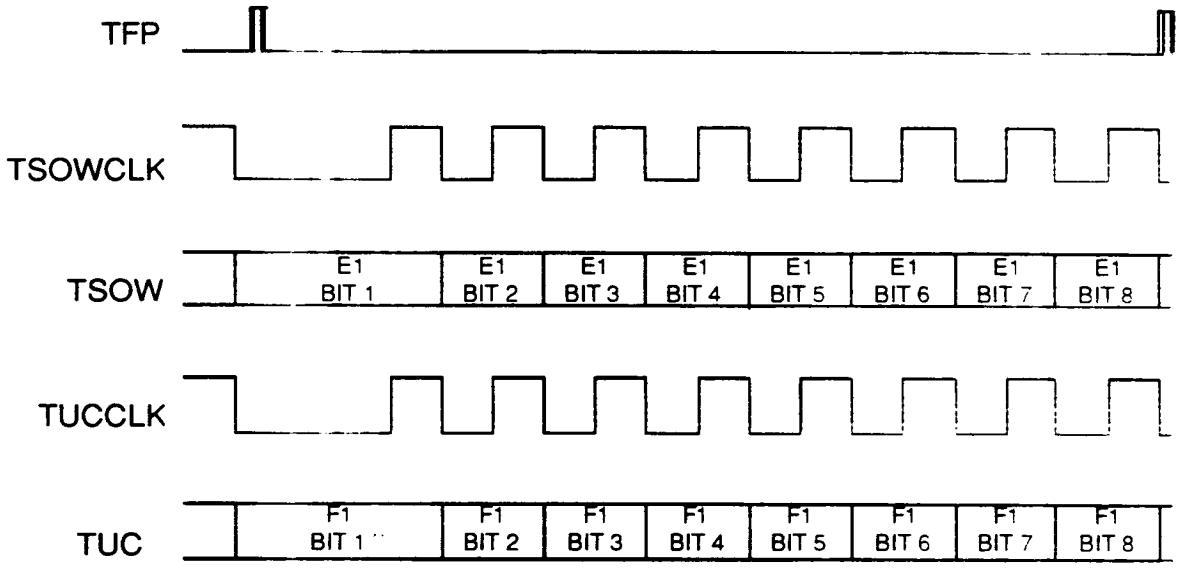
The Transmit Section Layer Overwrite Disable timing diagram (Figure 24) illustrates the STS1 #12 C1 identity byte being passed through to TSD without being altered TSDIS is sampled high during the STS1 #12 C1 time slot of the internal transmit section bus.

Fig. 25 Transmit Line AIS Insertion



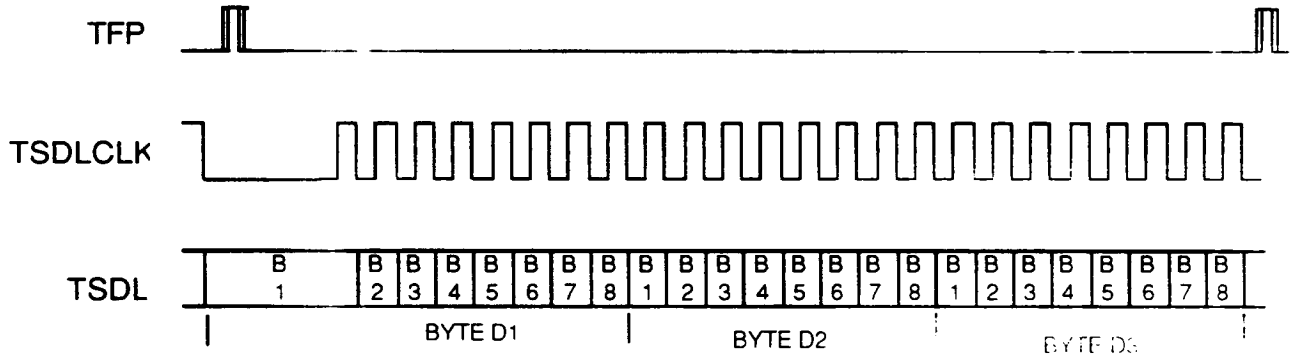
The Transmit Line AIS Insertion timing diagram (Figure 25) Shows the TLAIS input sampled once per frame. If LAIS is sampled high, line AIS is inserted by forcing all subsequent bytes, except the section layer overhead bytes, to FF H. If TLAIS is sampled low, then data is passed through to the output unaltered. Note that at the TSD output , any byte in an SPE slot will be scrambled.

Fig. 26 Transmit Section Order Wire and User Channel Insertion



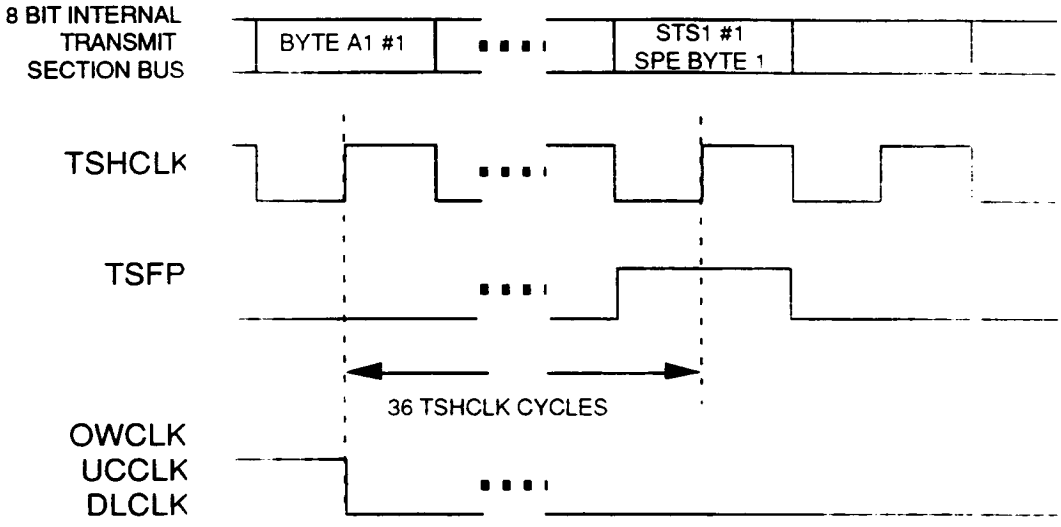
The Order Wire and User Channel Insertion diagram (Figure X) shows the relationship between the TSOW and TUC serial data inputs and their associated clocks, TSOWCLK and TUCCLK. Note that the timing of these two signals is based on a 72 kHz, 50 % duty cycle clock, that is gapped to produce a 64 kHz nominal rate. TFP is high during the gap in the clocks, as shown in the timing diagram.

Fig. 27 Transmit Section Data Link Insertion



The Data Link Insertion timing diagram (Figure 27) shows the relationship between the TSDL serial data input and its associated clock, TSDLCLK. Note that the timing of this signal is based on a 216 kHz, 50 % duty cycle clock, that is gapped to produce a 192 kHz nominal rate. TFP is high during the gap in the clock, as shown in the timing diagram.

Fig. 28 TLOWCLK, TUCCLK, and TSDLCLK Alignment



The TSOWCLK, TUCCLK, and TSDLCLK clock alignment diagram (Figure 26) shows the alignment of the last falling edge of these clocks before they enter the steady state, gapped portion of their cycle. This edge occurs on the rising edge of TSHCLK, 36 TSHCLK clock cycles before the centre of the TSFP frame pulse. For more information about the relationship of TSFP to TFP, see figure 18

AC TIMING CHARACTERISTICS

(Ta = 0 C to Tc = +70 C, VDD = 5V ± 10%
VEE = -5.2V ± 10% VTT = -2V± 5%)

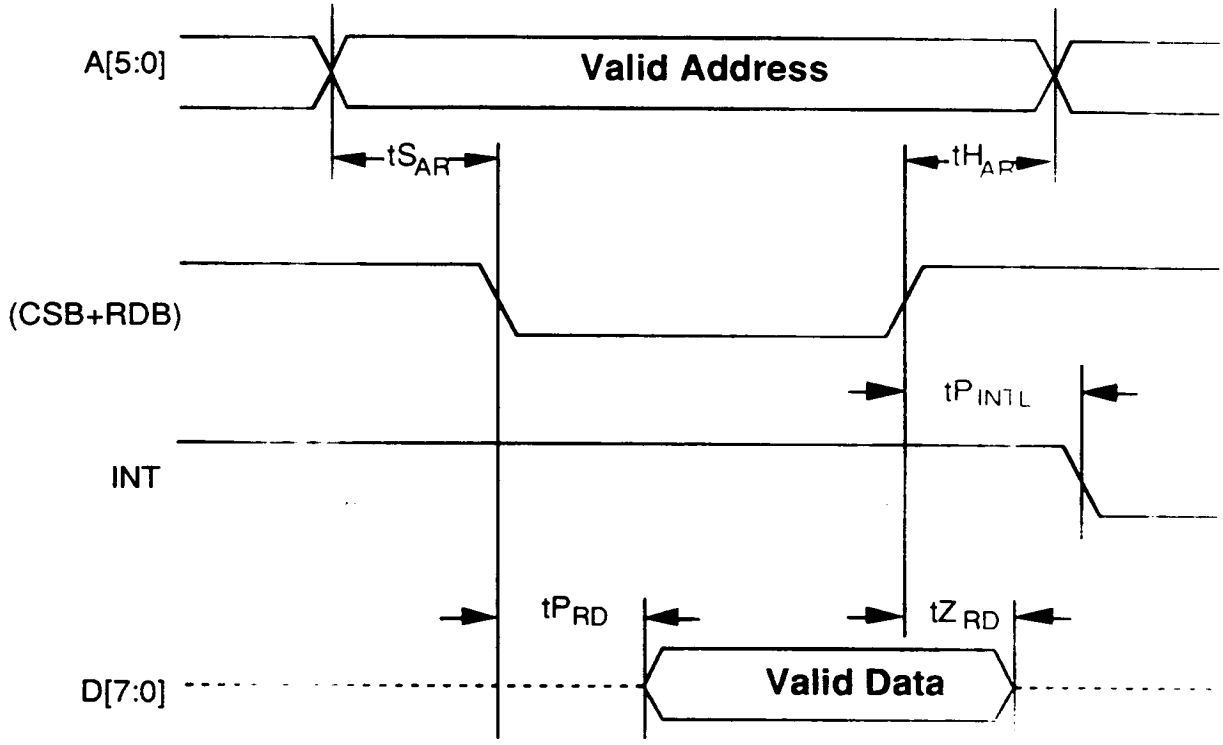
Microprocessor Interface Timing Characteristics

(T_a = 0°C to T_c+70°C, V_{DD} = 5 V ±10%)

Microprocessor Interface Read Access (Fig. 29)

Symbol	Parameter	Min	Max	Units
tS_{AR}	Address to Valid Read Set-up Time	20		ns
tH_{AR}	Address to Valid Read Hold Time	20		ns
tP_{RD}	Valid Read to Valid Data Propagation Delay		80	ns
tZ_{RD}	Valid Read Deasserted to Output Tri-state		20	ns
tP_{INTL}	Valid Read Deasserted to INT Low		50	ns

Fig. 29 Microprocessor Interface Read Access Timing



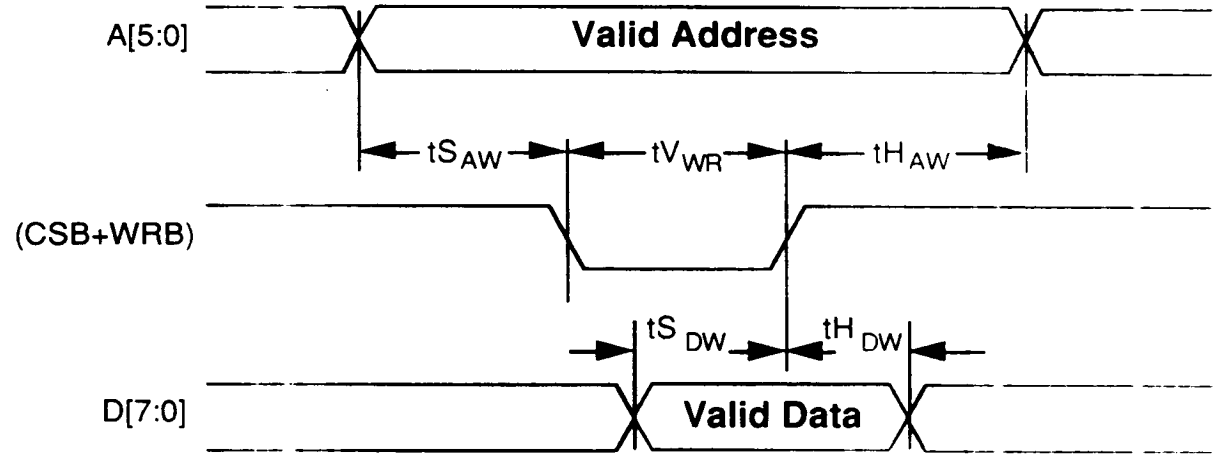
Notes on Microprocessor Interface Read Timing:

1. Output propagation delay time is the time in nanoseconds from the 50% point of the reference signal to the 30% or 70% point of the output.
2. Maximum output propagation delays are measured with a 100 pF load on the Microprocessor Interface data bus, (D[7:0]).
3. A valid read cycle is defined as a logical OR of the CSB and the RDB signals.
4. Microprocessor interface timing applies to normal mode register accesses only.

Microprocessor Interface Write Access (Fig. 30)

Symbol	Parameter	Min	Max	Units
tS_{AW}	Address to Valid Write Set-up Time	20		ns
tS_{DW}	Data to Valid Write Set-up Time	20		ns
tH_{DW}	Data to Valid Write Hold Time	20		ns
tH_{AW}	Address to Valid Write Hold Time	20		ns
tV_{WR}	Valid Write Pulse Width	40		ns

Fig. 30 Microprocessor Interface Write Access Timing



Notes on Microprocessor Interface Write Timing:

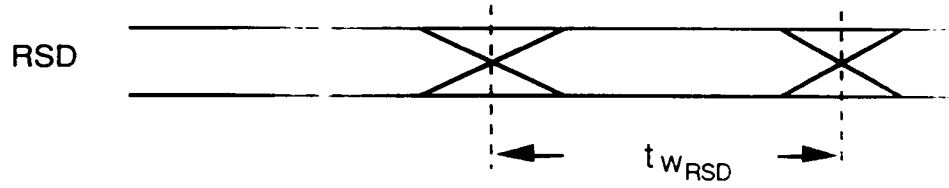
1. A valid write cycle is defined as a logical OR of the CSB and the WRB signals.
2. Microprocessor Interface timing applies to normal mode register accesses only.

STS-12 Input/Output Timing Characteristics

STS-12 Receive Serial Data Input Timing (Fig. 31)

Symbol	Description	Min	Max	Units
tW_{RSD}	RSD Pulse Width at 50% points Nom 1600 ps	1200	2000	ps
B_{RSD}	RSD Bit Rate Nom. 622.08 MHz	620	624	MBit/s

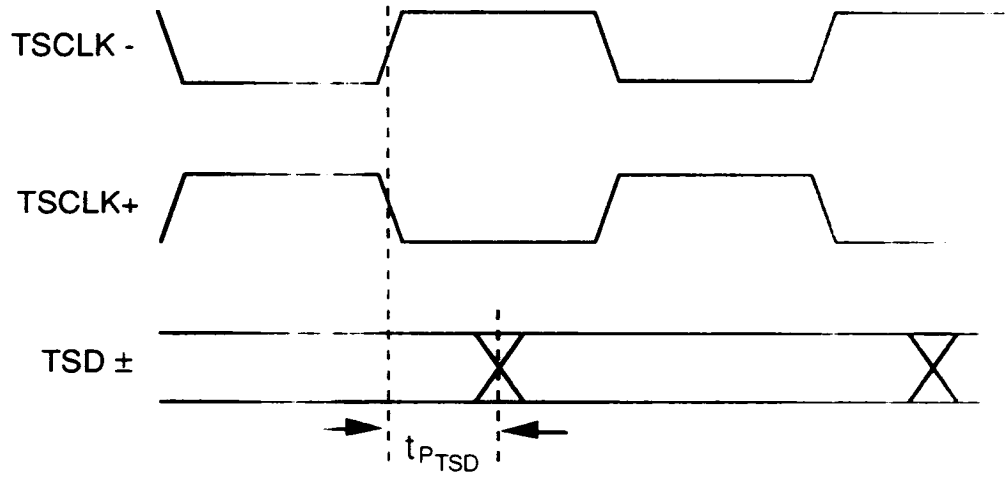
Fig. 31 STS-12 Receive Serial Data Input Timing



STS-12 Transmit Serial Data Output Timing (Fig. 32)

Symbol	Description	Min	Max	Units
tP_{TSD}	Propagation Delay from TSCLK Low to TSD Valid		500	ps
B_{TSD}	Bit rate of TSD output. Nom. 622.08 MHz	620	624	MBit/s

Fig. 32 STS-12 Transmit Serial Data Output Timing

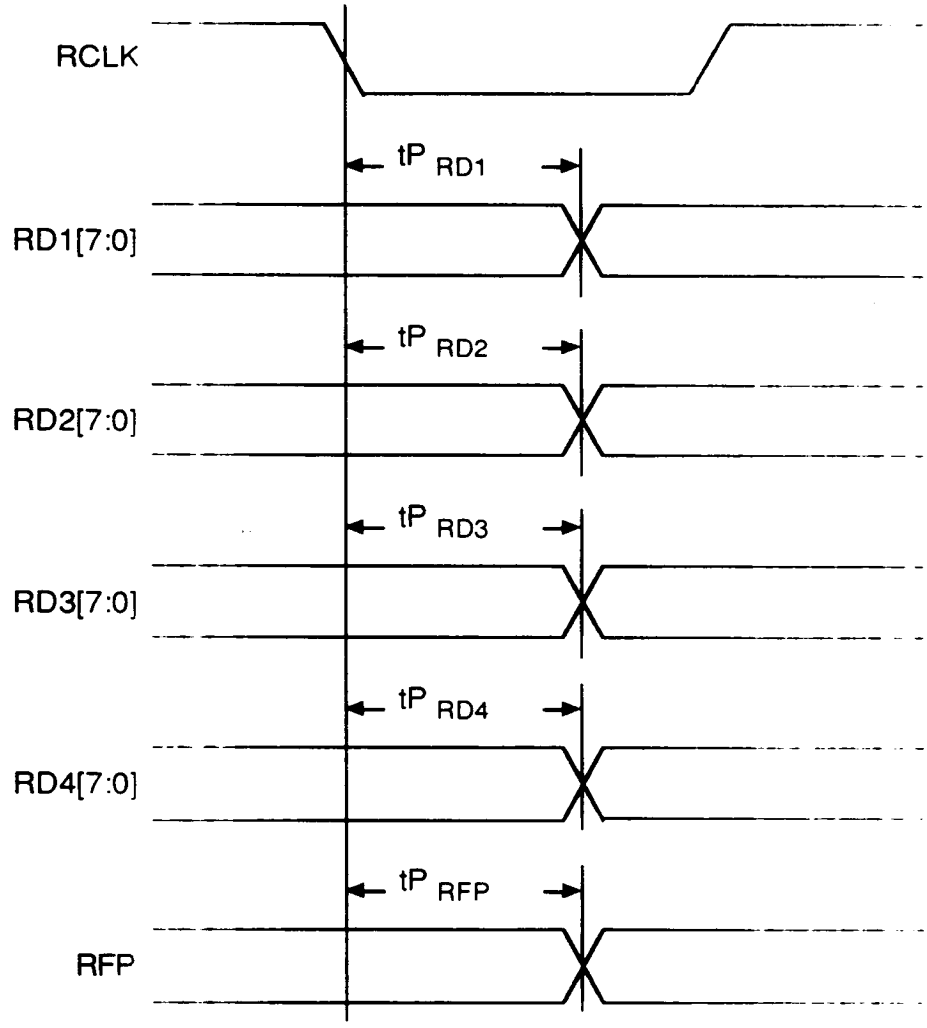


STS-3 Input/Output Timing Characteristics

STS-3 Receive Data Output Timing (Fig. 33)

Symbol	Description	Min	Max	Units
tP_{RD1}	RCLK Low to RD1 Valid Propagation Delay	2	10	ns
tP_{RD2}	RCLK Low to RD2 Valid Propagation Delay	2	10	ns
tP_{RD3}	RCLK Low to RD3 Valid Propagation Delay	2	10	ns
tP_{RD4}	RCLK Low to RD4 Valid Propagation Delay	2	10	ns
tP_{RFP}	RCLK Low to RFP Valid Propagation Delay	2	10	ns

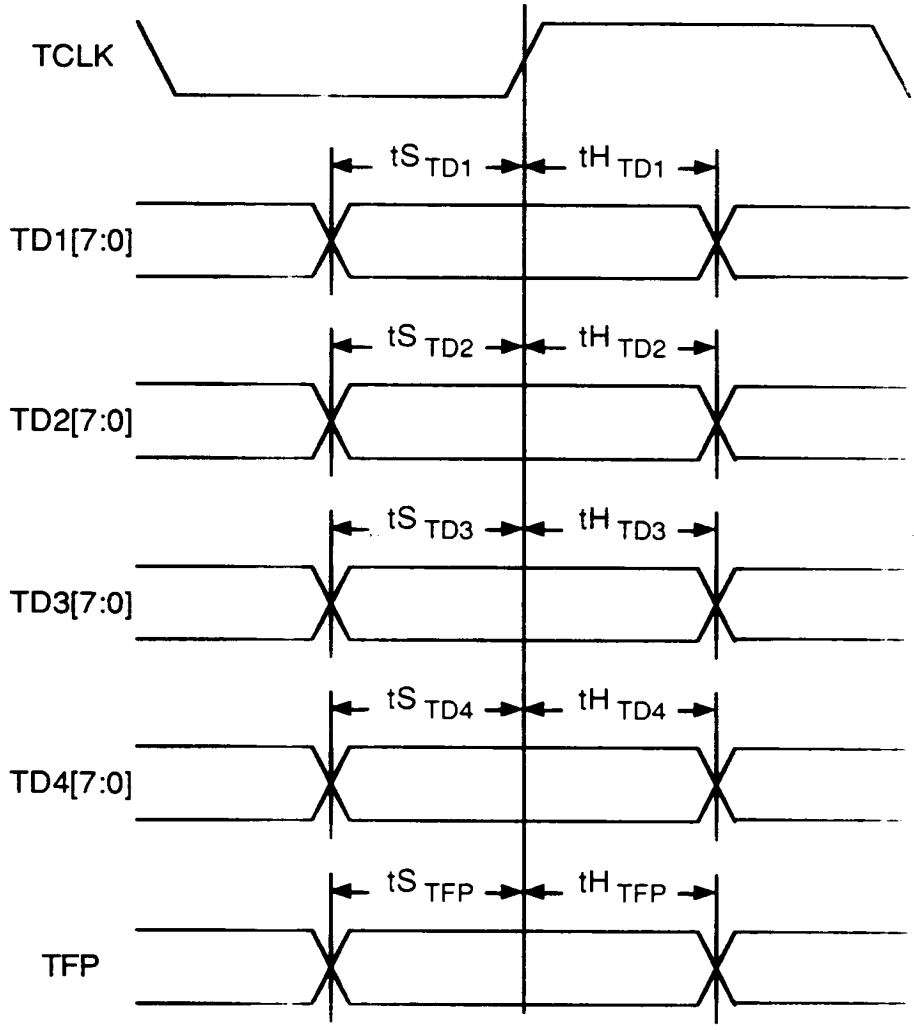
Fig. 33 STS-3 Receive Data Output Timing



STS-3 Transmit Data Input Timing (Fig. 34)

Symbol	Description	Min	Max	Units
	TCLK Frequency	19.37	19.50	
	TCLK Duty Cycle	33	67	%
tS_{TD1}	TD1 Set-up Time	6		ns
tH_{TD1}	TD1 Hold Time	6		ns
tS_{TD2}	TD2 Set-up Time	6		ns
tH_{TD2}	TD2 Hold Time	6		ns
tS_{TD3}	TD3 Set-up Time	6		ns
tH_{TD3}	TD3 Hold Time	6		ns
tS_{TD4}	TD4 Set-up Time	6		ns
tH_{TD4}	TD4 Hold Time	6		ns
tS_{TFP}	TFP Set-up Time	6		ns
tH_{TFP}	TFP Hold Time	6		ns

Fig. 34 STS-3 Transmit Data Input Timing

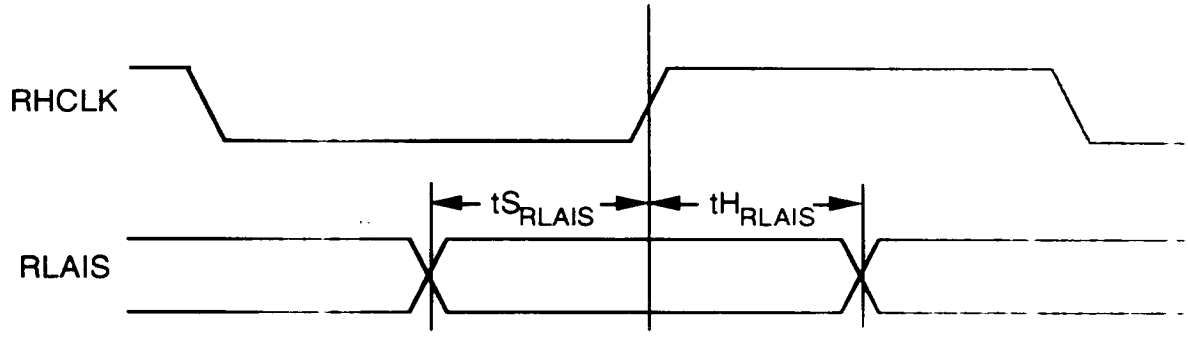


Receive Overhead Input/Output Timing Characteristics

Receive Section Overhead Input Timing (Fig. 35)

Symbol	Description	Min	Max	Units
tS_{RLAIS}	RLAIS Set up time to RHCLK	4		ns
tH_{RLAIS}	RLAIS Hold up time to RHCLK	5		ns

Fig. 35 Receive Section Overhead Input Timing



Receive Section Overhead Output Timing (Fig. 36)

Symbol	Description	Min	Max	Units
tP_{RSOW}	RSDLCLK Low to RSDL Valid	2	10	ns
tP_{RUC}	RSOWCLK Low to RSOW Valid	2	10	ns
tP_{SDL}	RUCCLK low to RUC Valid.	2	10	ns
tP_{LOF}	RHCLK low to LOF Valid.	-1	2	ns
tP_{LOS}	RHCLK low to LOS Valid.	-1	2	ns

Fig. 36a Receive Section Overhead Output Timing

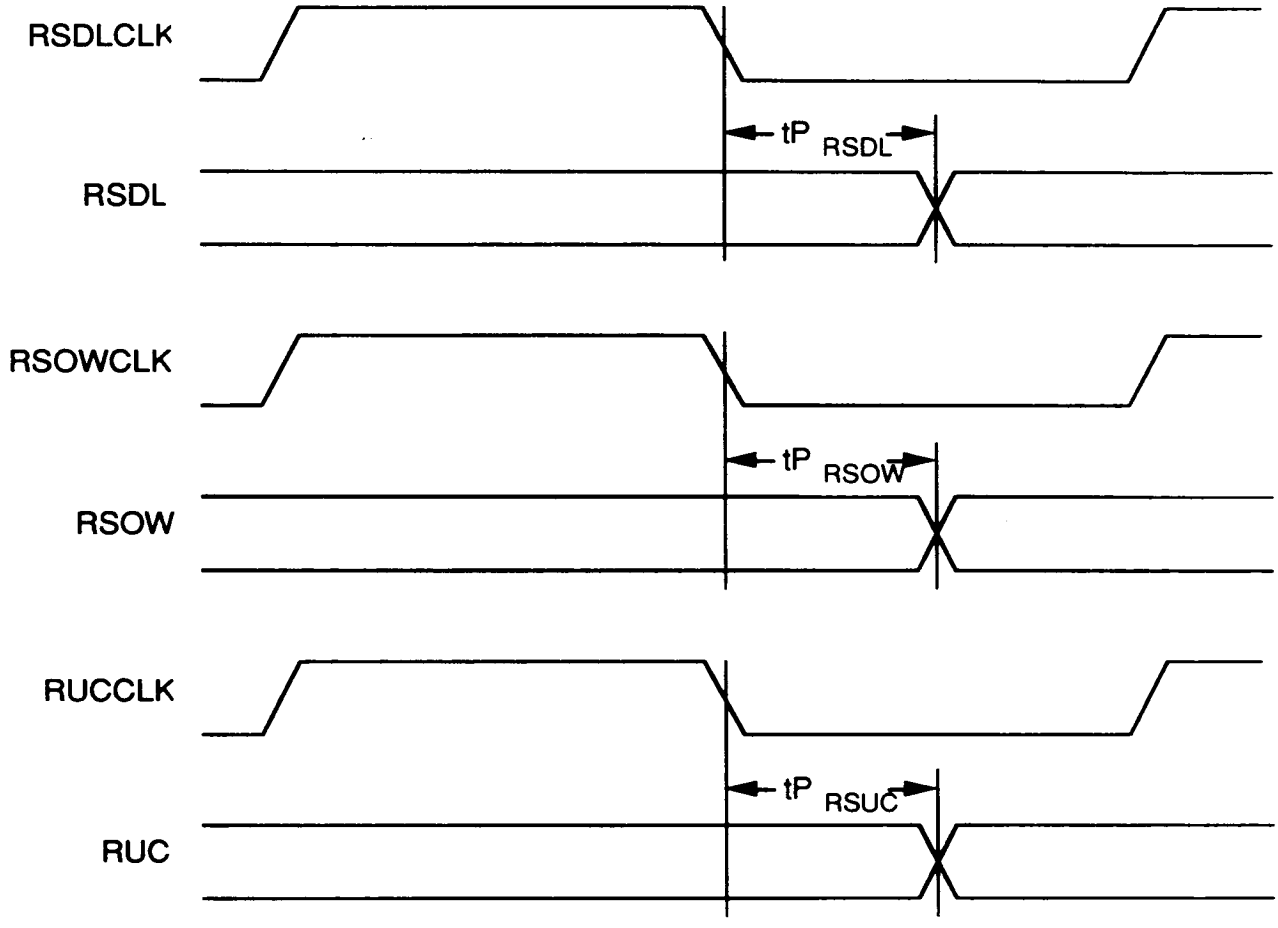
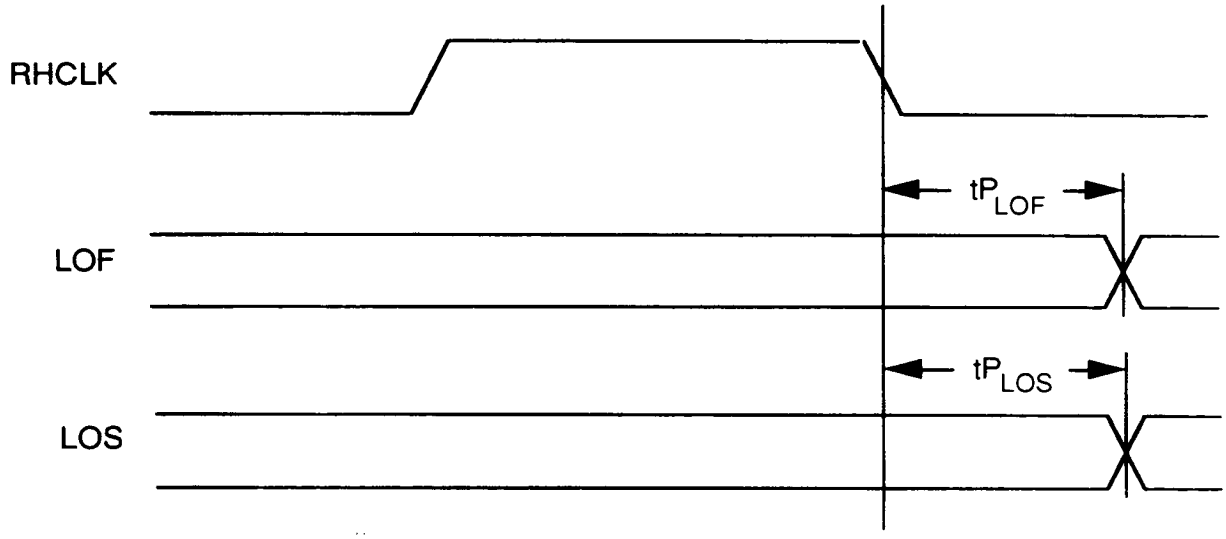


Fig. 36b Receive Section Overhead Output Timing



Receive Line Overhead Output Timing (Fig. 37)

Symbol	Description	Min	Max	Units
tP_{RLFP}	RHCLK Low to RLFP Propagation	2	10	ns
tP_{RAIS}	RHCLK Low to RLFP Propagation	2	10	ns
tP_{RFERF}	RHCLK Low to RLFP Propagation	2	10	ns
tP_{RLDL}	RLDLCLK Low to RLDL Propagation	2	10	ns
tP_{RLOW}	RLOWCLK Low to RLOW Propagation	2	10	ns
tP_{RAPS}	RAPSCLK Low to RAPS Propagation	2	10	ns

Fig. 37a Receive Line Overhead Output Timing

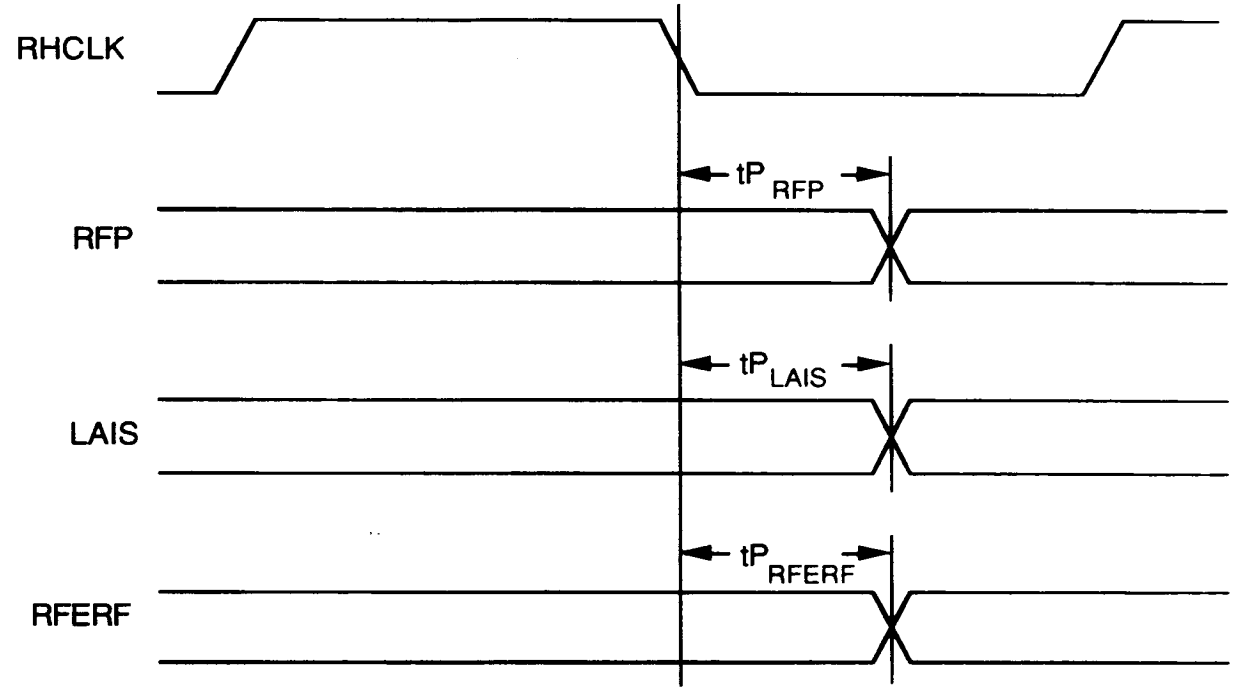
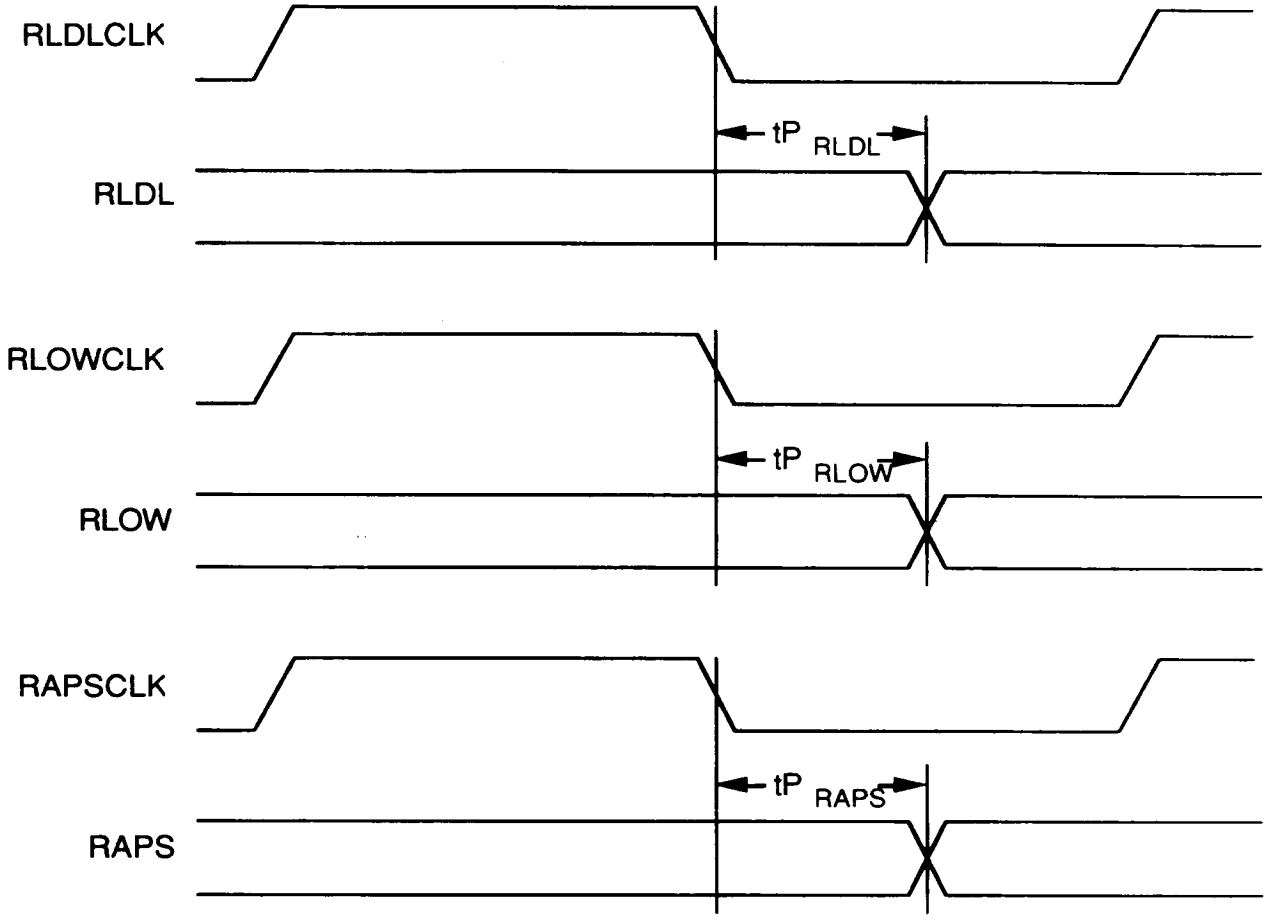


Fig. 37b Receive Line Overhead Output Timing



Transmit Overhead Input/Output Timing Characteristics

Transmit Line Overhead Input Timing (Fig. 38)

Symbol	Description	Min	Max	Units
tS_{TFERF}	TFERF to TLHCLK High Setup time	6		ns
tH_{TFERF}	TLHCLK High to TFERF Hold time.	6		ns
tS_{TLDIS}	TLDIS to THCLK High Setup time	6		ns
tH_{TLDIS}	THCLK High to TLDIS Hold time.	6		ns
tS_{TLDL}	TLDL to TLDLCLK High Setup time.	20		ns
tH_{TLDL}	TLDLCLK High to TLDL Hold time.	20		ns
tS_{TLOW}	TLOW to TLOWCLK High Setup time.	20		ns
tH_{TLOW}	TLOWCLK High to TLOW Hold time	20		ns
tS_{TAPS}	TLDL to TLDLCLK High Setup time.	20		ns
tH_{TAPS}	TLDLCLK High to TLDL Hold time.	20		ns

Fig. 38a Transmit Line Overhead Input Timing

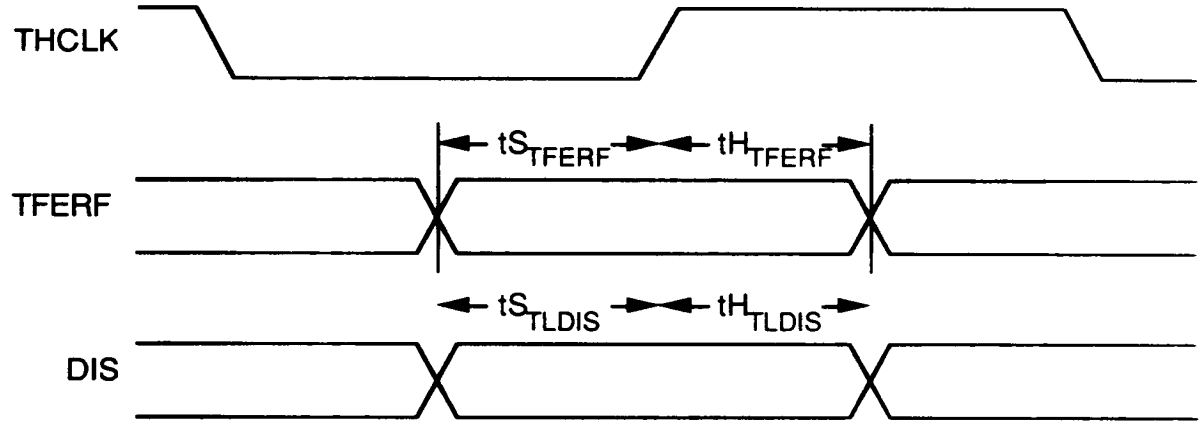
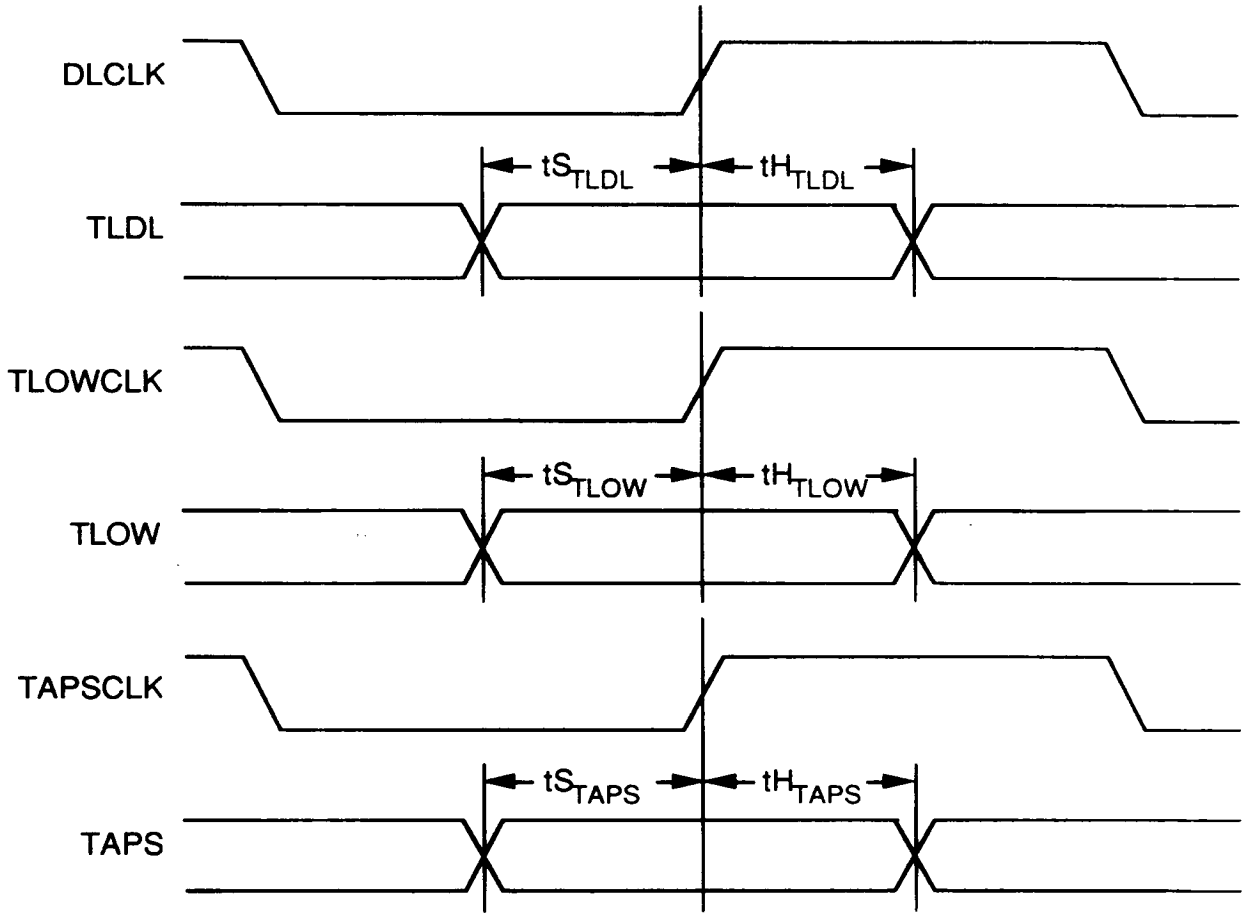


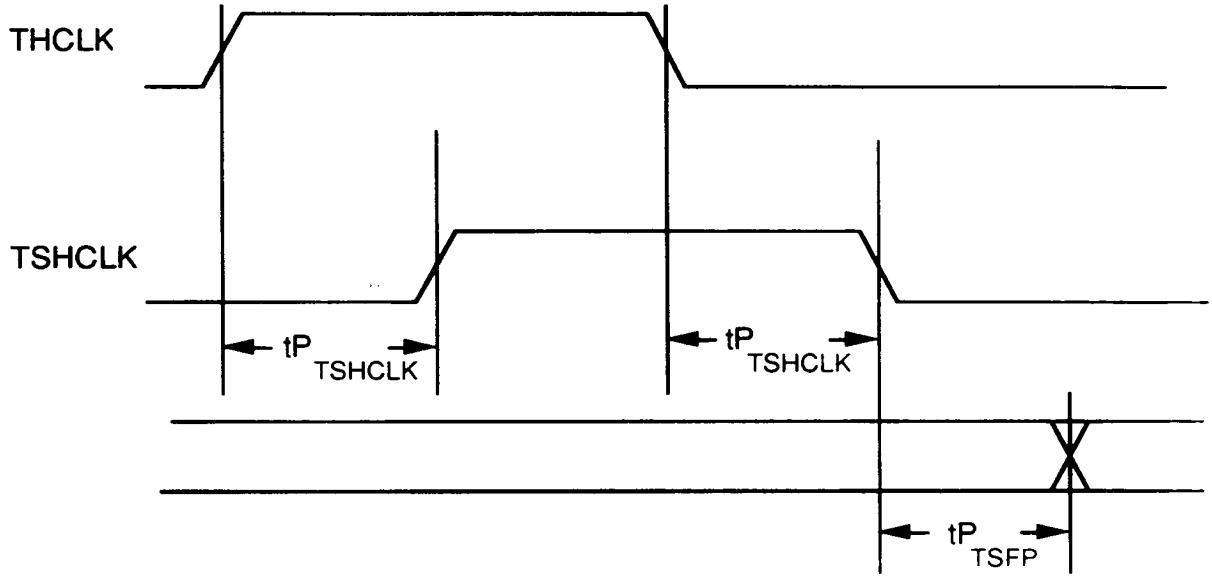
Fig. 38b Transmit Line Overhead Input Timing



Transmit Line Overhead Output Timing (Fig. 39)

Symbol	Description	Min	Max	Units
tP_{TSHCLK}	Propagation Delay, THCLK to TSHCLK Valid	14	50	ns
tP_{TSFP}	Propagation Delay, TSHCLK low to TSFP Valid	0	4	ns

Fig. 39 Transmit Line Overhead Output Timing



Transmit Section Overhead Input Timing (Fig. 40)

Symbol	Description	Min	Max	Units
tS_{TLAIS}	TLAIS to TSHCLK High Setup time.	4		ns
tH_{TLAIS}	TSHCLK High to TLAIS Hold.time	5		ns
tS_{TSDIS}	TSDIS to TSHCLK High Setup time.	4		ns
tH_{TSDIS}	TSHCLK High to TSDIS Hold.time	5		ns
tS_{TSDL}	TSOW to TSOWCLK High Setup time.	20		ns
tH_{TSDL}	TSOWCLK High to TSOW Hold.time	20		ns
tS_{TSOW}	TSUC to TSUCCLK High Setup time.	20		ns
tH_{TSOW}	TSUCCLK High to TSUC Hold.time	20		ns
tS_{TUC}	TSUC to TSUCCLK High Setup time	20		ns
tH_{TUC}	TUCCLK High to TSUC DATA Hold time	20		ns

Fig. 40a Transmit Section Overhead Input Timing

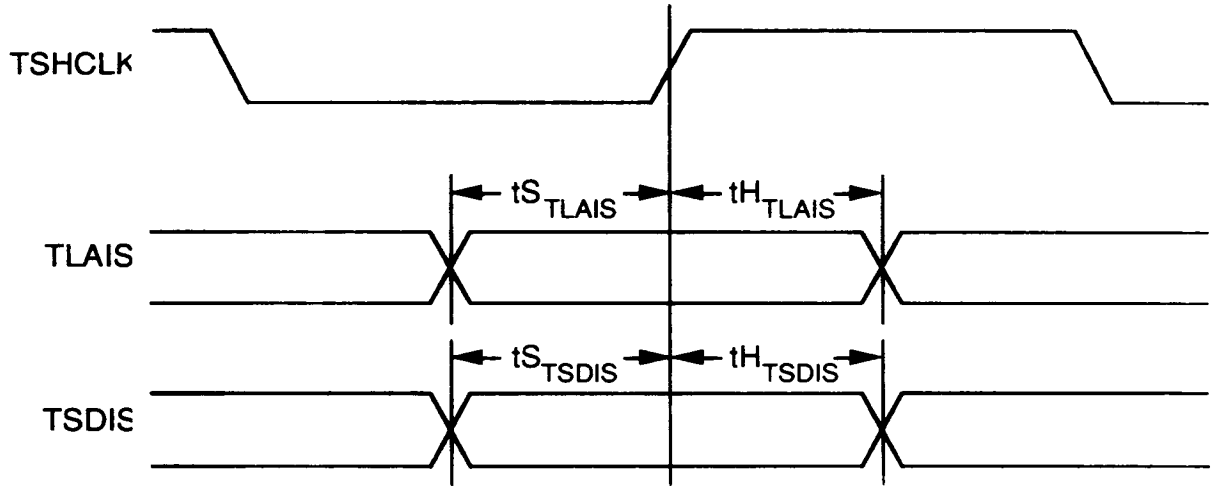
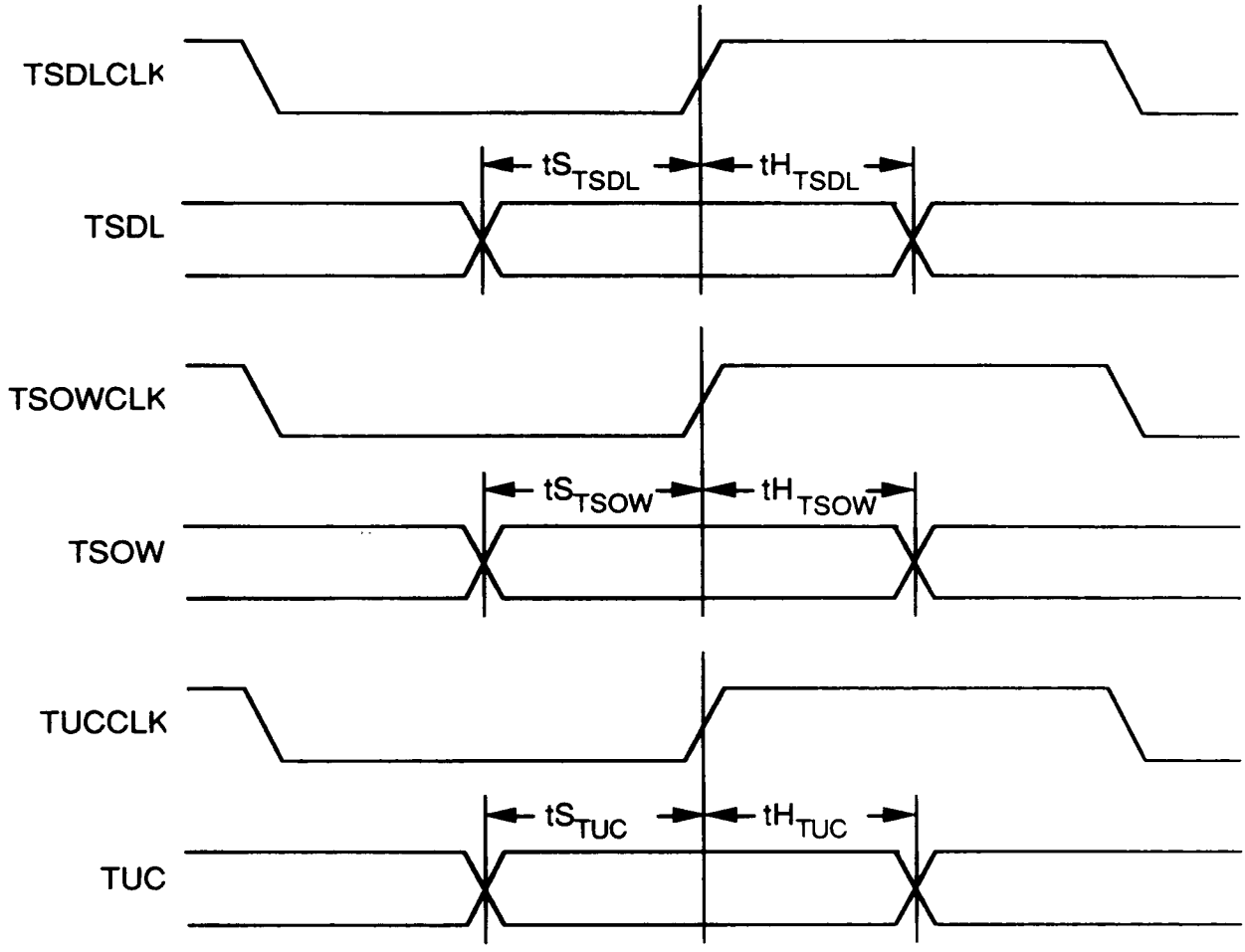


Fig. 40b Transmit Section Overhead Input Timing



DC CHARACTERISTICS

(T_a= 0°C to T_c+70°C, V_{DD} = 5 V ±10%)

Input Output Logic Levels

Symbol	Parameter	Min	Max	Unit	Notes
V_{IL}	CMOS Input Low Voltage		0.8	Volts	Guaranteed Input LOW Voltage
V_{IH}	CMOS Input High Voltage	2.0		Volts	Guaranteed Input HIGH Voltage
V_{OL}	CMOS Output or Bidirectional Low Voltage		0.4	Volts	V_{DD} = min, I_{OL} = 4 mA for Data Bus Pins and 2 mA for others, Note 3
V_{OH}	CMOS Output or Bidirectional High Voltage	2.4		Volts	V_{DD} = min, I_{OL} = 4 mA for Data Bus Pins and 2 mA for others, Note 3
V_T	CMOS Reset Input High Voltage	2.3	2.8	Volts	RSTB levels
V_{TH}	CMOS Reset Input Hysteresis Voltage	0.5	1.2	Volts	RSTB levels
I_{ILPU}	CMOS Input Low Current		-26	-110	µA $V_{IL} \leq 1.65$ V, Notes 1, 3
I_{IHPU}	CMOS Input High Current	-48	-110	µA	$V_{IH} \geq 3.85$ V, Notes 1, 3
I_{IL}	CMOS Input Low Current	-10	0	µA	$V_{IL} \leq 1.65$ V, Notes 2, 3
I_{IH}	CMOS Input High Current	-10	10	µA	$V_{IH} \geq 3.85$ V, Notes 2, 3
I_{RSD}	RSD Input Current	-300	300	µA	$V_{RSDH} \geq V_{RSD} \geq V_{RSDL}$
V_{RSDH}	RSD Input High Voltage	-1.0		V	V_{TH} = 1.3 V
V_{RSDL}	RSD Input Low Voltage		-1.6	V	V_{TH} = 1.3 V
V_{EOH}	ECL Output High Voltage	-0.93	-0.6	V	
V_{EOH}	ECL Output Low Voltage	-2.0	-1.7	V	

Notes on D.C. Characteristics:

1. Input pin or bidirectional pin with internal pull-up resistors.
2. Input pin or bidirectional pin without internal pull-up resistors
3. Negative currents flow into the device (sinking), positive currents flow out of the device (sourcing).
4. T_a ambient temperature, T_c case temperature.

D.C. Power Supply Currents

(T_a = 0°C to T_c +70°C, V_{DD} = 5 V ±10%)

Symbol	Parameter	Min	Max	Units	Conditions
I_{DDO}	Operating Current		1075	mA	V_{DDS} = +5.5 V, Outputs Unloaded
I_{CCRO}	Operating Current		40	mA	V_{CCR} = +5.5 V, Outputs Unloaded
I_{CCTO}	Operating Current		40	mA	V_{CCR} = +5.5 V, Outputs Unloaded
I_{EERO}	Operating Current		-290	mA	V_{EER} = -5.5 V, Outputs Unloaded
I_{EETO}	Operating Current		-290	mA	V_{EER} = -5.5 V, Outputs Unloaded
I_{EEO}	Operating Current		1000	mA	V_{EE} = -5.4 V, Outputs Unloaded
I_{DTTO}	Operating Current		650	mA	V_{TT} = - 2.2 V, Outputs Unloaded
I_{DDS}	Static Current			µA	V_{DDS} = +5.5 V, Outputs Unloaded
I_{CCTS}	Static Current			mA	V_{CCR} = +5.5 V, Outputs Unloaded
I_{EERS}	Static Current			mA	V_{EER} = -5.5 V, Outputs Unloaded
I_{EETS}	Static Current			mA	V_{EER} = -5.5 V, Outputs Unloaded

I_{EES}	Static Current			mA	$V_{EE\ G}$ = -5.5 V, Outputs Unloaded
I_{CCRS}	Static Current			mA	V_{CCR} = +5.5 V, Outputs Unloaded

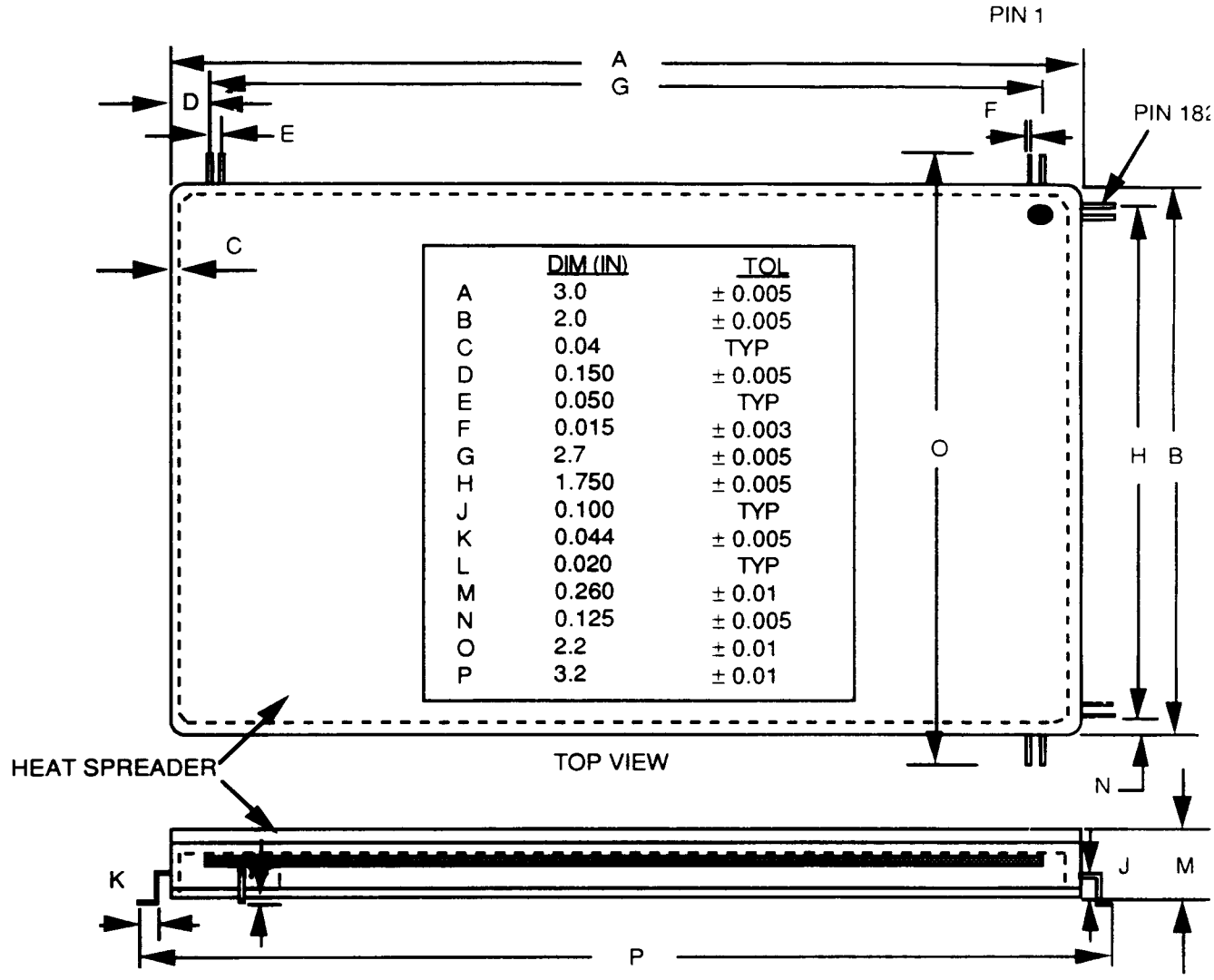
Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Condition
T_S	Storage Temp	-40	+125	°C	
V_{CCR}	Voltage on V_{CCR} w.r.t. GND	0	+7.0	V	
V_{CCT}	Voltage on V_{CCT} w.r.t. GND	0	+7.0	V	
V_{EER}	Voltage on V_{EER} w.r.t. GND	-7.0	0	V	
V_{EET}	Voltage on V_{EET} w.r.t. GND	-7.0	0	V	
V_{EE}	Voltage on V_{EE} w.r.t. GND	-6.0	+0.5	V	
V_{DD}	Voltage on V_{DD} w.r.t. GND	-0.5	+6.0	V	
V_{CI}	Voltage on any CMOS input pin	-0.5	+6.0	V	
V_S	Static Discharge Voltage on any pin		2000	V	
V_{EI}	Voltage applied to any ECL input	-4.0	+0.5	V	
V_{TT}	Terminating Voltage for any ECL output .	-4.0	+7.0	V	
I_{EO}	Current drawn from any ECL output	0	100	mA	

Normal Operating Range

Symbol	Parameter	Min	Max	Unit	Conditions
T_C	Case Operating Temperature	0	70	°C	
T_A	Ambient Operating Temperature	0	70	°C	
V_{DD}	Power Supply	4.5	5.5	V	
V_{CCT}	Power Supply	4.75	5.25	V	
V_{CCR}	Power Supply	4.75	5.25	V	
V_{EERA}	Power Supply	-5.4	-5.1	V	
V_{EETA}	Power Supply	-5.4	-5.1	V	
V_{EET}	Power Supply	-5.5	-4.8	V	
V_{TTT}	Power Supply	-2.1	-1.9	V	

MECHANICAL DRAWING



	DIM (IN)	TOL
A	3.0	± 0.005
B	2.0	± 0.005
C	0.04	TYP
D	0.150	± 0.005
E	0.050	TYP
F	0.015	± 0.003
G	2.7	± 0.005
H	1.750	± 0.005
J	0.100	TYP
K	0.044	± 0.005
L	0.020	TYP
M	0.260	± 0.01
N	0.125	± 0.005
O	2.2	± 0.01
P	3.2	± 0.01

Notes:

1. Pin 1 is indicated on the top of the package. Pin numbering is counterclockwise when the package is viewed from the top with the dot indicator visible.
2. The standard package for the PM5712 is cavity down to allow for a heat sink to be attached to the top, and is denoted by part number PM5712AU.
3. An alternate package version may be supplied with cavity up, if heat sinking through the printed circuit card is desired.
4. Upon special request, the module may be supplied with informed leads, and the tie bar between the leads entact.

NOTES

910121ref 900612A6 Issue date: January, 1992.

Printed in Canada

Pacific Microelectronics Centre 8999 Nelson Way Burnaby. BC Canada V5A 4B5 604 293 5755

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