PM7347

S/UNI-JET™

S/UNI-JET

SATURN USER NETWORK INTERFACE FOR J2/E3/T3

DATA SHEET

ISSUE 2: MARCH 2000

CONTENTS

FEATURES

- Single chip ATM User Network Interface operating at 44.736 Mbit/s, 34.368 Mbit/s, and 6.312 Mbit/s conforming to af-phy-0054.000, af-phy-0034.000 and AF-PHY-0029.000.
- Implements ATM Direct Cell Mapping into DS1, DS3, E1, E3, and J2 transmission systems according to ITU-T Recommendation G.804.
- Provides a UTOPIA Level 2 compatible ATM-PHY Interface.
- Implements the Physical Layer Convergence Protocol (PLCP) for DS1 and DS3 transmission systems according to the ATM Forum User Network Interface Specification and ANSI TA-TSY-000773, TA-TSY-000772, and E1 and E3 transmission systems according to the ETSI 300-269 and ETSI 300-270.
- Support is provided for SMDS and ATM mappings into various rate transmission systems as follows:

Table 1 - Supported Operating Formats

Rate	Format	Framer Only	SMDS PLCP Mapping	ATM Direct Mapping
T3 (44.736 Mbit/s)	C-bit Parity	YES	YES	YES
	M23	YES	YES	YES
E3 (34.368 Mbit/s)	G.751	YES	YES	YES
	G.832	YES	n/a	YES
J2 (6.312 Mbit/s)	G.704 & NTT	YES	n/a	YES
E1 (2.048 Mbit/s)	CRC-4	external	YES	YES
	PCM30	external	YES	YES
T1 (1.544 Mbit/s)	ESF	external	YES	YES
	SF	external	YES	YES
Arbitrary Cell Rate (up to 52 Mbit/s)		bypass	n/a	YES

- Implements the ATM physical layer for Broadband ISDN according to ITU-T Recommendation I.432.
- Provides on-chip DS3, E3 (G.751 and G.832), and J2 framers.
- Can be configured to be used solely as a DS3, E3, or J2 Framer.

- When configured to operate as a DS3, E3, or J2 Framer, gapped transmit and receive clocks can be optionally generated for interface to devices which only need access to payload data bits.

- Provides support for an arbitrary rate external transmission system interface up to a maximum rate of 52 Mbit/s which enables the S/UNI-JET to be used as an ATM cell delineator.

- Uses the PMC-Sierra PM4351 COMET, PM4341 T1XC and PM6341 E1XC T1 and E1 framer/line interface chips for DS1 and E1 applications.

- Provides programmable pseudo-random test pattern generation, detection, and analysis features.

- Provides integral transmit and receive HDLC controller with 128-byte FIFO depth.

- Provides performance monitoring counters suitable for accumulation periods of up to 1 second.

- Provides an 8-bit microprocessor interface for configuration, control and status monitoring.

- Provides a standard 5 signal P1149.1 JTAG test port for boundary scan board test purposes.

- Low power 3.3V CMOS technology with 5V tolerant inputs.

- Available in a 256-pin SBGA package (27mm x 27mm).

The receiver section:

- Provides frame synchronization for the M23 or C-bit parity DS3 applications, alarm detection, and accumulates line code violations, framing errors, parity errors, path parity errors and FEBE events. In addition, far end alarm channel codes are detected, and an integral HDLC receiver is provided to terminate the path maintenance data link.

- Provides frame synchronization for the G.751 or G.832 E3 applications, alarm detection, and accumulates line code violations, framing errors, parity errors, and FEBE events. In addition, in G.832, the Trail Trace is detected, and an integral HDLC receiver is provided to terminate either the Network Requirement or the General Purpose data link.

- Provides frame synchronization for G.704 and NTT 6.312 Mbit/s J2 applications, alarm detection, and accumulates line code violations, framing errors, and CRC parity errors. An integral HDLC receiver is provided to terminate the data link.

- Provides frame synchronization, cell delineation and extraction for DS3, G.751 E3, G.832 E3, and G.704 and NTT J2 ATM direct-mapped formats.

- Provides PLCP frame synchronization, path overhead extraction, and cell extraction for DS1 PLCP, DS3 PLCP, E1 PLCP, and G.751 E3 PLCP formatted streams.

- Provides a 50 MHz 8-bit wide or 16-bit wide Utopia FIFO buffer in the receive path with parity support, and multi-PHY (Level 2) control signals.

- Provides ATM framing using cell delineation. ATM cell delineation may optionally be disabled to allow passing of all cell bytes regardless of cell delineation status.

- Provides cell descrambling, header check sequence (HCS) error detection, idle cell filtering, header descrambling (for use with PPP packets), and accumulates the number of received idle cells, the number of received cells written to the FIFO, and the number of HCS errors.

- Provides a four cell FIFO for rate decoupling between the line, and a higher layer processing entity. FIFO latency may be reduced by changing the number of operational cell FIFOs.

- Provides a receive HDLC controller with a 128-byte FIFO to accumulate data link information.

- Provides detection of yellow alarm and loss of frame (LOF), and accumulates BIP-8 errors, framing errors and FEBE events.

- Provides programmable pseudo-random test-sequence detection (up to 2^{32}-1 bit length patterns conforming to ITU-T O.151 standards) and analysis features.

The transmitter section:

- Provides frame insertion for the M23 or C-bit parity DS3 applications, alarm insertion, and diagnostic features. In addition, far end alarm channel codes may be inserted, and an integral HDLC transmitter is provided to insert the path maintenance data link.

- Provides frame insertion for the G.751 or G.832 E3 applications, alarm insertion, and diagnostic features. In addition, for G.832, the Trail Trace is inserted, and an integral HDLC transmitter is provided to insert either the Network Requirement or the General Purpose data link.

- Provides frame insertion for G.704 6.312 Mbit/s J2 applications, alarm insertion, and diagnostic features. An integral HDLC transmitter is provided to insert the path maintenance data link.

- Provides frame insertion and path overhead insertion for DS1, DS3, E1 or E3 based PLCP formats. In addition, alarm insertion and diagnostic features are provided.

- Provides a 50 MHz 8-bit wide or 16-bit wide Utopia FIFO buffer in the transmit path with parity support and multi-PHY (Level 2) control signals.

- Provides optional ATM cell scrambling, header scrambling (for use with PPP packets), HCS generation/insertion, programmable idle cell insertion, diagnostics features and accumulates transmitted cells read from the FIFO.

- Provides a four cell FIFO for rate decoupling between the line and a higher layer processing entity. FIFO latency may be reduced by changing the number of operational cells in the FIFO.
- Provides a transmit HDLC controller with a 128-byte FIFO.
- Provides an 8 kHz reference input for locking the transmit PLCP frame rate to an externally applied frame reference.
- Provides programmable pseudo-random test sequence generation (up to 2^{32}-1 bit length sequences conforming to ITU-T O.151 standards). Diagnostic abilities include single bit error insertion or error insertion at bit error rates ranging from 10^{-1} to 10^{-7}.

Bypass and Loopback features:

- Allows bypassing of the DS3, E3, and J2 framers to enable transmission system sublayer processing by an external device.
- Allows bypassing of the PLCP and ATM functions to enable use of the S/UNI-JET as a DS3, E3, or J2 framer.
- Provides for diagnostic loopbacks, line loopbacks, and payload loopbacks.

1 APPLICATIONS

- ATM or SMDS Switches, Multiplexers, and Routers
- SONET/SDH Mux E3/DS3 Tributary Interfaces
- PDH Mux J2/E3/DS3 Line Interfaces
- DS3/E3/J2 Digital Cross Connect Interfaces
- DS3/E3/J2 PPP Internet Access Interfaces
- DS3/E3/J2 Frame Relay Interfaces

2 REFERENCES

1. ANSI T1.627 - 1993, "Broadband ISDN - ATM Layer Functionality and Specification".

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3. ANSI T1.107 - 1995, "Digital Hierarchy - Formats Specifications".

4. ANSI T1.646 - 1995, "Broadband ISDN - Physical Layer Specification for User-Network Interfaces Including DS1/ATM".

5. ATM Forum - ATM User-Network Interface Specification, V3.1, October, 1995.

6. ATM Forum - “UTOPIA, An ATM PHY Interface Specification, Level 2, Version 1”, June, 1995.

7. ATM Forum, af-phy-0034.000, "E3 (34,368 kbps) Physical Layer Interface", August, 1995.

8. ATM Forum, af-phy-0054.000, "DS3 Physical Layer Interface Specification", January, 1996.

9. ATM Forum, af-phy-0029.000, "6,312 Kbps UNI Specification, Version 1.0", June 1995.

10. Bell Communications Research, TA-TSY-000773 - “Local Access System Generic Requirements, Objectives, and Interface in Support of Switched Multi-megabit Data Service” Issue 2, March 1990 and Supplement 1, December 1990.

11. ETS 300 269 Draft Standard T/NA(91)17 - “Metropolitan Area Network Physical Layer Convergence Procedure for 2.048 Mbit/s”, April 1994.

12. ETS 300 270 Draft Standard T/NA(91)18 - “Metropolitan Area Network Physical Layer Convergence Procedure for 34.368 Mbit/s”, April 1994.

13. ITU-T Recommendation O.151 - "Error Performance Measuring Equipment Operating at the Primary Rate and Above", October, 1992.

14. ITU-T Recommendation I.432 - "B-ISDN User-Network Interface - Physical Layer Specification", 1993

15. ITU-T Recommendation G.703 - "Physical/Electrical Characteristics of Hierarchical Digital Interfaces", 1991.

16. ITU-T Recommendation G.704 - "General Aspects of Digital Transmission Systems; Terminal Equipments - Synchronous Frame Structures Used At 1544, 6312, 2048, 8488 and 44 736 kbit/s Hierarchical Levels", July, 1995.

17. ITU-T Recommendation G.751 - CCITT Blue Book Fasc. III.4, "Digital Multiplex Equipments Operating at the Third Order Bit Rate of 34,368 kbit/s and the Fourth Order Bit Rate of 139,264 kbit/s and Using Positive Justification", 1988.

18. ITU-T Draft Recommendation G.775 - "Loss of Signal (LOS) and Alarm Indication Signal (AIS) Defect Detection and Clearance Criteria", October 1993.

19. ITU-T Recommendation G.804 - "ATM Cell Mapping into Plesiochronous Digital Hierarchy (PDH)", 1993.

20. ITU-T Recommendation G.832 - "Transport of SDH Elements on PDH Networks: Frame and Multiplexing Structures", 1993.

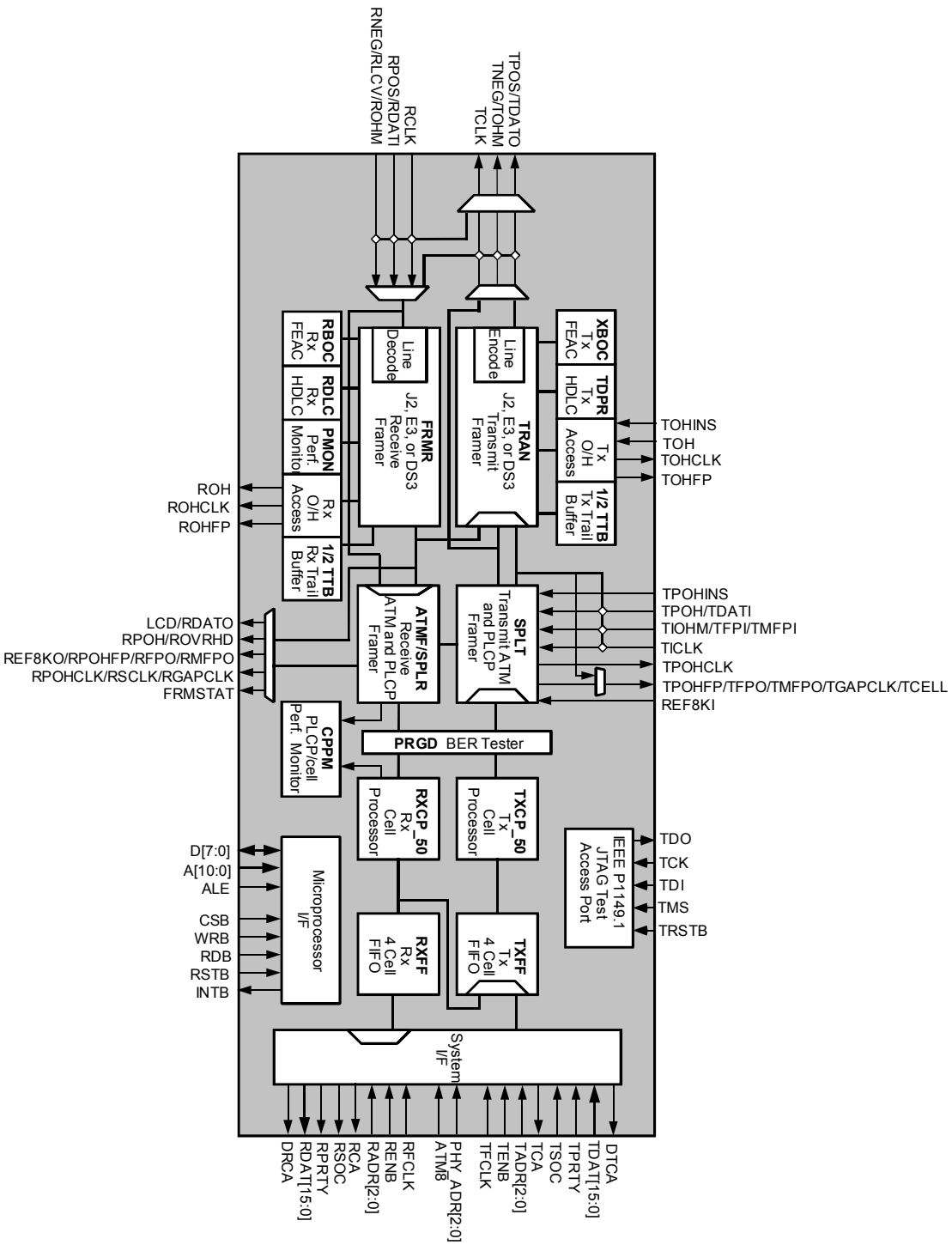
21. ITU-T Recommendation Q.921 - "ISDN User-Network Interface - Data Link Layer Specification", March, 1993.

22. NTT Technical Reference, "NTT Technical Reference for High-Speed Digital Leased Circuit Services", 1991.

3 DATASHEET OVERVIEW

The PM7347 S/UNI-JET is functionally equivalent to a single channel PM7346 S/UNI-QJET. The devices are software compatible and pin compatible. This datasheet provides a complete pin-out description for the S/UNI-JET, as well as any differences between these devices (including boundary scan register, test mode 0 register, 006H register and the Device Identification register). For a complete functional and register description, please refer to the PMC-96-0835 S/UNI-QJET datasheet.

4 BLOCK DIAGRAM



5 PIN DIAGRAM

The S/UNI-JET is packaged in a 256-pin SBGA package having a body size of 27mm by 27mm and a pin pitch of 1.27 mm.

	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
A	VSS	VSS	VSS	TDAT[10]	TDAT[14]	D[1]	D[5]	VSS	A[3]	A[7]	VSS	VSS	ALE	INTB	TRSTB	TNEG	RCLK	VSS	VSS	VSS
B	VSS	VDD	VDD	TDAT[9]	TDAT[13]	D[0]	D[4]	A[0]	A[2]	A[6]	A[9]	A[10]	WRB	TDO	TCK	TCLK	NC	VDD	VDD	VSS
C	VSS	VDD	VDD	TDAT[7]	TDAT[11]	TDAT[15]	D[2]	D[6]	A[1]	A[5]	A[8]	CSB	RSTB	TMS	TPOS	RNEG	NC	VDD	VDD	VSS
D	TDAT[3]	TDAT[4]	TDAT[6]	NC	TDAT[8]	TDAT[12]	VDD	D[3]	D[7]	A[4]	VDD	RDB	TDI	VDD	RPOS	NC	BIAS	NC	NC	VSS
E	TFCLK	TDAT[0]	TDAT[2]	TDAT[5]													NC	VSS	VSS	VSS
F	TADR[0]	TADR[1]	TADR[2]	TDAT[1]													VSS	VSS	NC	NC
G	TSOC	TPRTY	VDD	VDD													VDD	NC	VSS	VSS
H	BIAS	TCA	TENB	VDD													VSS	TOH	TOHCLK	VSS
J	VSS	NC	NC	DTCA													TOHINS	TOHFP	ROH	ROHFP
K	VSS	NC	PHY_ADR[2]	VDD					BOTTOM VIEW								ROHCLK	VSS	VSS	NC
L	PHY_ADR[1]	PHY_ADR[0]	ATM8	DRCA													VDD	NC	NC	VSS
M	NC	NC	NC	RSOC													VSS	NC	NC	VSS
N	VSS	RCA	RENB	RADR[1]													NC	NC	NC	VSS
P	RFCLK	RADR[2]	RADR[0]	VDD													VDD	VSS	NC	NC
R	VDD	VDD	RPRTY	RDAT[13]													NC	NC	NC	VSS
T	RDAT[15]	RDAT[14]	RDAT[12]	RDAT[9]													NC	REF8KI	NC	NC
U	RDAT[11]	RDAT[10]	RDAT[8]	BIAS	RDAT[6]	RDAT[2]	VDD	TPOHCLK	REF8KO	VDD	NC	VSS	NC	VDD	NC	NC	BIAS	NC	NC	FRMSTAT
V	VSS	VDD	VDD	RDAT[7]	RDAT[3]	TICLK	TPOHINS	RPOH	VSS	NC	NC	VSS	NC	NC	VSS	NC	NC	VDD	VDD	VSS
W	VSS	VDD	VDD	RDAT[5]	RDAT[1]	TIOHM	TPOHFP	RPOHCLK	VSS	VSS	NC	VSS	VSS	NC	VSS	VSS	NC	VDD	VDD	VSS
Y	VSS	VSS	VSS	RDAT[4]	RDAT[0]	TPOH	LCD	VSS	VSS	VSS	NC	NC	VSS	NC	NC	VSS	NC	VSS	VSS	VSS
	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1

6 PIN DESCRIPTION

Pin Name	Type	Pin No.	Function
TPOS	Output	C6	Transmit Digital Positive Pulse (TPOS). TPOS contains the positive pulses transmitted on the B3ZS-encoded DS3, HDB3-encoded E3, or B8ZS-encoded J2 transmission system when the dual-rail output format is selected.
TDATO			Transmit Data (TDATO). TDATO contains the transmit data stream when the single-rail (unipolar) output format is enabled or when a non-DS3/E3/J2 based transmission system is selected. The TPOS/TDATO pin function selection is controlled by the TFRM[1:0] and the TUNI bits in the S/UNI-JET Transmit Configuration Register. Output signal polarity control is provided by the TPOSINV bit in the S/UNI-JET Transmit Configuration Register. Both TPOS and TDATO are updated on the falling edge of TCLK by default, and may be configured to be updated on the rising edge of TCLK through the TCLKINV bit in the S/UNI-JET Transmit Configuration Register. Finally, both TPOS and TDATO can be updated on the rising edge of TICLK, enabled by the TICLK bit in the S/UNI-JET Transmit Configuration Register.
TNEG	Output	A5	Transmit Digital Negative Pulse (TNEG). TNEG contains the negative pulses transmitted on the B3ZS-encoded DS3, HDB3-encoded E3, or B8ZS-encoded J2 transmission system when the dual-rail NRZ output format is selected.

Pin Name	Type	Pin No.	Function
TOHM	Output	A5	Transmit Overhead Mask (TOHM). TOHM indicates the position of overhead bits (non-payload bits) in the transmission system stream aligned with TDATO. TOHM indicates the location of the M-frame boundary for DS3, the position of the frame boundary for E3, and the position of the multi-frame boundary for J2 when the single-rail (unipolar) NRZ input format is enabled. When a PLCP formatted signal is transmitted, TOHM is set to logic 1 once per transmission frame, and indicates the DS1 or E1 frame alignment. When a non-PLCP, non-DS3, non-E3, non-J2 based signal is transmitted, TOHM is a delayed version of the TIOHM input, and indicates the position of each overhead bit in the transmission frame. TOHM is updated on the falling edge of TCLK. The TNEG/TOHM pin function selection is controlled by the TFRM[1:0] and the TUNI bits in the S/UNI-JET Transmit Configuration Register. Output signal polarity control is provided by the TNEGINV bit in the S/UNI-JET Transmit Configuration Register. Both TNEG and TOHM are updated on the falling edge of TCLK by default, and may be enabled to be updated on the rising edge of TCLK. This sampling is controlled by the TCLKINV bit in the S/UNI-JET Transmit Configuration Register. Finally, both TNEG and TOHM can be updated on the rising edge of TICLK, enabled by the TICLK bit in the S/UNI-JET Transmit Configuration Register.
TCLK	Output	B5	Transmit Output Clock (TCLK). TCLK provides the transmit direction timing. TCLK is a buffered version of TICLK and can be enabled to update the TPOS/TDATO and TNEG/TOHM outputs on its rising or falling edge.
RPOS	Input	D6	Receive Digital Positive Pulse (RPOS). RPOS contains the positive pulses received on the B3ZS-encoded DS3, the HDB3-encoded E3, or the B8ZS-encoded J2 transmission system when the dual-rail NRZ input format is selected.

Pin Name	Type	Pin No.	Function
RDATI			Receive Data (RDATI). RDATI contains the data stream when the single-rail (unipolar) NRZ input format is enabled or when a non-DS3/E3/J2 based transmission system is being processed (for example RDATI may contain a DS1 or E1 stream). The RPOS/RDATI pin function selection is controlled by the RFRM[1:0] bits in the S/UNI-JET Configuration Register and by the UNI bits in the DS3 FRMR, the E3 FRMR, or the J2 FRMR Configuration Register. Both RPOS and RDATI are sampled on the rising edge of RCLK by default, and may be enabled to be sampled on the falling edge of RCLK. This sampling is controlled by the RCLKINV bit in the S/UNI-JET Receive Configuration Register. In addition, signal polarity control is provided by the RPOSINV bit in the S/UNI-JET Receive Configuration Register.
RNEG	Input	C5	Receive Digital Negative Pulse (RNEG). RNEG contains the negative pulses received on the B3ZS encoded DS3, the HDB3-encoded E3, or the B8ZS-encoded J2 transmission system when the dual-rail NRZ input format is selected.
RLCV			Receive Line Code Violation (RLCV). RLCV contains line code violation indications when the single-rail (unipolar) NRZ input format is enabled for DS3, E3, or J2 applications. Each line code violation is represented by an RCLK period-wide pulse.

Pin Name	Type	Pin No.	Function
ROHM	Input	C5	Receive Overhead Mask (ROHM). When a DS1 or E1 PLCP or ATM direct-mapped signal is received, ROHM is pulsed once per transmission frame, and indicates the DS1 or E1 frame alignment relative to the RDATI data stream. When an alternate frame-based signal is received, ROHM indicates the position of each overhead bit in the transmission frame. The RNEG/RLCV/ROHM pin function selection is controlled by the RFRM[1:0] bits in the S/UNI-JET Receive Configuration Register, the UNI bits in the DS3 FRMR, E3 FRMR, or J2 FRMR Configuration Register, and the PLCPEN and EXT bits in the SPLR Configuration register. RNEG, RLCV, and ROHM are sampled on the rising edge of RCLK by default, and may be enabled to be sampled on the falling edge of RCLK. This sampling is controlled by the RCLKINV bit in the S/UNI-JET Receive Configuration Register. In addition, signal polarity control is provided by the RNEGINV bit in the S/UNI-JET Receive Configuration Register.
RCLK	Input	A4	Receive Clock (RCLK). RCLK provides the receive direction timing. RCLK is the externally recovered transmission system baud rate clock that samples the RPOS/RDATI and RNEG/RLCV/ROHM inputs on its rising or falling edge.
TOHINS	Input	J4	Transmit DS3/E3/J2 Overhead Insertion (TOHINS). TOHINS controls the insertion of the DS3, E3, or J2 overhead bits from the TOH input. When TOHINS is high, the associated overhead bit in the TOH stream is inserted in the transmitted DS3, E3, or J2 frame. When TOHINS is low, the DS3, E3, or J2 overhead bit is generated and inserted internally. TOHINS is sampled on the rising edge of TOHCLK. If TOHINS is a logic 1, the TOH input has precedence over the internal datalink transmitter, or any internal register bit setting.

Pin Name	Type	Pin No.	Function
TOH	Input	H3	Transmit DS3/E3/J2 Overhead Data (TOH). When configured for DS3 operation, TOH contains the overhead bits (C, F, X, P, and M) that may be inserted in the transmit DS3 stream. When configured for G.832 E3 operation, TOH contains the overhead bytes (FA1, FA2, EM mask, TR, MA, NR, and GC) that may be inserted in the transmit G.832 E3 stream. When configured for G.751 E3 operation, TOH contains the overhead bits (RAI, National Use, Stuff Indication, and Stuff Opportunity) that may be inserted in the transmit G.751 E3 stream. When configured for J2 operation, TOH contains the overhead bits (TS97, TS98, Framing, X_{1-3}, A, M, E_{1-5}) that may be inserted in the transmit J2 stream. If TOHINS is a logic 1, the TOH input has precedence over the internal datalink transmitter, or any other internal register bit setting. TOH is sampled on the rising edge of TOHCLK.
TOHFP	Output	J3	Transmit DS3/E3/J2 Overhead Frame Position (TOHFP). TOHFP is used to align the individual overhead bits in the transmit overhead data stream, TOH, to the DS3 M-frame or the E3 frame. For DS3, TOHFP is high during the X1 overhead bit position in the TOH stream. For G.832 E3, TOHFP is high during the first bit of the FA1 byte. For G.751 E3, TOHFP is high during the RAI overhead bit position in the TOH stream. For J2, TOHFP is high during the first bit of timeslot 97 in the first frame of a 4-frame multiframe). TOHFP is updated on the falling edge of TOHCLK.
TOHCLK	Output	H2	Transmit DS3/E3/J2 Overhead Clock (TOHCLK). TOHCLK is active when a DS3, E3, or J2 stream is being processed. TOHCLK is nominally a 526 kHz clock for DS3, a 1.072 MHz clock for G.832 E3, a 1.074 MHz clock for G.751 E3, and a gapped 6.312 MHz clock with an average frequency of 168 kHz for J2. TOHFP is updated on the falling edge of TOHCLK. TOH, and TOHINS are sampled on the rising edge of TOHCLK.

Pin Name	Type	Pin No.	Function
REF8KI	Input	T3	Reference 8 kHz Input (REF8KI). The PLCP frame rate is locked to an external 8 kHz reference applied on this input . An internal phase-frequency detector compares the transmit PLCP frame rate with the externally applied 8 kHz reference and adjusts the PLCP frame rate. The REF8KI input must transition high once every 125 µs for correct operation. The REF8KI input is treated as an asynchronous signal and must be "glitch-free". If the LOOPT register bit is logic 1, the PLCP frame rate is locked to the RPOHFP signal instead of the REF8KI input.
TPOHINS	Input	V14	Transmit Path Overhead Insertion (TPOHINS). TPOHINS controls the insertion of PLCP overhead octets on the TPOH input. When TPOHINS is logic 1, the associated overhead bit in the TPOH stream is inserted in the transmit PLCP frame. When TPOHINS is logic 0, the PLCP path overhead bit is generated and inserted internally. TPOHINS is sampled on the rising edge of TPOHCLK. Note, when operating in G.751 E3 PLCP mode, bits 8, 7 and 6 of the C1 octet should not be manipulated.
TPOH	Input	Y15	Transmit PLCP Overhead Data (TPOH). TPOH is valid when the FRMRONLY bit in the S/UNI-JET Configuration 1 register is logic 0. TPOH contains the PLCP path overhead octets (Zn, F1, B1, G1, M1, M2, and C1) which may be inserted in the transmit PLCP frame. The octet data on TPOH is shifted in order from the most significant bit (bit 1) to the least significant bit (bit 8). TPOH is sampled on the rising edge of TPOHCLK.
TDATI			Framer Transmit Data (TDATI). TDATI contains the serial data to be transmitted when the S/UNI-JET is configured as a DS3, E3, or J2 framer device for non-ATM applications by setting the FRMRONLY bit in the S/UNI-JET Configuration 1 Register. TDATI is sampled on the rising edge of TICLK if the TXGAPEN register bit in the S/UNI-JET Configuration 2 register is logic 0. If TXGAPEN is logic 1, then TDATI is sampled on the falling edge of TGAPCLK.

Pin Name	Type	Pin No.	Function
TPOHFP	Output	W14	Transmit Path Overhead Frame Position (TPOHFP). TPOHFP is valid when the FRMRONLY bit in the S/UNI-JET Configuration 1 Register is logic 0. The TPOHFP output locates the individual PLCP path overhead bits in the transmit overhead data stream, TPOH. TPOHFP is logic 1 while bit 1 (the most significant bit) of the path user channel octet (F1) is present in the TPOH stream. TPOHFP is updated on the falling edge of TPOHCLK.
TFPO TMFPO	Output	W14	Framer Transmit Frame Pulse/Multi-frame Pulse Reference (TFPO/TMFPO). TFPO/TMFPO is valid when the S/UNI-JET is configured as a DS3, E3, or J2 framer for non-ATM applications by setting the FRMRONLY bit in the S/UNI-JET Configuration 1 Register to logic 1 and the TXGAPEN bit in the S/UNI-JET Configuration Register to logic 0. TFPO pulses high for 1 out of every 85 clock cycles when configured for DS3, giving a free-running mark for all overhead bits in the frame. TFPO pulses high for 1 out of every 1536 clock cycles when configured for G.751 E3, giving a free-running reference G.751 indication. TFPO pulses high for 1 out of every 4296 clock cycles when configured for G.832 E3, giving a free-running reference G.832 frame indication. TFPO pulses high for 1 out of every 789 clock cycles when configured for J2, giving a free-running reference frame indication. TMFPO pulses high for 1 out of every 4760 clock cycles when configured for DS3, giving a free-running reference M-frame indication. TMFPO pulses high for 1 out of every 3156 clock cycles when configured for J2, giving a free-running reference multi-frame indication. TMFPO behaves the same as TFPO for E3 applications. TFPO/TMFPO is updated on the rising edge of TICLK or RCLK if loop-timed.

Pin Name	Type	Pin No.	Function
TGAPCLK	Output	W14	Framer Gapped Transmit Clock (TGAPCLK). TGAPCLK is valid when the S/UNI-JET is configured as a DS3, E3, or J2 framer for non-ATM applications by setting the FRMRONLY bit in the S/UNI-JET Configuration 1 Register and the TXGAPEN bit in the S/UNI-JET Configuration 2 Register. TGAPCLK is derived from the transmit reference clock TICLK or from the receive clock if loop-timed. The overhead bit (gapped) positions are generated internal to the device. TGAPCLK is held high during the overhead bit positions. This clock is useful for interfacing to devices which source payload data only. TGAPCLK is used to sample TDATI.
TCELL			Transmit Cell Indication (TCELL). TCELL is valid when the TCELL bit in the S/UNI-JET Misc. register is set. TCELL pulses once for every cell (idle or assigned) transmitted. TCELL is updated using timing derived from the transmit input clock (TICLK), and is active for a minimum of 8 TICLK periods (or 8 RCLK periods if loop-timed).
TPOHCLK	Output	U13	Transmit PLCP Overhead Clock (TPOHCLK). TPOHCLK is active when PLCP processing is enabled. TPOHCLK is nominally a 26.7 kHz clock for a DS1 PLCP frame, a 768 kHz clock for a DS3 PLCP frame, a 33.7 kHz clock for an E1 based PLCP frame, and a 576 kHz clock for an G.751 E3 based PLCP frame. TPOHFP is updated on the falling edge of TPOHCLK. TPOH, and TPOHINS are sampled on the rising edge of TPOHCLK.

Pin Name	Type	Pin No.	Function
TIOHM	Input	W15	Transmit Input Overhead Mask (TIOHM). TIOHM is valid only if the FRMRONLY bit in the S/UNI-JET Configuration 1 register is logic 0. TIOHM indicates the position of overhead bits when not configured for DS1, DS3, E1, E3, or J2 transmission system streams. TIOHM is delayed internally to produce the TOHM output. When configured for operation over a DS1, a DS3, an E1, an E3, or a J2 transmission system sublayer, TIOHM is not required, and should be set to logic 0. When configured for other transmission systems, TIOHM is set to logic 1 for each overhead bit position. TIOHM is set to logic 0 if the transmission system contains no overhead bits. TIOHM is sampled on the rising edge of TICLK.
TFPI TMFPI	Input	W15	Framer Transmit Frame Pulse/Multiframe Pulse (TFPI/TMFPI). TFPI/TMFPI is valid when the S/UNI-JET is configured as a DS3, E3, or J2 framer for non-ATM applications by setting the FRMRONLY bit in the S/UNI-JET Configuration 1 Register to logic 1. TFPI indicates the position of all overhead bits in each DS3 M-subframe, the first bit in each G.751 E3 or G.832 E3 frame, or the first framing bit in each J2 frame. TFPI is not required to pulse at every frame boundary in E3 or J2 modes. TMFPI indicates the position of the first bit in each DS3 M-frame, the first bit in each E3 frame, or the first framing bit in each J2 multiframe. TMFPI is not required to pulse at every multiframe boundary. TFPI/TMFPI is sampled on the rising edge of TICLK.
TICLK	Input	V15	Transmit Input Clock (TICLK). TICLK provides the transmit direction timing. TICLK is the externally generated transmission system baud rate clock. It is internally buffered to produce the transmit clock output, TCLK, and can be enabled to update the TPOS/TDATO and TNEG/TOHM outputs on the TICLK rising edge. The TICLK maximum frequency is 52 MHz.

Pin Name	Type	Pin No.	Function
ROHFP	Output	J1	Receive DS3/E3/J2 Overhead Frame Position (ROHFP). ROHFP locates the individual overhead bits in the received overhead data stream, ROH. ROHFP is high during the X1 overhead bit position in the ROH stream when processing a DS3 stream. ROHFP is high during the first bit of the FA1 byte when processing a G.832 E3 stream. ROHFP is high during the RAI overhead bit position when processing a G.751 E3 stream. ROHFP is high during the first bit in Timeslot 97 in the first frame of the 4-frame multiframe when processing a J2 stream. ROHFP is updated on the falling edge of ROHCLK.
ROH	Output	J2	Receive DS3/E3/J2 Overhead Data (ROH). ROH contains the overhead bits (C, F, X, P, and M) extracted from the received DS3 stream; ROH contains the overhead bytes (FA1, FA2, EM, TR, MA, NR, and GC) extracted from the received G.832 E3 stream; ROH contains the overhead bits (RAI, National Use, Stuff Indication, and Stuff Opportunity) extracted from the received G.751 E3 stream; ROH contains the overhead bits (Framing, X_{1-3}, A, M, E_{1-5}) extracted from the received J2 stream. ROH is updated on the falling edge of ROHCLK.
ROHCLK	Output	K4	Receive DS3/E3/J2 Overhead Clock (ROHCLK). ROHCLK is active when a DS3, E3, or J2 stream is being processed. ROHCLK is nominally a 526 kHz clock when processing DS3, a 1.072 MHz clock when processing G.832 E3, a 1.074 MHz clock when processing G.751 E3, and a gapped 6.312 MHz clock with an average frequency of 168 kHz for J2. ROH, and ROHFP are updated on the falling edge of ROHCLK.
REF8KO	Output	U12	Reference 8kHz Output (REF8KO). REF8KO is an 8kHz reference derived from the receive clock (RCLK). A free-running divide-down counter is used to generate REF8KO so it will not glitch on reframe actions. REF8KO will pulse high for approximately 1 RCLK cycle every 125 µs. REF8KO should be treated as a glitch-free asynchronous signal.

Pin Name	Type	Pin No.	Function
RPOHFP			Receive PLCP Overhead Frame Position (RPOHFP). RPOHFP locates the individual PLCP path overhead bits in the receive overhead data stream, RPOH. RPOHFP is logic 1 while bit 1 (the most significant bit) of the path user channel octet (F1) is present in the RPOH stream. RPOHFP is updated on the falling edge of RPOHCLK. RPOHFP is available when the PLCPEN register bit is logic 1 in the SPLR Configuration Register.
RFPO RMFPO	Output	U12	Framer Receive Frame Pulse/Multi-frame Pulse (RFPO/RMFPO). RFPO/RMFPO is valid when the S/UNI-JET is configured to be in framer only mode. The 8KREFO bit must be set to logic 0 in the S/UNI-JET Configuration Register. RFPO is aligned to RDATO and indicates the position of the first bit in each DS3 M-subframe, the first bit in each G.751 E3 or G.832 E3 frame, or the first framing bit in each J2 frame RMFPO is aligned to RDATO and indicates the position of the first bit in each DS3 M-frame, the first bit in each G.751 or G.832 E3 multiframe, or the first framing bit in each J2 multiframe. RFPO/RMFPO is updated on either the falling or rising edge of RSCLK depending on the setting of the RSCLKR bit in the S/UNI-JET Receive Configuration register.
RPOH	Output	V13	Receive PLCP Overhead Data (RPOH). RPOH contains the PLCP path overhead octets (Zn, F1, B1, G1, M1, M2, and C1) extracted from the received PLCP frame when the PLCP layer is in-frame. When the PLCP layer is in the loss of frame state, RPOH is forced to all ones. The octet data on RPOH is shifted out in order from the most significant bit (bit 1) to the least significant bit (bit 8). RPOH is updated on the falling edge of RPOHCLK.

Pin Name	Type	Pin No.	Function
ROVRHD	Output	V13	Framer Receive Overhead Indication (ROVRHD). ROVRHD is valid when the S/UNI-JET is configured as a DS3, E3, or J2 framer for non-ATM applications by setting the FRMRONLY bit in the S/UNI-JET Configuration 1 Register. ROVRHD will be high whenever the data on RDATO corresponds to an overhead bit position. ROVRHD is updated on the either the falling or rising edge of RSCLK depending on the setting of the RSCLKR bit in the S/UNI-JET Receive Configuration register.
RPOHCLK	Output	W13	Receive PLCP Overhead Clock (RPOHCLK). RPOHCLK is active when PLCP processing is enabled. The frequency of this signal depends on the selected PLCP format. RPOHCLK is nominally a 26.7 kHz clock for a DS1 PLCP frame, a 768 kHz clock for a DS3 PLCP frame, a 33.7 kHz clock for an E1 based PLCP frame, or a 576 kHz clock for a G.751 E3 based PLCP frame. RPOHFP and RPOH are updated on the falling edge of RPOHCLK.
RSCLK			Framer Recovered Clock (RSCLK). RSCLK is valid when the S/UNI-JET is configured as a DS3, E3, or J2 framer for non-ATM applications by setting the FRMRONLY bit in the S/UNI-JET Configuration Register. RSCLK is the recovered clock and timing reference for RDATO, RFPO/RMFPO, and ROVRHD.
RGAPCLK]	Output	W13	Framer Recovered Gapped Clock (RGAPCLK). RGAPCLK is valid when the S/UNI-JET is configured as a DS3, E3, or J2 framer for non-ATM applications by setting the FRMRONLY bit in the S/UNI-JET Configuration 1 Register and the RXGAPEN bit in the S/UNI-JET Configuration 2 Register. RGAPCLK is the recovered clock and timing reference for RDATO. RGAPCLK is held high for bit positions which correspond to overhead.

Pin Name	Type	Pin No.	Function
LCD	Output	Y14	Loss of Cell Delineation (LCD). LCD is an active high signal which is asserted while the ATM cell processor has detected a Loss of Cell Delineation defect. The FRMRONLY bit in the S/UNI-JET Configuration 1 Register must be set to logic 0 for LCD to be valid.
RDATO			Framer Receive Data (RDATO). RDATO is valid when the S/UNI-JET is configured as a DS3, E3, or J2 framer for non-ATM applications by setting the FRMRONLY bit in the S/UNI-JET Configuration 1 Register. RDATO is the received data aligned to RFPO/RMFPO and ROVRHD. RDATO is updated on the active edge (as set by the RSCLKR register bit) of RSCLK or RGAPCLK.
FRMSTAT	Output	U1	Framer Status (FRMSTAT). FRMSTAT is an active high signal which can be configured to show when one of the J2, E3, DS3, or PLCP framers have detected certain conditions. The FRMSTAT output can be programmed via the STATSEL[2:0] bits in the S/UNI-JET Configuration 2 Register to indicate: E3/DS3 Loss of Frame or J2 extended Loss of Frame, E3/DS3 Out of Frame or J2 Loss of Frame, PLCP Loss of Frame, PLCP Out of Frame, AIS, Loss of Signal, and DS3 Idle. FRMSTAT should be treated as a glitch free asynchronous signal.
ATM8	Input	L18	ATM Interface Bus Width Selection (ATM8). The ATM8 input pin determines whether the S/UNI-JET works with a 8-bit wide interface (RDAT[7:0] and TDAT[7:0]) or a 16-bit wide interface (RDAT[15:0] and TDAT[15:0]). If ATM8 is set to logic 1, then the 8-bit wide interface is chosen. If ATM8 is set to logic 0, then the 16-bit wide interface is chosen.

Pin Name	Type	Pin No.	Function
TDAT[15] TDAT[14] TDAT[13] TDAT[12] TDAT[11] TDAT[10] TDAT[9] TDAT[8] TDAT[7] TDAT[6] TDAT[5] TDAT[4] TDAT[3] TDAT[2] TDAT[1] TDAT[0]	Input	C15 A16 B16 D15 C16 A17 B17 D16 C17 D18 E17 D19 D20 E18 F17 E19	Transmit Cell Data Bus (TDAT[15:0]). This bus carries the ATM cell octets that are written to the transmit FIFO. TDAT[15:0] is sampled on the rising edge of TFCLK and is considered valid only when TENB is simultaneously asserted and the S/UNI-JET has been selected via the TADR[2:0] inputs. The S/UNI-JET can be configured to operate with an 8-bit wide or 16-bit wide ATM data interface via the ATM8 input pin. When configured for the 8-bit wide interface, TDAT[15:8] are not used and should be tied to ground.
TPRTY	Input	G19	Transmit bus parity (TPRTY). The transmit parity (TPRTY) signal indicates the parity of the TDAT[15:0] or TDAT[7:0] bus. If configured for the 8-bit bus (via the ATM8 input pin), then parity is calculated over TDAT[7:0]. If configured for the 16-bit bus, then parity is calculated over TDAT[15:0]. A parity error is indicated by a status bit and a maskable interrupt. Cells with parity errors are inserted in the transmit stream, so the TPRTY input may be unused. Odd or even parity selection is made using the TPTYP register bit. TPRTY is sampled on the rising edge of TFCLK and is considered valid only when TENB is simultaneously asserted and the S/UNI-JET has been selected via the TADR[2:0] inputs.

Pin Name	Type	Pin No.	Function
TSOC	Input	G20	Transmit Start of Cell (TSOC). The transmit start of cell (TSOC) signal marks the start of cell on the TDAT bus. When TSOC is high, the first word of the cell structure is present on the TDAT bus. It is not necessary for TSOC to be present for each cell. An interrupt may be generated if TSOC is high during any word other than the first word of the cell structure. TSOC is sampled on the rising edge of TFCLK and is considered valid only when TENB is simultaneously asserted and the S/UNI-JET has been selected via the TADR[2:0] inputs.
TENB	Input	H18	Transmit Multi-Phy Write Enable (TENB). The TENB signal is an active low input which is used along with the TADR[2:0] inputs to initiate writes to the transmit FIFO. When sampled low using the rising edge of TFCLK, the word on the TDAT bus is written into the transmit FIFO selected by the TADR[2:0] address bus. When sampled high using the rising edge of TFCLK, no write is performed, but the TADR[2:0] address is latched to identify the transmit FIFO to be accessed. A complete 53 octet cell must be written to the transmit FIFO before it is inserted into the transmit stream. Idle cells are inserted when a complete cell is not available.
TADR[2] TADR[1] TADR[0]	Input	F18 F19 F20	Transmit Address (TADR[2:0]). The TADR[2:0] bus is used for device selection and device polling in accordance with the Utopia Level 2 standard. When TADR[2:0] is set to the same value as the PHY_ADR[2:0] inputs than the transmit interface of this S/UNI-JET is either being selected or polled. Note that the null-phy address 7H is an invalid address and cannot be used to select the S/UNI-JET. TADR[2:0] is sampled on the rising edge of TFCLK.

Pin Name	Type	Pin No.	Function
TCA	Output	H19	Transmit Multi-Phy Cell Available (TCA). The TCA signal indicates when a cell is available in the transmit FIFO for the device selected by TADR[2:0]. When high, TCA indicates that the corresponding transmit FIFO is not full and a complete cell may be written. When TCA goes low, it can be configured to indicate either that the corresponding transmit FIFO is near full or that the corresponding transmit FIFO is full. TCA will transition low on the rising edge of TFCLK which samples Payload byte 43 (TCALEVEL0=0) or 47 (TCALEVEL0=1) for the 8-bit interface (ATM8=1), or the rising edge of TFCLK which samples Payload word 19 (TCALEVEL0=0) or 23 (TCALEVEL0=1) for the 16-bit interface (ATM8=0) if the device being polled is the same as the selected device. To reduce FIFO latency, the FIFO depth at which TCA indicates "full" can be set to one, two, three or four cells. Note that regardless of what fill level TCA is set to indicate "full" at, the transmit cell processor can store 4 complete cells. TCA is tri-stated when either the null-PHY address (7H) or an address not matching the address space set by PHY_ADR[2:0] is latched (by TFCLK) from the TADR[2:0] inputs. The polarity of TCA (with respect the the description above) is inverted when the TCAINV register bit is set to logic 1.
TFCLK	Input	E20	Transmit FIFO Write Clock (TFCLK). This signal is used to write ATM cells to the four cell transmit FIFOs. TFCLK cycles at a 52 MHz or lower instantaneous rate.

Pin Name	Type	Pin No.	Function
DTCA	Output	J17	Direct Access Transmit Cell Available (DTCA). These output signals indicate when a cell is available in the transmit FIFO. When high, DTCA indicates that the corresponding transmit FIFO is not full and a complete cell may be written. DTCA can be configured to indicate either that the corresponding transmit FIFO is near full and can accept no more than four writes or that the corresponding transmit FIFO is full. DTCA will thus transition low on the rising edge of TFCLK which samples Payload byte 43 (TCALEVEL0=0) or 47 (TCALEVEL0=1) for the 8-bit interface (ATM8=1), or the rising edge of TFCLK which samples Payload word 19 (TCALEVEL0=0) or 23 (TCALEVEL0=1) for the 16-bit interface (ATM8=0). To reduce FIFO latency, the FIFO depth at which DTCA indicates "full" can be set to one, two, three or four cells. Note that regardless of what fill level DTCA is set to indicate "full" at, the transmit cell processor can store 4 complete cells. The polarity of DTCA (with respect the the description above) is inverted when the TCAINV register bit is set to logic 1. The DTCA outputs can be used to support Utopia Direct Access mode.

Pin Name	Type	Pin No.	Function
RDAT[15] RDAT[14] RDAT[13] RDAT[12] RDAT[11] RDAT[10] RDAT[9] RDAT[8] RDAT[7] RDAT[6] RDAT[5] RDAT[4] RDAT[3] RDAT[2] RDAT[1] RDAT[0]	Output	T20 T19 R17 T18 U20 U19 T17 U18 V17 U16 W17 Y17 V16 U15 W16 Y16	Receive Cell Data Bus (RDAT[15:0]). This bus carries the ATM cell octets that are read from the receive ATM FIFO selected by RADR[2:0]. RDAT[15:0] is tri-stated when RENB is high. RDAT[15:0] is updated on the rising edge of RFCLK. The S/UNI-JET can be configured to operate with an 8-bit wide or 16-bit wide ATM data interface via the ATM8 input pin. RDAT[15:8] will remain tri-stated if ATM8 is set to logic 1. RDAT[15:0] is tri-stated when either the null-PHY address (7H) or an address not matching the address space set by PHY_ADR[2:0] is latched from the RADR[2:0] inputs when RENB is high.
RPRTY	Output	R18	Receive Parity (RPRTY). The receive parity (RPRTY) signal indicates the parity of the RDAT bus. The S/UNI-JET can be configured to operate with an 8-bit wide or 16-bit wide ATM data interface via the ATM8 input pin. In the 8-bit mode, RPRTY reflects the parity of RDAT[7:0]. In the 16-bit mode, RPRTY reflects the parity of RDAT[15:0]. Odd or even parity selection is made using the RXPTYP register bit. RPRTY is tri-stated when either the null-PHY address (7H) or an address not matching the address space set by PHY_ADR[2:0] is latched from the RADR[2:0] inputs when RENB is high.

Pin Name	Type	Pin No.	Function
RSOC	Output	M17	Receive Start of Cell (RSOC). This signal marks the start of cell on the RDAT bus. RSOC marks the start of the cell on the RDAT bus. RSOC is tri-stated when either the null-PHY address (7H) or an address not matching the address space set by PHY_ADR[2:0] is latched from the RADR[2:0] inputs when RENB is high.
RENB	Input	N18	Receive Multi-Phy Read Enable (RENB). The RENB signal is used to initiate reads from the receive FIFO. When sampled low using the rising edge of RFCLK, a byte is read (if one is available) from the receive FIFO selected by the RADR[2:0] address bus and output on the RDAT bus. When sampled high using the rising edge of RFCLK, no read is performed and RDAT[15:0], RPRTY, and RSOC are tri-stated, and the address on RADR[2:0] is latched to select the device or port for the next ATM FIFO access. RENB must operate in conjunction with RFCLK to access the FIFOs at a high enough rate to prevent FIFO overflows. The ATM layer device may de-assert RENB at anytime it is unable to accept another byte.
RADR[2] RADR[1] RADR[0]	Input	P19 N17 P18	Receive Address (RADR[2:0]). The RADR[2:0] bus is used for device selection and device polling in accordance with the Utopia Level 2 standard. When RADR[2:0] is set to the same value as the PHY_ADR[2:0] inputs than the receive interface of this S/UNI-JET is either being selected or polled. Note that the null phy address 7H is an invalid address and cannot be used to select the S/UNI-JET. RADR[2:0] is sampled on the rising edge of TFCLK.

Pin Name	Type	Pin No.	Function
RCA	Output	N19	Receive Multi-Phy Cell Available (RCA). The RCA signal indicates when a cell is available in the receive FIFO for the device selected by RADR[2:0]. RCA can be configured to be de-asserted when either zero or four bytes remain in the selected/addressed FIFO. RCA will thus transition low on the rising edge of RFCLK after Payload byte 48 (RCALEVEL0=1) or 43 (RCALEVEL0=0) is output for the 8-bit interface (ATM8=1), or after Payload word 24 (RCALEVEL0=1) or 19 (RCALEVEL0=0) is output for the 16-bit interface (ATM8=0) if the PHY being polled is the same as the selected device. RCA is tri-stated when either the null-PHY address (7H) or an address not matching the address space set by PHY_ADR[2:0] is latched (by RFCLK) from the RADR[2:0] inputs. The polarity of RCA (with respect to the description above) is inverted when the RCAINV register bit is set to logic 1.
RFCLK	Input	P20	Receive FIFO Read Clock (RFCLK). This signal is used to read ATM cells from the receive FIFOs. RFCLK must cycle at a 52 MHz or lower instantaneous rate, but at a high enough rate to avoid FIFO overflows.
DRCA	Output	L17	Direct Access Receive Cell Available (DRCA). These output signals indicate when a cell is available in the receive FIFO. DRCA can be configured to be de-asserted when either zero or four bytes remain in the FIFO. DRCA will thus transition low on the rising edge of RFCLK after Payload byte 48 (RCALEVEL0=1) or 43 (RCALEVEL0=0) is output for the 8-bit interface (ATM8=1), or after Payload word 24 (RCALEVEL0=1) or 19 (RCALEVEL0=0) is output for the 16-bit interface (ATM8=0). The DRCA outputs can be used to support Utopia Direct Access mode.

Pin Name	Type	Pin No.	Function
PHY_ADR[2] PHY_ADR[1] PHY_ADR[0]	Input	K18 L20 L19	Device Identification Address (PHY_ADR[2:0]). The PHY_ADR[2:0] inputs represent the address space which this S/UNI-JET occupies. When the PHY_ADR[2:0] inputs match the TADR[2:0] or RADR[2:0] inputs, then this S/UNI-JET is selected for transmit or receive ATM access. Note that the null-PHY address 7H is an invalid address and will not select the S/UNI-JET. The S/UNI-JET can be used directly in applications requiring 7 or fewer ports. Applications requiring more than 7 ports may require external decoding of the Utopia address to avoid bus contention.
CSB	Input	C9	Active low Chip Select (CSB). This signal must be low to enable S/UNI-JET register accesses. If CSB is not used, (RDB and WRB determine register reads and writes) then it should be tied to an inverted version of RSTB.
WRB	Input	B8	Active low Write Strobe (WRB). This signal is pulsed low to enable a S/UNI-JET register write access. The D[7:0] bus is clocked into the addressed register on the rising edge of WRB while CSB is low.
RDB	Input	D9	Active low Read Enable (RDB). This signal is pulsed low to enable a S/UNI-JET register read access. The S/UNI-JET drives the D[7:0] bus with the contents of the addressed register while RDB and CSB are both low.
D[7] D[6] D[5] D[4] D[3] D[2] D[1] D[0]	I/O	D12 C13 A14 B14 D13 C14 A15 B15	Bi-directional Data Bus (D[7:0]). The bi-directional data bus D[7:0] is used during S/UNI-JET register read and write accesses.

Pin Name	Type	Pin No.	Function
A[10] A[9] A[8] A[7] A[6] A[5] A[4] A[3] A[2] A[1] A[0]	Input	B9 B10 C10 A11 B11 C11 D11 A12 B12 C12 B13	Address Bus (A[10:0]). The address bus A[10:0] selects specific registers during S/UNI-JET register accesses.
RSTB	Input	C8	Active low Reset (RSTB). This signal is set low to asynchronously reset the S/UNI-JET. RSTB is a Schmitt-trigger input with an integral pull-up resistor.
ALE	Input	A8	Address Latch Enable (ALE). The address latch enable (ALE) is active-high and latches the address bus A[10:0] when low. When ALE is high, the internal address latches are transparent. It allows the S/UNI-JET to interface to a multiplexed address/data bus. ALE has an integral pull-up resistor.
INTB	Output	A7	Active low Open-Drain Interrupt (INTB). This signal goes low when an unmasked interrupt event is detected on any of the internal interrupt sources. Note that INTB will remain low until all active, unmasked interrupt sources are acknowledged at their source.
TCK	Input	B6	Test Clock (TCK). This signal provides timing for test operations that can be carried out using the IEEE P1149.1 test access port.
TMS	Input	C7	Test Mode Select (TMS). This signal controls the test operations that can be carried out using the IEEE P1149.1 test access port. TMS is sampled on the rising edge of TCK. TMS has an integral pull up resistor.

Pin Name	Type	Pin No.	Function
TDI	Input	D8	Test Data Input (TDI). This signal carries test data into the S/UNI-JET via the IEEE P1149.1 test access port. TDI is sampled on the rising edge of TCK. TDI has an integral pull up resistor.
TDO	Output	B7	Test Data Output (TDO). This signal carries test data out of the S/UNI-JET via the IEEE P1149.1 test access port. TDO is updated on the falling edge of TCK. TDO is a tri-state output which is inactive except when scanning of data is in progress.
TRSTB	Input	A6	Active low Test Reset (TRSTB). This signal provides an asynchronous S/UNI-JET test access port reset via the IEEE P1149.1 test access port. TRSTB is a Schmitt triggered input with an integral pull up resistor. TRSTB must be asserted during the power up sequence. Note that if not used, TRSTB must be connected to the RSTB input.
BIAS	Input	H20 U17 D4 U4	+5V Bias (BIAS). When tied to +5V, the BIAS input is used to bias the wells in the input and I/O pads so that the pads can tolerate 5V on their inputs without forward biasing internal ESD protection devices. When tied to VDD, the inputs and bi-directional inputs will only tolerate input levels up to VDD.

Pin Name	Type	Pin No.	Function
VDD[1]	Power	B2	DC Power. The DC Power pins should be connected to a well-decoupled +3.3V DC supply.
VDD[2]		B3	
VDD[3]		B18	
VDD[4]		B19	
VDD[5]		C2	
VDD[6]		C3	
VDD[7]		C18	
VDD[8]		C19	
VDD[9]		D7	
VDD[10]		D10	
VDD[11]		D14	
VDD[12]		G4	
VDD[13]		G17	
VDD[14]		G18	
VDD[15]		H17	
VDD[16]		K17	
VDD[17]		L4	
VDD[18]		P4	
VDD[19]		P17	
VDD[20]		R19	
VDD[21]		R20	
VDD[22]		U7	
VDD[23]		U11	
VDD[24]		U14	
VDD[25]		V2	
VDD[26]		V3	
VDD[27]		V18	
VDD[28]		V19	
VDD[29]		W2	
VDD[30]		W3	
VDD[31]		W18	
VDD[32]		W19	

Pin Name	Type	Pin No.	Function
VSS[1]	Ground	A1	DC Ground. The DC Ground pins should be connected to GND.
VSS[2]		A2	
VSS[3]		A3	
VSS[4]		A9	
VSS[5]		A10	
VSS[6]		A13	
VSS[7]		A18	
VSS[8]		A19	
VSS[9]		A20	
VSS[10]		B1	
VSS[11]		B20	
VSS[12]		C1	
VSS[13]		C20	
VSS[14]		D1	
VSS[15]		E1	
VSS[16]		E2	
VSS[17]		E3	
VSS[18]		F3	
VSS[19]		F4	
VSS[20]		G1	
VSS[21]		G2	
VSS[22]		H1	
VSS[23]		H4	
VSS[24]		J20	
VSS[25]		K2	
VSS[26]		K3	
VSS[27]		K20	
VSS[28]		L1	
VSS[29]		M1	
VSS[30]		M4	
VSS[31]		N1	
VSS[32]		N20	

Pin Name	Type	Pin No.	Function
VSS[33]	Ground	P3	DC Ground. The DC Ground pins should be connected to GND.
VSS[34]		R1	
VSS[35]		U9	
VSS[36]		V1	
VSS[37]		V6	
VSS[38]		V9	
VSS[39]		V12	
VSS[40]		V20	
VSS[41]		W1	
VSS[42]		W5	
VSS[43]		W6	
VSS[44]		W8	
VSS[45]		W9	
VSS[46]		W11	
VSS[47]		W12	
VSS[48]		W20	
VSS[49]		Y1	
VSS[50]		Y2	
VSS[51]		Y3	
VSS[52]		Y5	
VSS[53]		Y8	
VSS[54]		Y11	
VSS[55]		Y12	
VSS[56]		Y13	
VSS[57]		Y18	
VSS[58]		Y19	
VSS[59]		Y20	

Pin Name	Type	Pin No.	Function
NC[1]	No-Connect	B4	These pins are No-Connects
NC[2]		C4	
NC[3]		D2	
NC[4]		D3	
NC[5]		D5	
NC[6]		D17	
NC[7]		E4	
NC[8]		F1	
NC[9]		F2	
NC[10]		G3	
NC[11]		J18	
NC[12]		J19	
NC[13]		K1	
NC[14]		K19	
NC[15]		L2	
NC[16]		L3	
NC[17]		M2	
NC[18]		M3	
NC[19]		M18	
NC[20]		M19	
NC[21]		M20	
NC[22]		N2	
NC[23]		N3	
NC[24]		N4	
NC[25]		P1	
NC[26]		P2	
NC[27]		R2	
NC[28]		R3	
NC[29]		R4	
NC[30]		T1	
NC[31]		T2	
NC[32]		T4	

Pin Name	Type	Pin No.	Function
NC[33]	No-Connect	U2	These pins are No-Connects
NC[34]		U3	
NC[35]		U5	
NC[36]		U6	
NC[37]		U8	
NC[38]		U10	
NC[39]		V4	
NC[40]		V5	
NC[41]		V7	
NC[42]		V8	
NC[43]		V10	
NC[44]		V11	
NC[45]		W4	
NC[46]		W7	
NC[47]		W10	
NC[48]		Y4	
NC[49]		Y6	
NC[50]		Y7	
NC[51]		Y9	
NC[52]		Y10	

Notes on Pin Description:

1. All S/UNI-JET inputs and bi-directionals present minimum capacitive loading and operate at TTL logic levels.

2. All S/UNI-JET outputs and bi-directionals have at least 3 mA drive capability. The data bus outputs, D[7:0], have 3 mA drive capability. The FIFO interface outputs, RDAT[15:0], RPRTY, RCA, DRCA, RSOC, TCA, and DTCA, have 12 mA drive capability. The outputs TCLK, TPOS/TDATO, TNEG/TOHM, TPOHFP/TFPO/TMFPO/TGAPCLK, LCD/RDATO, RPOH/ROVRHD, RPOHCLK/RSCLK/RGAPCLK, and REF8KO/RPOHFP/RFPO/RMFPO have 6 mA drive capability. All other outputs have 3 mA drive capability.

3. Inputs RSTB, ALE, TMS, TDI and TRSTB have internal pull-up resistors.

4. RSTB, TRSTB, TMS, TDI, TCK, REF8KI, TFCLK, RFCLK, TICLK, and RCLK are schmitt trigger input pads.

5. The VSS [59:1] ground pins are not internally connected together. Failure to connect these pins externally may cause malfunction or damage the S/UNI-JET.

6. The VDD[32:1] power pins are not internally connected together. Failure to connect these pins externally may cause malfunction or damage the device. These power supply connections must all be utilized and must all connect to a common +3.3 V or ground rail, as appropriate.

7. During power-up and power-down, the voltage on the BIAS pin must be kept equal to or greater than the voltage on the VDD [32:1] pins, to avoid damage to the device.

6.1 JTAG Test Access Port

The JTAG Test Access Port block provides JTAG support for boundary scan. The standard JTAG EXTEST, SAMPLE, BYPASS, IDCODE and STCTEST instructions are supported. The S/UNI-JET identification code is 073460CD hexadecimal.

6.2 Microprocessor Interface

The microprocessor interface block provides normal and test mode register, and the logic required to connect to the microprocessor interface. The normal mode registers are required for normal operation, and test mode register are used to enhance the testability of the S/UNI-JET. With the exception of the S/UNI-JET Identification register, all register descriptions can be found in the S/UNI-QJET datasheet (PMC-960835). The register set is accessed as follows:

Table 2 - Register Memory Map

Address	Register
000H-2FFH	Reserved
300H	S/UNI-JET Configuration 1
301H	S/UNI-JET Configuration 2
302H	S/UNI-JET Transmit Configuration
303H	S/UNI-JET Receive Configuration
304H	S/UNI-JET Data Link and FERF/RAI Control
305H	S/UNI-JET Interrupt Status
006H	S/UNI-JET Identification, Master Reset, and Global Monitor Update
306H	S/UNI-JET Reserved
307H	S/UNI-JET Clock Activity Monitor and Interrupt Identification
308H	SPLR Configuration
309H	SPLR Interrupt Enable
30AH	SPLR Interrupt Status
30BH	SPLR Status
30CH	SPLT Configuration
30DH	SPLT Control
30EH	SPLT Diagnostics and G1 Octet
30FH	SPLT F1 Octet
310H	PMON Change of PMON Performance Meters
311H	PMON Interrupt Enable/Status
312H-313H	PMON Reserved

Address	Register
314H	PMON Line Code Violation Event Count LSB
315H	PMON Line Code Violation Event Count MSB
316H	PMON Framing Bit Error Event Count LSB
317H	PMON Framing Bit Error Event Count MSB
318H	PMON Excessive Zeros Count LSB
319H	PMON Excessive Zeros Count MSB
31AH	PMON Parity Error Event Count LSB
31BH	PMON Parity Error Event Count MSB
31CH	PMON Path Parity Error Event Count LSB
31DH	PMON Path Parity Error Event Count MSB
31EH	PMON FEBE/J2-EXZS Event Count LSB
31FH	PMON FEBE/J2-EXZS Event Count MSB
320H	CPPM Reserved
321H	CPPM Change of CPPM Performance Meter
322H	CPPM BIP Error Count LSB
323H	CPPM BIP Error Count MSB
324H	CPPM PLCP Framing Error Event Count LSB
325H	CPPM PLCP Framing Error Event Count MSB
326H	CPPM PLCP FEBE Count LSB
327H	CPPM PLCP FEBE Count MSB
328H-32FH	CPPM Reserved
330H	DS3 FRMR Configuration
331H	DS3 FRMR Interrupt Enable
332H	DS3 FRMR Interrupt Status
333H	DS3 FRMR Status
334H	DS3 TRAN Configuration
335H	DS3 TRAN Diagnostics
336H-337H	DS3 TRAN Reserved
338H	E3 FRMR Framing Options

Address	Register
339H	E3 FRMR Maintenance Options
33AH	E3 FRMR Framing Interrupt Enable
33BH	E3 FRMR Framing Interrupt Indication and Status
33CH	E3 FRMR Maintenance Event Interrupt Enable
33DH	E3 FRMR Maintenance Event Interrupt Indication
33EH	E3 FRMR Maintenance Event Status
33FH	E3 FRMR Reserved
340H	E3 TRAN Framing Options
341H	E3 TRAN Status and Diagnostic Options
342H	E3 TRAN BIP-8 Error Mask
343H	E3 TRAN Maintenance and Adaptation Options
344H	J2 FRMR Configuration
345H	J2 FRMR Status
346H	J2 FRMR Alarm Interrupt Enable
347H	J2 FRMR Alarm Interrupt Status
348H	J2 FRMR Error/X-bit Interrupt Enable
349H	J2 FRMR Error/X-bit Interrupt Status
34AH-34BH	J2 FRMR Reserved
34CH	J2 TRAN Configuration
34DH	J2 TRAN Diagnostics
34EH	J2 TRAN TS97 Signaling
34FH	J2 TRAN TS98 Signaling
350H	RDLC Configuration
351H	RDLC Interrupt Control
352H	RDLC Status
353H	RDLC Data
354H	RDLC Primary Address Match
355H	RDLC Secondary Address Match
356H	RDLC Reserved

Address	Register
357H	RDLC Reserved
358H	TDPR Configuration
359H	TDPR Upper Transmit Threshold
35AH	TDPR Lower Interrupt Threshold
35BH	TDPR Interrupt Enable
35CH	TDPR Interrupt Status/UDR Clear
35DH	TDPR Transmit Data
35EH-35FH	TDPR Reserved
360H	RXCP-50 Configuration 1
361H	RXCP-50 Configuration 2
362H	RXCP-50 FIFO/UTOPIA Control & Config
363H	RXCP-50 Interrupt Enables and Counter Status
364H	RXCP-50 Status/Interrupt Status
365H	RXCP-50 LCD Count Threshold (MSB)
366H	RXCP-50 LCD Count Threshold (LSB)
367H	RXCP-50 Idle Cell Header Pattern
368H	RXCP-50 Idle Cell Header Mask
369H	RXCP-50 Corrected HCS Error Count
36AH	RXCP-50 Uncorrected HCS Error Count
36BH	RXCP-50 Received Cell Count LSB
36CH	RXCP-50 Received Cell Count
36DH	RXCP-50 Received Cell Count MSB
36EH	RXCP-50 Idle Cell Count LSB
36FH	RXCP-50 Idle Cell Count
370H	RXCP-50 Idle Cell Count MSB
371H-37FH	RXCP-50 Reserved
380H	TXCP-50 Configuration 1
381H	TXCP-50 Configuration 2
382H	TXCP-50 Transmit Cell Status

Address	Register
383H	TXCP-50 Interrupt Enable/Status
384H	TXCP-50 Idle Cell Header Control
385H	TXCP-50 Idle Cell Payload Control
386H	TXCP-50 Transmit Cell Counter LSB
387H	TXCP-50 Transmit Cell Counter
388H	TXCP-50 Transmit Cell Counter MSB
389H-38FH	TXCP-50 Reserved
390H	TTB Control Register
391H	TTB Trail Trace Identifier Status
392H	TTB Indirect Address Register
393H	TTB Indirect Data Register
394H	TTB Expected Payload Type Label Register
395H	TTB Payload Type Label Control/Status
396H-397H	TTB Reserved
398H	RBOC Configuration/Interrupt Enable
399H	RBOC Status
39AH	XBOC Code
39BH	S/UNI-JET Misc.
39CH	S/UNI-JET FRMR LOF Status.
3A0H	PRGD Control
3A1H	PRGD Interrupt Enable/Status
3A2H	PRGD Length
3A3H	PRGD Tap
3A4H	PRGD Error Insertion
3A5H-3A7H	PRGD Reserved
3A8H	PRGD Pattern Insertion Register #1
3A9H	PRGD Pattern Insertion Register #2
3AAH	PRGD Pattern Insertion Register #3
3ABH	PRGD Pattern Insertion Register #4

Address	Register
3ACH	PRGD Pattern Detector Register #1
3ADH	PRGD Pattern Detector Register #2
3AEH	PRGD Pattern Detector Register #3
3AFH	PRGD Pattern Detector Register #4
3B0H-3FFH	S/UNI-JET Reserved
400H	S/UNI-JET Master Test Register
401H-40BH	Reserved for S/UNI-JET Test
40CH	S/UNI-JET Identification Register
40DH - 7FFH	Reserved for S/UNI-JET Test

Notes:

1. For all register accesses, CSB must be low.

2. Writing any value to any of the PMON(314H to 31FH), RXCP-50(369H to 370H) or TXCP-50(386H to 388H) counter holding registers will latch the current count value to the holding registers. To ensure that the transfer was completed a wait function must be performed via software as indicated by the specific count registers being latched. Each of the above mentioned registers have a specified clock cycle completion requirement that is stated in the specific count registers description. For example the LCV PMON count of registers 314H and 315H specifies that it takes 3 RCLK cycles to complete a transfer of the current count value to the count holding registers. Other registers may specify a different clock cycle requirement for the three different operational modes of the JET: DS3, E3 and J2.

Register 006H: S/UNI-QJET Identification, Master Reset, and Global Monitor Update

Bit	Type	Function	Default
Bit 7	R/W	RESET	0
Bit 6	R	TYPE[3]	1
Bit 5	R	TYPE[2]	0
Bit 4	R	TYPE[1]	0
Bit 3	R	TYPE[0]	0
Bit 2	R	Reserved	X
Bit 1	R	ID[1]	1
Bit 0	R	ID[0]	0

This register is used for global performance monitor updates, global software resets, and for device identification. Writing any value except 80H into this register initiates latching of all performance monitor counts in the PMON, RXCP-50, and TXCP-50 blocks in all four quadrants of the S/UNI-QJET. The TIP register bit is used to signal when the latching is complete.

The CPPM counter registers are **not** latched by writing to register 006H. Counters in the CPPM can only be updated by writing to CPPM register addresses (x22H – x2FH).

RESET:

The RESET bit allows software to asynchronously reset the S/UNI-QJET. The software reset is equivalent to setting the RSTB input pin low, except that the S/UNI-QJET Master Test Register is not affected. When a logic 1 is written to RESET, the S/UNI-QJET is reset. When a logic 0 is written to RESET, the reset is removed. The RESET bit must be explicitly set and cleared by writing the corresponding logic value to this register.

TYPE[3:0]:

The TYPE[3:0] bits allow software to identify this device as the S/UNI-QJET member of the S/UNI family of products.

Reserved:

The reserved bit must be a not connect.

ID[1:0]:

The ID[1:0] bits allows software to identify the version level of the S/UNI-QJET.

Register 40CH: S/UNI-JET Identification Register

Bit	Type	Function	Default
Bit 7	R	Reserved	X
Bit 6	R	Device_ID	1
Bit 5	R	Reserved	X
Bit 4	R	Reserved	X
Bit 3	R	Reserved	X
Bit 2	R	Reserved	X
Bit 1	R	Reserved	X
Bit 0	R	Reserved	X

This register provides a device identification to distinguish the S/UNI-JET from a S/UNI-QJET in applications where the S/UNI-QJET is used for prototype purposes.

DEVICE_ID:

The DEVICE_ID bit allows software to identify the device as a S/UNI-JET. A logic one identifies the device as a S/UNI-JET, whereas a logic zero identifies the device as a S/UNI-QJET. To access this register, the IOTST bit in the S/UNI-QJET Master Test register must first be set to logic one. The Device_ID bit can now be read. A logic zero must then be written back to the IOTST bit to put the device back into normal mode of operation.

7 TEST FEATURES DESCRIPTION

Simultaneously asserting (low) the CSB, RDB and WRB inputs causes all digital output pins and the data bus to be held in a high-impedance state. This test feature may be used for board testing.

Test mode registers are used to apply test vectors during production testing of the S/UNI-JET. Test mode registers (as opposed to normal mode registers) are selected when A[10] is high.

Test mode registers may also be used for board testing. When all of the TSBs within the S/UNI-JET are placed in test mode 0, device inputs may be read and device outputs may be forced via the microprocessor interface (refer to the section "Test Mode 0" for details).

In addition, the S/UNI-JET also supports a standard IEEE 1149.1 five-signal JTAG boundary scan test port for use in board testing. All digital device inputs may be read and all digital device outputs may be forced via the JTAG test port.

Table 3 - Test Mode Register Memory Map

Address	Register
000H-3FFH	Normal Mode Registers
400H	Master Test Register
708H	SPLR Test Register 0
709H	SPLR Test Register 1
70AH	SPLR Test Register 2
70BH	Reserved
70CH	SPLT Test Register 0
70DH	SPLT Test Register 1
70EH	SPLT Test Register 2
70FH	SPLT Test Register 3
710H	PMON Test Register 0
711H	PMON Test Register 1
712H-71FH	Reserved
720H	CPPM Test Register 0
721H	CPPM Test Register 1
722H	CPPM Test Register 2

Address	Register
723H-72FH	Reserved
730H	DS3 FRMR Test Register 0
731H	DS3 FRMR Test Register 1
732H	DS3 FRMR Test Register 2
733H	DS3 FRMR Test Register 3
734H	DS3 TRAN Test Register 0
735H	DS3 TRAN Test Register 1
736H	DS3 TRAN Test Register 2
737H	Reserved
738H	E3 FRMR Test Register 0
739H	E3 FRMR Test Register 1
73AH	E3 FRMR Test Register 2
73BH-73FH	Reserved
740H	E3 TRAN Test Register 0
741H	E3 TRAN Test Register 1
742H	E3 TRAN Test Register 2
743H	Reserved
744H	J2 FRMR Test Register 0
745H	J2 FRMR Test Register 1
746H	J2 FRMR Test Register 2
747H	J2 FRMR Test Register 3
748H-74BH	Reserved
74CH	J2 TRAN Test Register 0
74DH	J2 TRAN Test Register 1
74EH	J2 TRAN Test Register 2
74FH	J2 TRAN Test Register 3
750H	RDLC Test Register 0
751H	RDLC Test Register 1
752H	RDLC Test Register 2

Address	Register
753H	RDLC Test Register 3
754H	RDLC Test Register 4
755H-757H	Reserved
758H	TDPR Test Register 0
759H	TDPR Test Register 1
75AH	TDPR Test Register 2
75BH	TDPR Test Register 3
75CH-75FH	Reserved
760H	RXCP-50 Test Register 0
761H	RXCP-50 Test Register 1
762H	RXCP-50 Test Register 2
763H	RXCP-50 Test Register 3
764H	RXCP-50 Test Register 4
765H	RXCP-50 Test Register 5
766H-77FH	Reserved
780H	TXCP-50 Test Register 0
781H	TXCP-50 Test Register 1
782H	TXCP-50 Test Register 2
783H	TXCP-50 Test Register 3
784H	TXCP-50 Test Register 4
785H	TXCP-50 Test Register 5
786H-78FH	Reserved
790H	TTB Test Register 0
791H	TTB Test Register 1
792H	TTB Test Register 2
793H-797H	Reserved
798H	RBOC Test Register 0
799H	RBOC Test Register 1
79AH	XBOC Test Register 1

Address	Register
79BH	XBOC Test Register 0
79CH-79FH	Reserved
7A0H	PRGD Test Register 0
7A1H	PRGD Test Register 1
7A2H	PRGD Test Register 2
7A3H	PRGD Test Register 3
7A4H-7FFH	Reserved

Notes on Test Mode Register Bits:

1. Writing values into unused register bits has no effect. However, to ensure software compatibility with future, feature-enhanced versions of the product, unused register bits must be written with logic zero. Reading back unused bits can produce either a logic one or a logic zero; hence, unused register bits should be masked off by software when read.

2. Writable test mode register bits are not initialized upon reset unless otherwise noted.

7.1 Test Mode 0 Details

In test mode 0, the S/UNI-JET allows the logic levels on the device inputs to be read through the microprocessor interface and allows the device outputs to be forced to either logic level through the microprocessor interface. The IOTST bit in the S/UNI-JET Master Test register must be set to logic one to access the device I/O.

To enable test mode 0, the IOTST bit in the S/UNI-JET Master Test register is set to logic one and the device should be left in its default state after reset unless otherwise noted. All Test Register 1 locations of all blocks must be written with the value 0 (see Table 3).

Reading the following address locations returns the values on the indicated inputs:

Table 4 - Test Mode 0 Input Read Address Locations

Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
40CH		Device_ID						
430H								
436H								
444H								
465H							RENB[3]	

Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
466H	RADR[2][4]	RADR[1][4]	RADR[0][4]					RFCLK
480H				ATM8				
482H	PHY_ADR[2]	TADR[2][1]			TSOC	TENB[2]	TPRTY	TFCLK
483H	PHY_ADR[1]	PHY_ADR[0]			TADR[1] [1]	TADR[0] [1]		
484H	TDAT[15]	TDAT[14]	TDAT[13]	TDAT[12]	TDAT[11]	TDAT[10]	TDAT[9]	TDAT[8]
485H	TDAT[7]	TDAT[6]	TDAT[5]	TDAT[4]	TDAT[3]	TDAT[2]	TDAT[1]	TDAT[0]
50CH								
50FH								REF8KI
530H								
536H								
544H								
565H								
60CH								
630H								
636H								
644H								
665H							RADR[0][4]	
70CH		TIOHM	TICLK	TPOH	TPOHINS			
730H								RCLK
736H							TOH	TOHINS
744H					RPOS	RNEG		
765H							RADR[1][4]	

1. Before reading these values, the input must be set to the test state, TENB must be set to logic 1, and TFCLK must transition from logic 0 to logic 1.

2. TENB must be set to its test state and TFCLK must transition from logic 0 to logic 1 before its value will be captured in the test register.

3. RENB must be set to its test state and RFCLK must transition from logic 0 to logic 1 before its value will be captured in the test register.

4. Before reading these values, the input must be set to the test state, RENB must be set to logic 1, and RFCLK must transition from logic 0 to logic 1.

Writing the following address locations forces the outputs to the value in the corresponding bit position (zeros should be written to all unused test register locations):

Table 5 - Test Mode 0 Output Write Address Locations

Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
408H								
40AH								INTB[1]
40CH								
410H								INTB[1]
430H	INTB[1]							
434H								
436H								
432H								
433H								
44CH								
44EH								
450H								INTB[1]
458H								INTB[1]
463H	RDAT[15][2]	RDAT[14][2]	RDAT[13][2]	RDAT[12][2]	RDAT[11][2]	RDAT[10][2]	RDAT[9][2]	RDAT[8][2]
464H	RDAT[7][2]	RDAT[6][2]	RDAT[5][2]	RDAT[4][2]	RDAT[3][2]	RDAT[2][2]	RDAT[1][2]	RDAT[0][2]
465H			RSOC[2]	RPRTY[2]	RCA[3]		INTB[1]	
480H								INTB[1]
490H								INTB[1]
498H		INTB[1]						
4A2H							INTB[1]	
508H								
50AH								INTB[1]
50CH								
510H								INTB[1]
530H	INTB[1]							
534H								
536H								
532H								
533H								
54CH								

Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
54EH								
550H								INTB[1]
558H								INTB[1]
565H			RSOC[2]	RPRTY[2]			INTB[1]	
580H								INTB[1]
590H								INTB[1]
598H		INTB[1]						
5A2H							INTB[1]	
608H								
60AH								INTB[1]
60CH								
610H								INTB[1]
630H	INTB[1]							
634H								
636H								
632H								
633H								
64CH								
64EH								
650H								INTB[1]
658H								INTB[1]
665H			RSOC[2]	RPRTY[2]			INTB[1]	
680H								INTB[1]
690H								INTB[1]
698H		INTB[1]						
6A2H							INTB[1]	
708H					RPOHCLK	RPOH	REF8KO	
70AH	FRMSTAT							INTB[1]
70CH						TPOHFP	TPOHCLK	
710H								INTB[1]
730H	INTB[1]							
734H								TCLK
736H							TOHFP	TOHCLK

Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
732H			ROH					ROHCL]
733H				ROHFP				
74CH	TPOS							
74EH								TNEG
750H								INTB[1]
758H								INTB[1]
765H		LCD	RSOC[2]	RPRTY[2]		DRCA	INTB[1]	
780H						DTCA		INTB[1]
790H								INTB[1]
798H		INTB[1]						
7A2H							INTB[1]	

1. All these register bits must be set to logic 0 for the INTB output to be tri-stated. If any one of these register bits is a logic 1, then INTB will be driven to logic 0.

2. To enable these outputs, after setting the desired state, RADR[0] must be set to logic 0, RENB must be set to logic 1, bit 4 of register 09BH must be set to logic 1, and RFCLK must transition from logic 0 to logic 1.

3. To enable this output, after setting the desired state, RADR[2:0] must be set equal to PHY_ADR[2:0], RADR[1:0] must be set equal to binary 00, RFCLK must transition from logic 0 to logic 1.

4. To enable this output, after setting the desired state, TADR[2:0] must be set equal to PHY_ADR[2:0], TADR[1:0] must be set equal to binary 00, TFCLK must transition from logic 0 to logic 1.

5. Bit 1 of this register must be logic 0.

7.2 JTAG Test Port

The S/UNI-JET JTAG Test Access Port (TAP) allows access to the TAP controller and the 4 TAP registers: instruction, bypass, device identification and boundary scan. Using the TAP, device input logic levels can be read, device outputs can be forced, the device can be identified and the device scan path can be bypassed. For more details on the JTAG port, please refer to the Operations section.

Table 6 - Instruction Register

Length - 3 bits

Instructions	Selected Register	Instruction Codes, IR[2:0]
EXTEST	Boundary Scan	000
IDCODE	Identification	001
SAMPLE	Boundary Scan	010
BYPASS	Bypass	011
BYPASS	Bypass	100
STCTEST	Boundary Scan	101
BYPASS	Bypass	110
BYPASS	Bypass	111

Identification Register

Length - 32 bits

Version number - 2H

Part Number - 7346H

Manufacturer's identification code - 0CDH

Device identification - 273460CDH

Table 7 - Boundary Scan Register

Length - 198 bits

Pin/Enable	Register Bit	Cell Type	ID Bit	Pin/Enable	Register Bit	Cell Type	ID Bit
TDAT[15][1]	0	IN_CELL	0	TPOHFP	87	OUT_CELL	(0)
TDAT[14]	1	IN_CELL	0	Unconnected	88:90	OUT_CELL	(0)
TDAT[13]	2	IN_CELL	1	LCD	91	OUT_CELL	(0)
TDAT[12]	3	IN_CELL	0	Unconnected	92:94	OUT_CELL	(0)
TDAT[11]	4	IN_CELL	0	RPOH	95	OUT_CELL	(0)
TDAT[10]	5	IN_CELL	1	Unconnected	96:98	OUT_CELL	(0)
TDAT[9]	6	IN_CELL	1	RPOHCLK	99	OUT_CELL	(0)
TDAT[8]	7	IN_CELL	1	Unconnected	100:102	OUT_CELL	(0)
TDAT[7]	8	IN_CELL	0	REF8KO	103	OUT_CELL	(0)
TDAT[6]	9	IN_CELL	0	Unconnected	104:106	OUT_CELL	(0)
TDAT[5]	10	IN_CELL	1	FRMSTAT	107	OUT_CELL	(0)

Pin/Enable	Register Bit	Cell Type	ID Bit	Pin/Enable	Register Bit	Cell Type	ID Bit
TDAT[4]	11	IN_CELL	1	Unconnected	108:110	OUT_CELL	(0)
TDAT[3]	12	IN_CELL	0	REF8KI	111	IN_CELL	(0)
TDAT[2]	13	IN_CELL	1	ROHCLK	112	OUT_CELL	(0)
TDAT[1]	14	IN_CELL	0	Unconnected	113;115	OUT_CELL	(0)
TDAT[0]	15	IN_CELL	0	ROHFP	116	OUT_CELL	(0)
TFCLK	16	IN_CELL	0	Unconnected	117:119	OUT_CELL	(0)
Tied to '1'	17	IN_CELL	1	ROH	120	OUT_CELL	(0)
Tied to '1'	18	IN_CELL	1	Unconnected	121:123	OUT_CELL	(0)
TADR[2]	19	IN_CELL	0	TOHFP	124	OUT_CELL	(0)
TADR[1]	20	IN_CELL	0	Unconnected	125:127	OUT_CELL	(0)
TADR[0]	21	IN_CELL	0	TOHCLK	128	OUT_CELL	(0)
TPRTY	22	IN_CELL	0	Unconnected	129:131	OUT_CELL	(0)
TSOC	23	IN_CELL	0	TOHINS	132	IN_CELL	(0)
TENB	24	IN_CELL	1	Tied to '0'	133:135	IN_CELL	(0)
TCA	25	OUT_CELL	1	TOH	136	IN_CELL	(0)
TCA_OEB[2]	26	OUT_CELL	0	Tied to '0'	137:139	IN_CELL	(0)
DTCA	27	OUT_CELL	0	RCLK	140	IN_CELL	(0)
Unconnected	28	OUT_CELL	1	Tied to '0'	141:143	IN_CELL	(0)
Unconnected	29	OUT_CELL	1	RNEG	144	IN_CELL	(0)
Unconnected	30	OUT_CELL	0	Tied to '0'	145;147	IN_CELL	(0)
PHY_ADR[2]	31	IN_CELL	1	RPOS	148	IN_CELL	(0)
PHY_ADR[1]	32	IN_CELL	(1)	Tied to '0'	149:151	IN_CELL	(0)
PHY_ADR[0]	33	IN_CELL	(1)	TCLK	152	OUT_CELL	(0)
ATM8	34	IN_CELL	(0)	Unconnected	153:155	OUT_CELL	(0)
DRCA	35	OUT_CELL	(0)	TNEG	156	OUT_CELL	(0)
Unconnected	36	OUT_CELL	(0)	Unconnected	157:159	OUT_CELL	(0)
Unconnected	37	OUT_CELL	(0)	TPOS	160	OUT_CELL	(0)
Unconnected	38	OUT_CELL	(0)	Unconnected	161:163	OUT_CELL	(0)
RCA	39	OUT_CELL	(0)	INTB	164	OUT_CELL	(0)
RCA_OEB[3]	40	OUT_CELL	(0)	RSTB	165	IN_CELL	(0)
RSOC	41	OUT_CELL	(0)	WRB	166	IN_CELL	(0)
RENB	42	IN_CELL	(0)	RDB	167	IN_CELL	(0)
RFCLK	43	IN_CELL	(0)	ALE	168	IN_CELL	(0)
Tied to '1'	44	IN_CELL	(0)	CSB	169	IN_CELL	(0)
Tied to '1'	45	IN_CELL	(0)	A[10:0]	170:180	IN_CELL	(0)
RADR[2]	46	IN_CELL	(0)	D[7]	181	IO_CELL	(0)
RADR[1]	47	IN_CELL	(0)	DOENB [7][5]	182	OUT_CELL	(0)
RADR[0]	48	IN_CELL	(0)	D[6]	183	IO_CELL	(0)
RPRTY	49	OUT_CELL	(0)	DOENB[6][5]	184	OUT_CELL	(0)
RDAT[15:0]	50:65	OUT_CELL	(0)	D[5]	185	IO_CELL	(0)
RX_OEB[4]	66	OUT_CELL	(0)	DOENB [5][5]	186	OUT_CELL	(0)
TICLK	67	IN_CELL	(0)	D[4]	187	IO_CELL	(0)
Tied to '0'	68:70	IN_CELL	(0)	DOENB [4][5]	188	OUT_CELL	(0)
TIOHM	71	IN_CELL	(0)	D[3]	189	IO_CELL	(0)

Pin/Enable	Register Bit	Cell Type	ID Bit	Pin/Enable	Register Bit	Cell Type	ID Bit
Tied to '0'	72:73	IN_CELL	(0)	DOENB [3][5]	190	OUT_CELL	(0)
Tied to '1'	74	IN_CELL	(0)	D[2]	191	IO_CELL	(0)
TPOH	75	IN_CELL	(0)	DOENB [2][5]	192	OUT_CELL	(0)
Tied to '0'	76:78	IN_CELL	(0)	D[1]	193	IO_CELL	(0)
TPOHINS	79	IN_CELL	(0)	DOENB [1][5]	194	OUT_CELL	(0)
Tied to '0'	80:82	IN_CELL	(0)	D[0]	195	IO_CELL	(0)
TPOHCLK	83	OUT_CELL	(0)	DOENB [0][5]	196	OUT_CELL	(0)
Unconnected	84:86	OUT_CELL	(0)	HIZ[6]	197	OUT_CELL	(0)

NOTES:

1. TDAT[15] is the first bit of the boundary scan chain.

2. TCA_OEB will set TCA to tri-state when set to logic 1. When set to logic 0, TCA will be driven.

3. RCA_OEB will set RCA to tri-state when set to logic 1. When set to logic 0, RCA will be driven.

4. RX_OEB will set RDAT[15:0], RPRTY, and RSOC to tri-state when set to logic 1. When set to logic 0, RDAT[15:0], RPRTY, and RSOC will be driven.

5. The DOENB signals will set the corresponding bidirectional signal (the one preceding the DOENB in the boundary scan chain — see note 1 also) to an output when set to logic 0. When set to logic 1, the bidirectional signal will be tri-stated.

6. HIZ will set all outputs not controlled by TCA_OEB, RCA_OEB, RX_OEB, and DOENB to tri-state when set to logic 1. When set to logic 0, those outputs will be driven.

8 OPERATION

8.1 Software Initialization Sequence

The S/UNI JET can come out of reset in a mode that consumes excess power. The device functionality is not altered except for excessive power consumption resulting excess heat dissipation which could lead to long term reliability problems.

The software initialization sequence in this section will put the S/UNI JET into a normal power consumption state should the device come out of reset in the excess power state. This reset sequence must be used to guarantee long term reliability of the device.

1. Reset the S/UNI JET.

2. Set IOTST (bit 2) in the Master Test Register to '1' (by writing 00000100 to register 400H).

3. Put the JET Receive Cell Processor (RXCP) into test mode by writing:

   00000101 to test register 461H

   00000101 to test register 561H

   00000101 to test register 661H

   00000101 to test register 761H

4. Set JET Receive Cell Processor block built in set test (BIST) controls signals by writing:

   01000000 to test register 462H

   01000000 to test register 562H

   01000000 to test register 662H

   01000000 to test register 762H

   10101010 to test register 463H

   10101010 to test register 563H

   10101010 to test register 663H

   10101010 to test register 763H

5. Put the JET Transmit Cell Processor (TXCP) into test mode by writing:

00000011 to test register 481H

00000011 to test register 581H

00000011 to test register 681H

00000011 to test register 781H

6. Set JET Transmit Cell Processor block built in set test (BIST) controls signals by writing:

10000000 to test register 480H

10000000 to test register 580H

10000000 to test register 680H

10000000 to test register 780H

10101010 to test register 482H

10101010 to test register 582H

10101010 to test register 682H

10101010 to test register 782H

7. Toggle REF8KI (pin T3) signal at least eight times (this provides the clock to the RAM). REF8KI is the test clock used by the TXCP and RXCP blocks when in test mode.

8. Set IOTST (bit 2) in the Master Test register to '0' (by writing 00000000 to register 400H).

9. Resume normal device programming.

9 ABSOLUTE MAXIMUM RATINGS

Table 8 - Absolute Maximum Ratings

Ambient Temperature under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Supply VDD with respect to GND	-0.3V to 4.6V
Voltage on BIAS with respect to GND	VDD - 0.3V to 5.5V
Voltage on Any Pin	-0.3 V to BIAS +0.3 V
Static Discharge Voltage	±1000 V
Latch-Up Current	±100 mA
DC Input Current	±20 mA
Lead Temperature	+230°C
Absolute Maximum Junction Temperature	+150°C

10 D.C. CHARACTERISTICS

T_C = -40°C to +85°C, V_{DD} = 3.3V ±10%, V_{DD} < BIAS < 5.5V

(Typical Conditions: T_C = 25°C, V_{DD} = 3.3V, V_{BIAS} = 5V)

Table 9 - DC Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{DD}	Power Supply	2.97	3.3	3.63	Volts	
BIAS	5V Tolerant Bias	VDD	5.0	5.5	Volts	
I_{BIAS}	Current into 5V Bias		6.0		µA	V_{BIAS} = 5.5V
V_{IL}	Input Low Voltage	0		0.8	Volts	Guaranteed Input Low voltage.
V_{IH}	Input High Voltage	2.0		BIAS	Volts	Guaranteed Input High voltage.
V_{OL}	Output or Bi-directional Low Voltage		0.23	0.4	Volts	Guaranteed output Low voltage at VDD=2.97V and I_{OL}=maximum rated for pad. [4, 5, 6]
V_{OH}	Output or Bi-directional High Voltage	2.4	2.93		Volts	Guaranteed output High voltage at VDD=2.97V and I_{OH}=maximum rated current for pad. [4, 5, 6]
V_{T-}	Reset Input Low Voltage			0.8	Volts	Applies to RSTB, TRSTB, TICLK[4:1], RCLK[4:1], TFCLK, RFCLK, TCK, TDI, TMS, and REF8KI.
V_{T+}	Reset Input High Voltage	2.0			Volts	Applies to RSTB, TRSTB, TICLK[4:1], RCLK[4:1], TFCLK, RFCLK, TCK, TDI, TMS, and REF8KI.
V_{TH}	Reset Input Hysteresis Voltage		0.5		Volts	Applies to RSTB, TRSTB, TICLK[4:1], RCLK[4:1], TFCLK, RFCLK, TCK, TDI, TMS, and REF8KI.
I_{ILPU}	Input Low Current	-100	-60	-10	µA	V_{IL} = GND. [1, 3]
I_{IHPU}	Input High Current	-10	0	+10	µA	V_{IH} = V_{DD}. [1. 3]
I_{IL}	Input Low Current	-10	0	+10	µA	V_{IL} = GND. [2, 3]
I_{IH}	Input High Current	-10	0	+10	µA	V_{IH} = V_{DD}. [2, 3]
C_{IN}	Input Capacitance		6		pF	t_A=25°C, f = 1 MHz
C_{OUT}	Output Capacitance		6		pF	t_A=25°C, f = 1 MHz

Symbol	Parameter	Min	Typ	Max	Units	Conditions
C_{IO}	Bi-directional Capacitance		6		pF	t_A=25°C, f = 1 MHz
I_{DDOP1}	Operating Current		TBD	TBD	mA	V_{DD} = 3.63V, Outputs Unloaded (DS3/PLCP mode)
I_{DDOP2}	Operating Current		TBD	TBD	mA	V_{DD} = 3.63V, Outputs Unloaded (T1/E1 PLCP mode)
I_{DDOP3}	Operating Current		TBD	TBD	mA	V_{DD} = 3.63V, Outputs Unloaded (DS3 ATM mode)
I_{DDOP4}	Operating Current		TBD	TBD	mA	V_{DD} = 3.63V, Outputs Unloaded (E3 ATM mode)
I_{DDOP5}	Operating Current		TBD	TBD	mA	V_{DD} = 3.63V, Outputs Unloaded (J2 ATM mode)
I_{DDOP6}	Operating Current		TBD	TBD	mA	V_{DD} = 3.63V, Outputs Unloaded (52 Mbit/s arbitrary framing format with ATM direct mapping)
I_{DDOP7}	Operating Current		TBD	TBD	mA	V_{DD} = 3.63V, Outputs Unloaded (DS3 framer only)
I_{DDOP8}	Operating Current		TBD	TBD	mA	V_{DD} = 3.63V, Outputs Unloaded (E3 framer only)
I_{DDOP9}	Operating Current		TBD	TBD	mA	V_{DD} = 3.63V, Outputs Unloaded (J2 framer only)

Notes on D.C. Characteristics:

1. Input pin or bi-directional pin with internal pull-up resistor.
2. Input pin or bi-directional pin without internal pull-up resistor
3. Negative currents flow into the device (sinking), positive currents flow out of the device (sourcing).
4. The Utopia interface outputs, RDAT[15:0], RPRTY, RCA, DRCA, RSOC, TCA, and DTCA, have 12 mA drive capability.
5. The outputs TCLK, TPOS/TDATO, TNEG/TOHM, TPOHFP/TFPO/TMFPO/TGAPCLK, LCD/RDATO, RPOH/ROVRHD, RPOHCLK/RSCLK/RGAPCLK, and REF8KO/RPOHFP/RFPO/RMFPO have 6 mA drive capability.
6. The data bus outputs, D[7:0], and all outputs not specified above have 3 mA drive capability.

11 ORDERING AND THERMAL INFORMATION

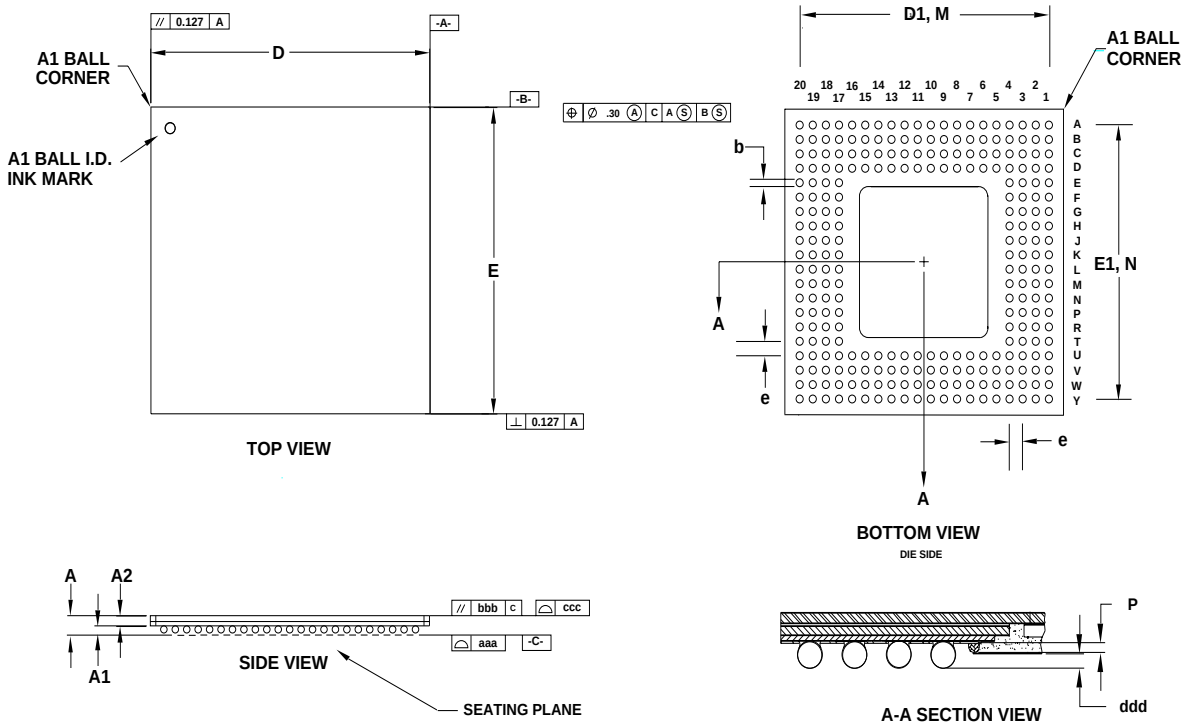
Table 10 - Packaging Information

PART NO	DESCRIPTION
PM7347-BI	256-pin Ball Grid Array (SBGA)

Table 11 - Thermal Information

PART NO.	CASE TEMPERATURE	Theta Ja	Theta Jc
PM7347-BI	-40°C to 85°C	19 °C/W	5 °C/W

12 MECHANICAL INFORMATION



Notes: 1) ALL DIMENSIONS IN MILLIMETER.

2) DIMENSION aaa DENOTES COPLANARITY

3) DIMENSION bbb DENOTES PARALLEL

4) DIMENSION ccc DENOTES FLATNESS

PACKAGE TYPE: 256 PIN THERMAL BALL GRID ARRAY															
BODY SIZE: 27 x 27 x 1.45 MM															
Dim.	A	A1	A2	D	D1	E	E1	M,N	e	b	aaa	bbb	ccc	ddd	P
Min.	1.32	0.56	0.76	26.90	24.03	26.90	24.03			0.60				0.15	0.20
Nom.	1.45	0.63	0.82	27.00	24.13	27.00	24.13	20x20	1.27	0.75				0.33	0.30
Max.	1.58	0.70	0.88	27.10	24.23	27.10	24.23			0.90	0.15	0.15	0.20	0.50	0.35

NOTES

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