SIEMENS

Quadrature Phase Modulator

PMB 2205

Preliminary Data

Bipolar IC

Features

- Double-balanced mixers
- Direct modulation
- Linear modulating inputs
- Symmetrical circuitry
- Generation of orthogonal carriers within a wide frequency range
- LO operation alternatively at transmit frequency (f_0) or double transmit frequency ($2f_0$)
- Output of frequency doubler may be filtered by external tank circuit
- 35 dB carrier rejection, 40 dB SSB rejection
- 42 dB rejection of third order products at normal drive level
- 38 dB rejection of doubled RF output frequency
- 0 dBm linear output power
- Power ON/OFF switch, low standby current
- LO frequency range 120 MHz to 800 MHz at LO, $\overline{LO}$ input
- Double transmit frequency range 80 MHz to 900 MHz at PP/$\overline{PP}$ input
- Modulation frequency range 0 to 400 MHz
- P-DSO-20-1; P-DSO-20-4 package
- Temperature range – 25 °C to 85 °C

P-DSO-20-1

P-DSO-20-4

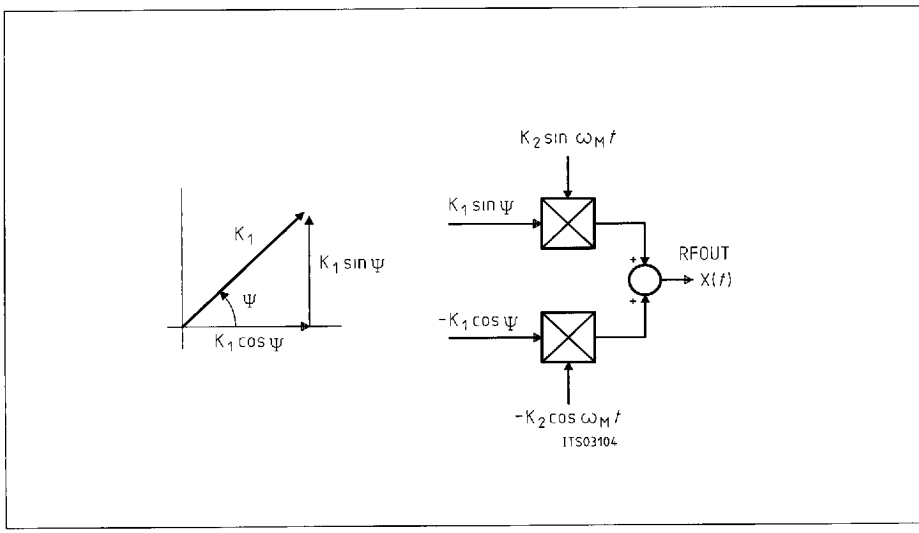
Type	Version	Ordering Code	Package
PMB 2205T	V1.1	Q67000-A6048	P-DSO-20-1 (SMD)
PMB 2205S	V1.1	Q67000-A6066	P-DSO-20-4 (SMD Shrink)
PMB 2205T	V1.2	Q67000-A6083	P-DSO-20-1 (SMD)
PMB 2205S	V1.2	Q67000-A6084	P-DSO-20-4 (SMD Shrink)

For new designs V1.2 has to be used.

Applications

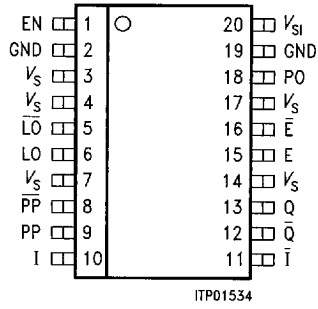
- Digital mobile radio and WLAN
- PCN & GSM-systems
- Continuous phase modulation, e.g. GMSK
- Various kinds of QPSK modulation and linear QAM
- Frequency fine tuning
- Image reject up and down mixer

The phase $\Psi(t) - \omega_M t$ of RF-carriers in the range 120 to 800 MHz is modulated by external signals $I(t) = K_2 \sin \omega_M t$ and $Q(t) = -K_2 \cos \omega_M t$. The circuit is to be incorporated into a transmitter for mobile telephones conforming to the PCN/GSM standards.



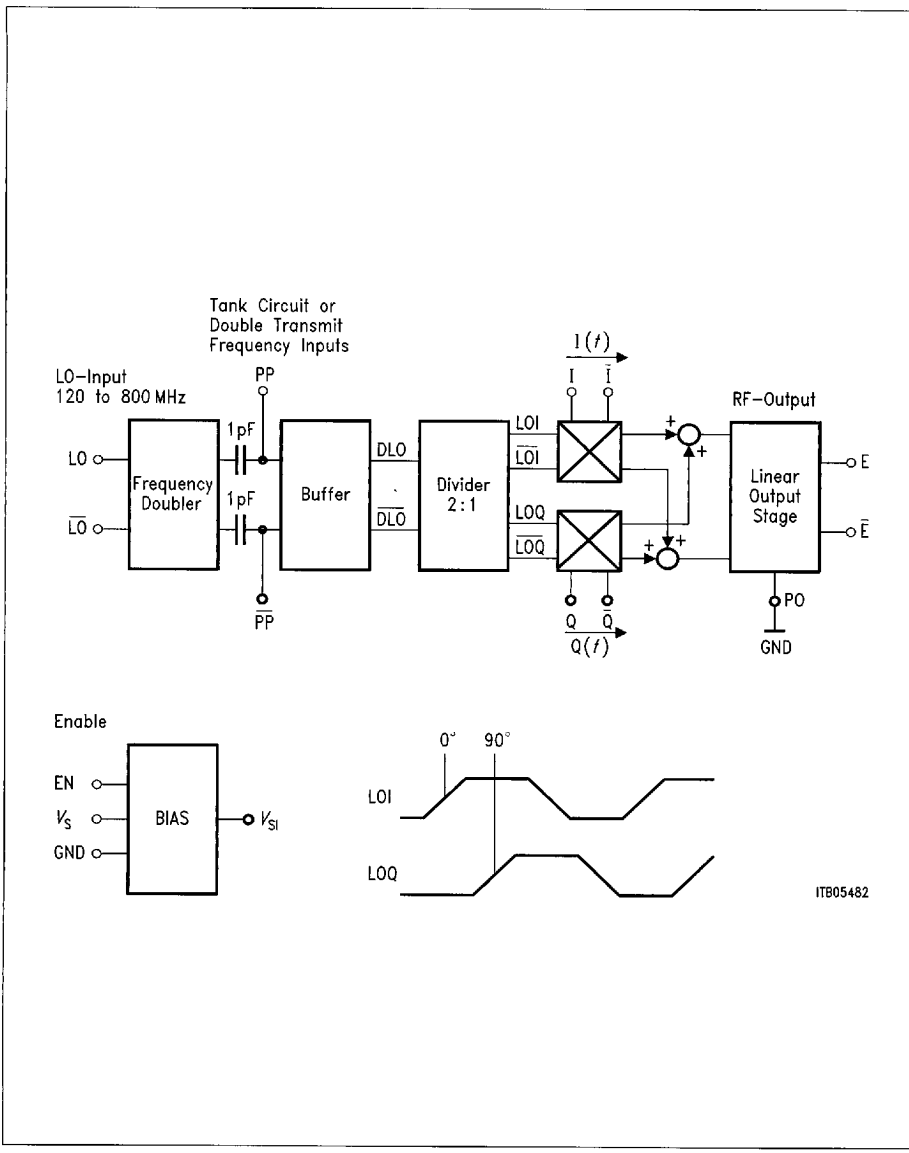
$X(t) = K_1 \sin \Psi(t) \times K_2 \sin \omega_M t + K_1 \cos \Psi(t) \times K_2 \cos \omega_M t$
$= K_1 K_2 \cos (\Psi(t) - \omega_M t) \rightarrow$ lower sideband
Realization to eq.(8) in GSM rec. 05. 04. Feb. 88
The actual internal generated orthogonal LO carriers work in switching mode.

Pin Configuration
(top view)



Pin Definitions and Functions

Pin No.	Symbol	Function
1	EN	Enable, power ON/OFF switch
2	GND	Ground
3	V_S	Supply voltage
4	V_S	Supply voltage, connected to pin 3
5	$\overline{LO}$	Local oscillator frequency input, inverted
6	LO	Local oscillator frequency input
7	V_S	Supply voltage, connected to pin 3
8	$\overline{PP}$	Tank circuit or double transmit frequency input, inverted
9	PP	Tank circuit or double transmit frequency input
10	I	Modulating input I, open base
11	$\overline{I}$	Inverted modulating input $\overline{I}$, open base
12	$\overline{Q}$	Inverted modulating input $\overline{Q}$, open base
13	Q	Modulating input Q, open base
14	V_S	Supply voltage, connected to pin 3
15	E	RF output, open collector
16	$\overline{E}$	Inverted RF output, open collector
17	V_S	Supply voltage, connected to pin 3
18	PO	Output emitter source resistor of output stage, to be connected to GND direct or via a resistor to program emitter current
19	GND	Ground, connected to pin 2
20	V_{SI}	Test output of internal bias voltage



Block Diagram

Circuit Description

The transmission frequency f_0 at the differential inputs LO, $\overline{LO}$ is first doubled and then bandpass filtered at $2f_0$.

The filter may be realized by an external tank circuit at PP, $\overline{PP}$ providing a high suppression at higher harmonics than $2f_0$. Alternatively, a local oscillator operating at 2 f_0 may be connected to PP, $\overline{PP}$ while LO, $\overline{LO}$ is RF grounded.

This frequency is the clock for a 2:1 divider. At the outputs of the two latches of this divider orthogonal carriers LOI and LOQ for the modulator are provided. The modulator consists of two Gilbert Multipliers which are operated in switching mode by LOI and LOQ respectively. Furthermore these multipliers are driven with high linearity by the modulating signals $I(t)$ and Q (t) up to 1.5 Vpp.

The output signals of both Gilbert cells are combined at the addition points. The sum drives a linear output stage.

An internal current source resistor of the output stage is fed to PO. This pad should be connected to GND when minimal nonlinear distortion and maximum output power is desired.

Alternatively a resistor can be inserted, e.g. 30 Ω, in order to reduce the output current by half.

The pin V_{SI} is used for DC-testing. A power-down switch EN reduces the current consumption from approximately 40 mA in the active mode to less than 10 µA in the standby mode.

Electrical Characteristics

Absolute Maximum Ratings

$T_A = -25$ to 85 °C

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Supply voltage	V_S	– 0.5	7	V
Differential input voltage (any differential input)	V_{Diff}	– 3	3	V
Output voltage at E and $\overline{E}$	V_{OUT}	$V_S - 1.6$	7	V
Junction temperature	T_j		125	°C
Storage temperature	T_{stg}	– 55	125	°C
Thermal resistance P-DSO-20-1	R_{thJA}		90	K/W
Thermal resistance P-DSO-20-4	R_{thJA}		143	K/W

Operational Range

Within the operational range the IC operates as described in the circuit description. The AC/DC characteristic limits are not guaranteed

Supply voltage	V_S	4.4	5.8	V
Ambient temperature	T_A	– 25	85	°C
Transmit frequency range at LO/$\overline{LO}$	$f_{LO/\overline{LO}}$	120	800	MHz
Transmit frequency input level referred to 50 Ω	$P_{LO/\overline{LO}}$	– 12	0	dBm
Double transmit frequency range at PP/$\overline{PP}$	$f_{PP/\overline{PP}}$	80	900	MHz
Double transmit frequency input level	$P_{PP/\overline{PP}}$	**see input sensitivity diagram figure 3**		

The pins E, $\overline{E}$, PP and $\overline{PP}$ have no additional internal ESD protection circuitry

AC/DC Characteristics

V_S = 5.0 V; T_A = 25 °C; P_{LO} = – 15 dBm (referred to test circuit)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Supply Current						
Normal operation	$I_E + I_{\overline{E}}$	11.5	14.5	18	mA	EN = H
Normal operation	I_S	23	27.5	33	mA	EN = H
Powered down	I_S		0.15	10	µA	EN = L
Transmit Frequency Input LO/$\overline{LO}$						
Internal DC voltage at the input bases	V_{DCLO} $V_{DC\overline{LO}}$	3.3	3.6	3.8	V	V_S = 5 V
Differential AC input impedance at 400 MHz *	$R_{LO/\overline{LO}}$		1.8		kΩ	
Input capacitance parallel to $R_{LO/\overline{LO}}$ at 400 MHz *	$C_{LO/\overline{LO}}$		0.8		pF	
Double Transmit Frequency Input PP/$\overline{PP}$						
Internal DC voltage at the input bases	V_{DCPP} $V_{DC\overline{PP}}$		3.6		V	V_S = 5 V
Differential AC input impedance at 800 MHz *	$R_{PP/\overline{PP}}$		190		Ω	
Input capacitance parallel to $R_{PP/\overline{PP}}$ at 800 MHz	$C_{PP/\overline{PP}}$		1.8		pF	

* Design hint

AC/DC Characteristics (cont'd)
V_S = 5.0 V; T_A = 25 °C; P_{LO} = – 15 dBm (referred to test circuit)

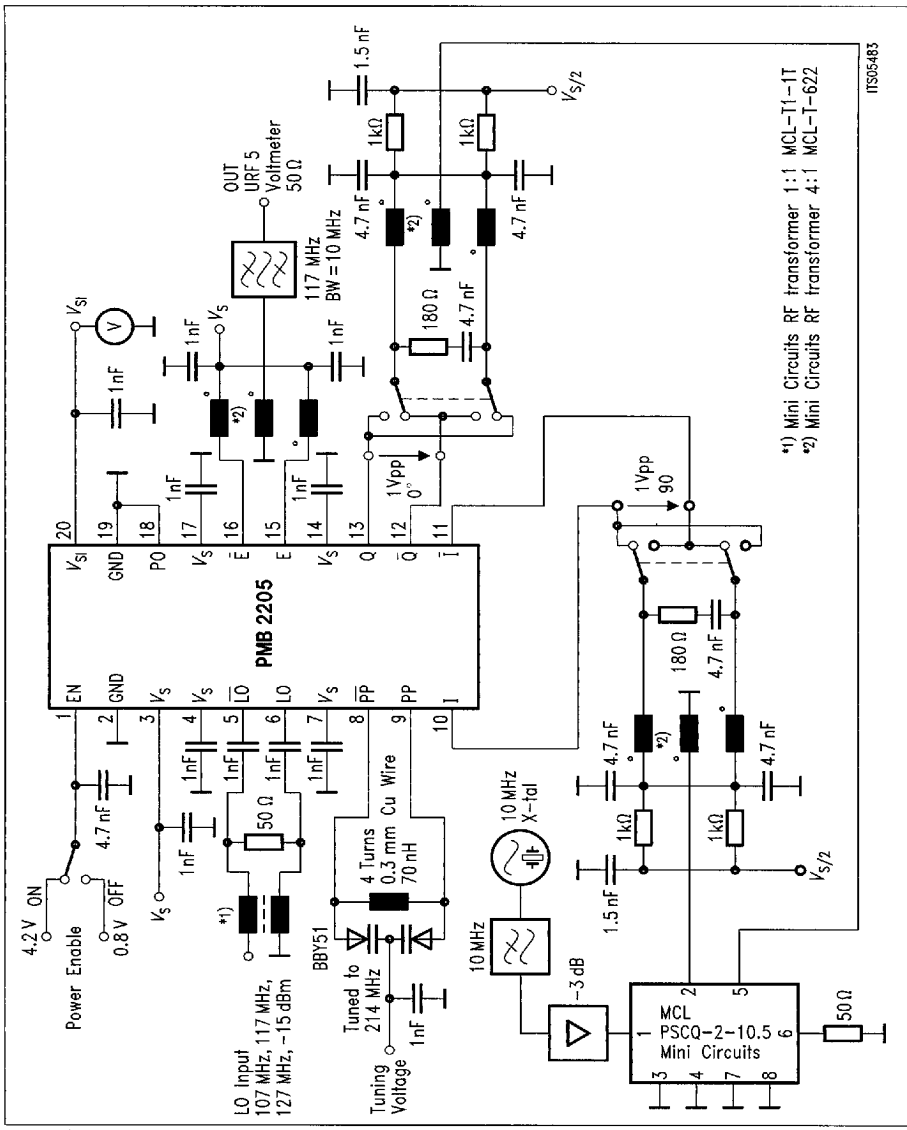
Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Modulation Inputs I to $\overline{I}$ and Q to $\overline{Q}$						
Input bias current of the open bases at I, $\overline{I}$, Q, $\overline{Q}$ **	I_B	4	6	8	µA	
External DC reference at I, $\overline{I}$ and Q, $\overline{Q}$	V_{REF}	2.1 2.1		2.6 3.2	V V	V_S = 4.5 V V_S = 5.5 V
Differential input swing for linear output power *	$V_{I,Q}$		1.0		Vpp	
Differential input swing for 3 dB compression	$V_{I,Q}$		1.9		Vpp	
External differential input offset voltage at I, $\overline{I}$ and Q, $\overline{Q}$ *	V_{offset}			10	mV	For 35 dB carrier suppression, **see figure 1**
External amplitude imbalance of I, Q modulation signals *	V_I/V_Q			0.15	dB	For single sideband suppression 40dB, **see figure 2**
Phase error of I, Q modulation signals *	$\Delta\varphi_{I,Q}$			1	deg	For single sideband suppression 40dB
Differential input impedance at the ports I, $\overline{I}$; Q, $\overline{Q}$: 1 pF parallel R_I	R_I		140		kΩ	f = 100 kHz
I, Q baseband input frequency range: 0 Hz up to the 3 dB point *	f			400	MHz	

* Design hint
** To avoid offset voltages, the base input should have identical bias

AC/DC Characteristics (cont'd)
V_S = 5.0 V; T_A = 25 °C; P_{LO} = – 15 dBm (referred to test circuit)

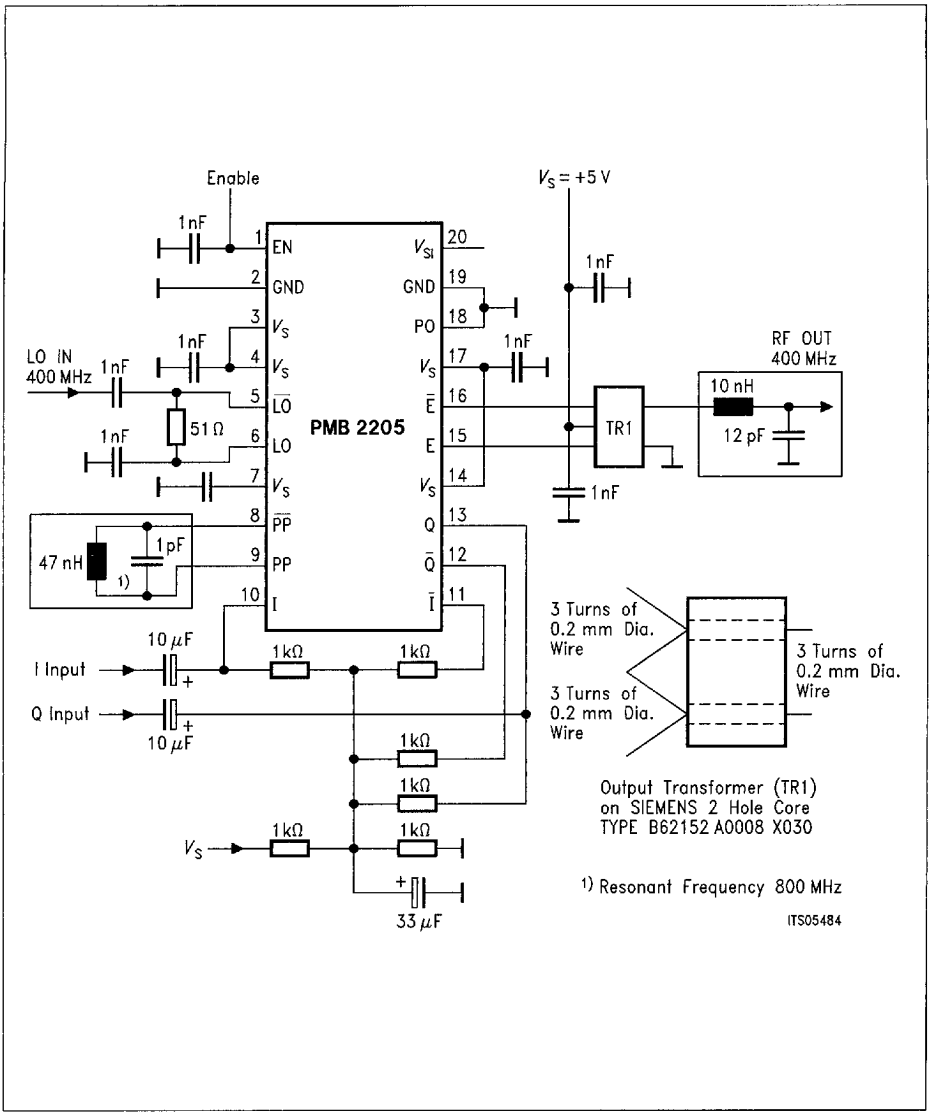
Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Output E/$\overline{E}$ (open collectors)						
Output power at 3 dB Compression *	P_{out}		6		dBm	$V_{I,Q}$ = 1.9 Vpp
Linear output power at 200 Ω load, low spurious	P_{out}	– 2	1	4	dBm	$V_{I,Q}$ = 1 Vpp **see test circuit**
Rejection of third order products			42		dB	$V_{I,Q}$ = 1 Vpp
Carrier suppression **see figure 1**	a_C	32	35		dB	$V_{I,Q}$ = 1 Vpp no external offset voltage
Single sideband suppression **	a_{SSB}	40	42		dB	**see test circuit**
Residual AM			2		%	**see figure 2**
Power ON/OFF Switching						
Input voltage at EN Active Powered down	 V_{EN} V_{EN}	 4.2 0		 V_S 0.8	 V V	 EN = H EN = L
Input current at EN	I_{EN}		30	80 0.1	µA µA	EN = H EN = L
Power up/down time	t_S		1.0		µs	EN = H ↔ L

* Design hint for matched output
** 90° phase shift between I and Q



Test Circuit

RF Test Circuit for SSB Sine Modulation Test and for Applications as Image Reject up Mixer



Typical Application Circuit

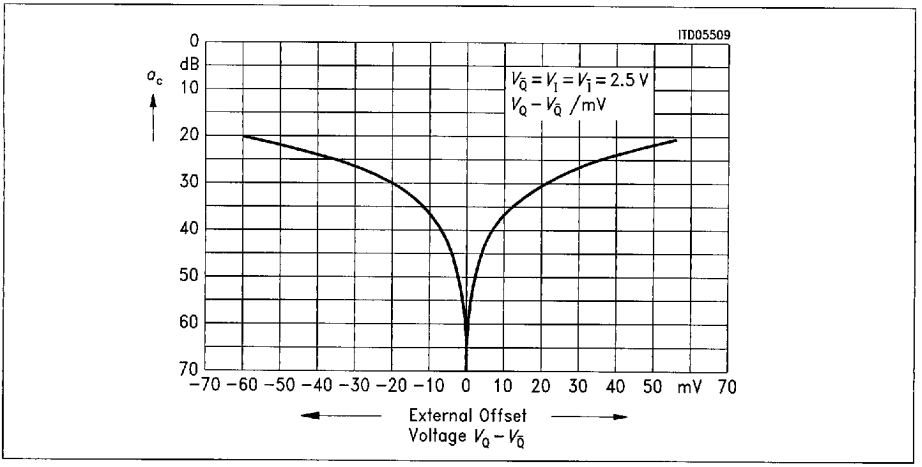


Figure 1
Carrier Suppression a_c versus Offset at Q, $\overline{Q}$

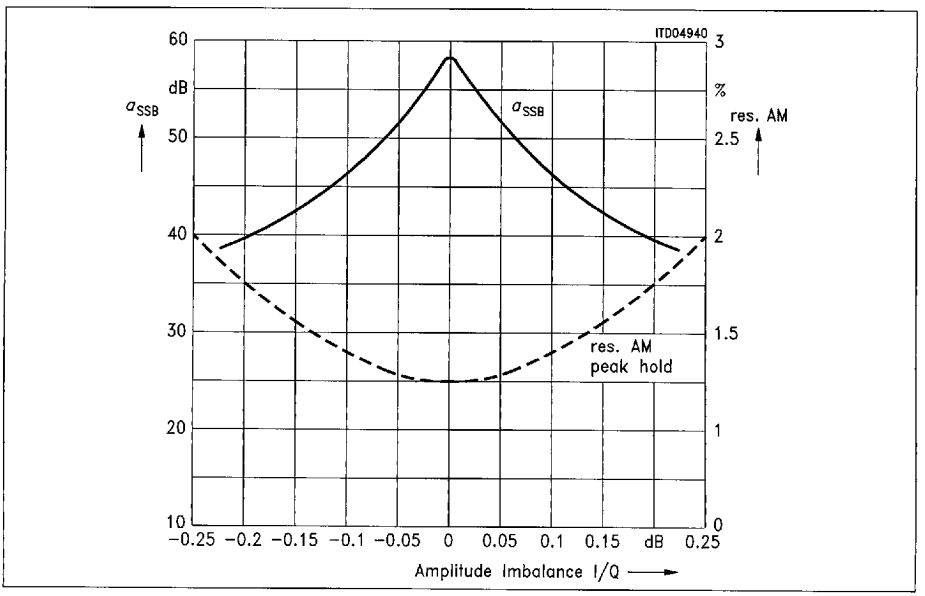


Figure 2
Single Sideband a_{SSB} and Residual AM versus I/Q Amplitude Imbalance

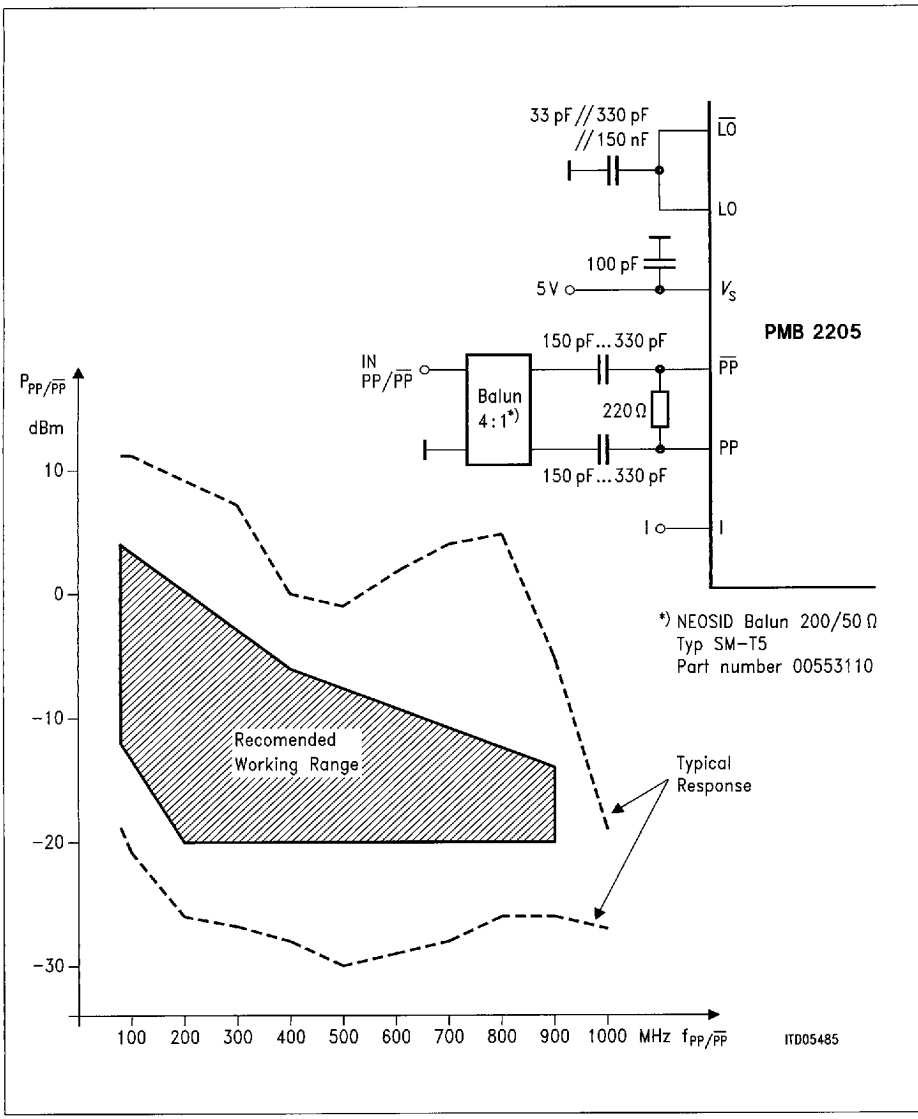


Figure 3
Input Level at PP, $\overline{PP}$ versus Double Transmit Frequency $f_{PP/\overline{PP}}$

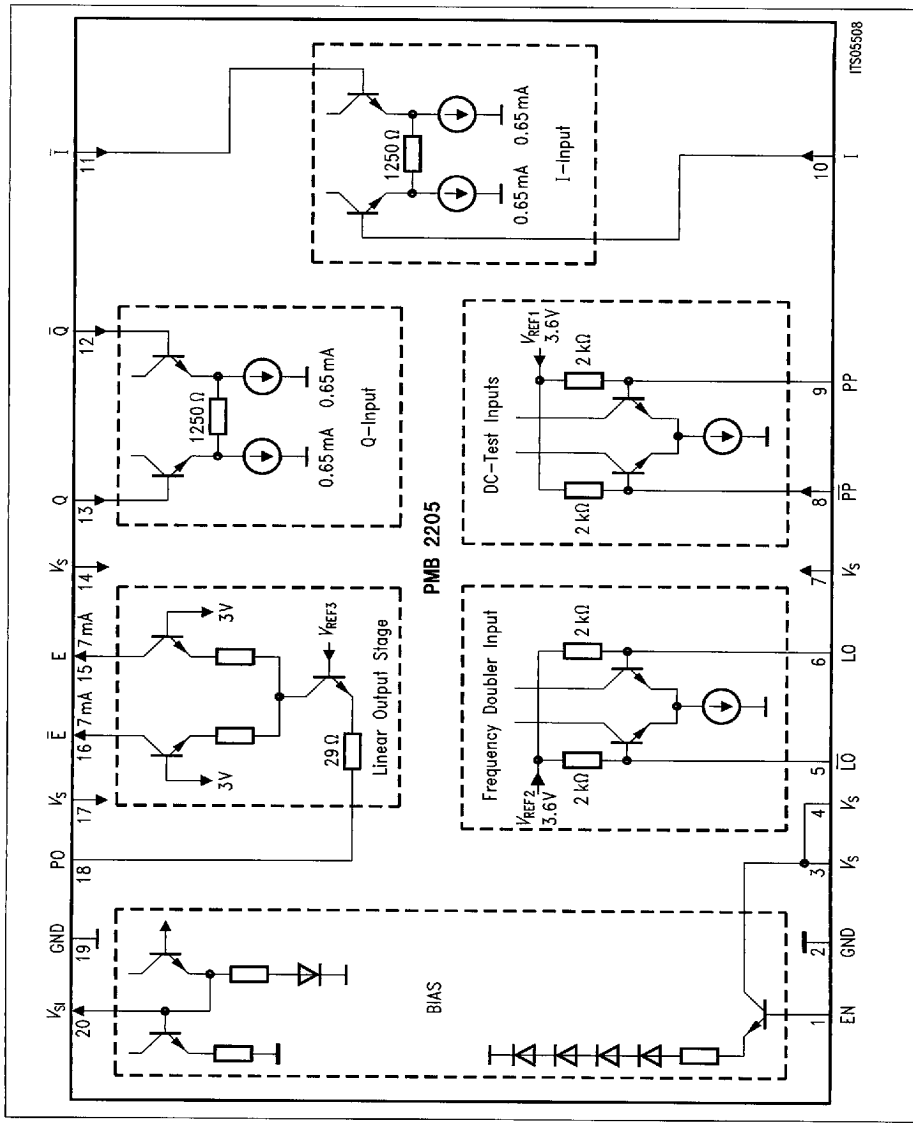
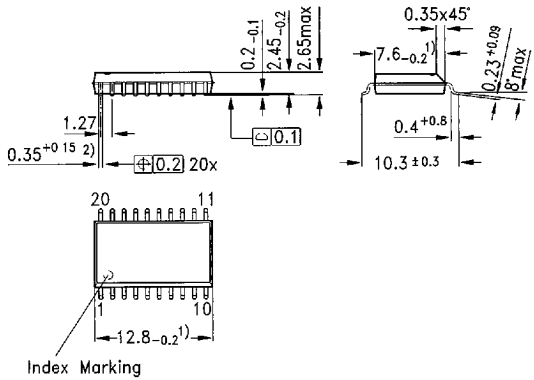


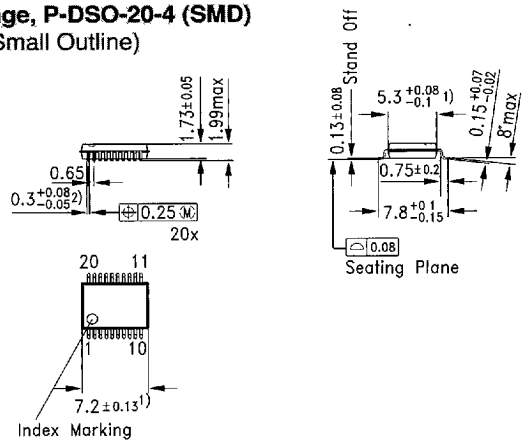
Figure 4
PMB 2205 – Input/Output Circuitry

Plastic Package, P-DSO-20-1 (SMD)
(Plastic Dual Small Outline)



1) Does not include plastic or metal protrusions of 0.15 max per side
2) Does not include dambar protrusion of 0.05 max per side

Plastic Package, P-DSO-20-4 (SMD)
(Plastic Dual Small Outline)



1) Does not include plastic or metal protrusions of 0.15 max per side
2) Does not include dambar protrusion of 0.08 max per side

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book "Package Information"
SMD = Surface Mounted Device

Dimensions in mm

B115-H6629-G1-X-7600

8235605 0059195 844