

Quadrature Modulator Circuit

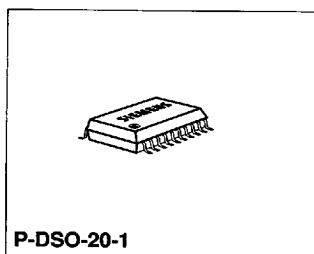
PMB 2210

Preliminary Data

Bipolar IC

Features

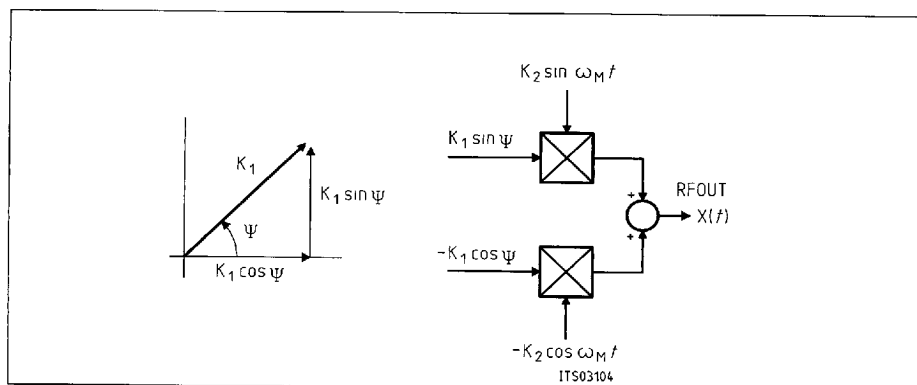
- Double-balanced mixer for 1 GHz with two Gilbert cells
- Linear modulating inputs
- Symmetrical circuitry
- Production of orthogonal carriers by two external resonant circuits
- Linear power output stage
- Power programmable
- Power ON/OFF switch
- Low power consumption 5 V x 26 mA



Applications

- 4 PSK-, MSK-, GMSK modulator
- Digital mobile radio
- GSM systems

Type	Ordering Code	Package
PMB 2210T	Q67000-A6028	P-DSO-20-1 (SMD)



$$X(t) = K_1 \cos \Psi(t) \times K_2 \cos \omega_M t - K_1 \sin \Psi(t) \times K_2 \sin \omega_M t = K_1 K_2 \cos (\omega_M t + \Psi)$$

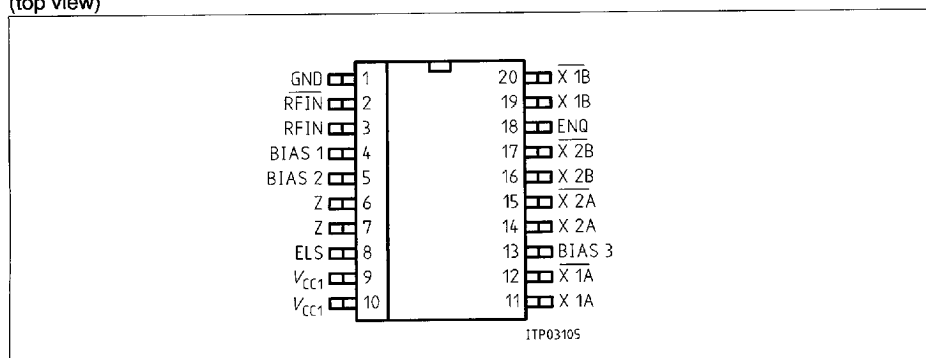
Application for continuous phase shift modulation

Realization to eq.(8) in GSM rec. 05. 04. Feb. 88

8235605 0059198 553

Semiconductor Group

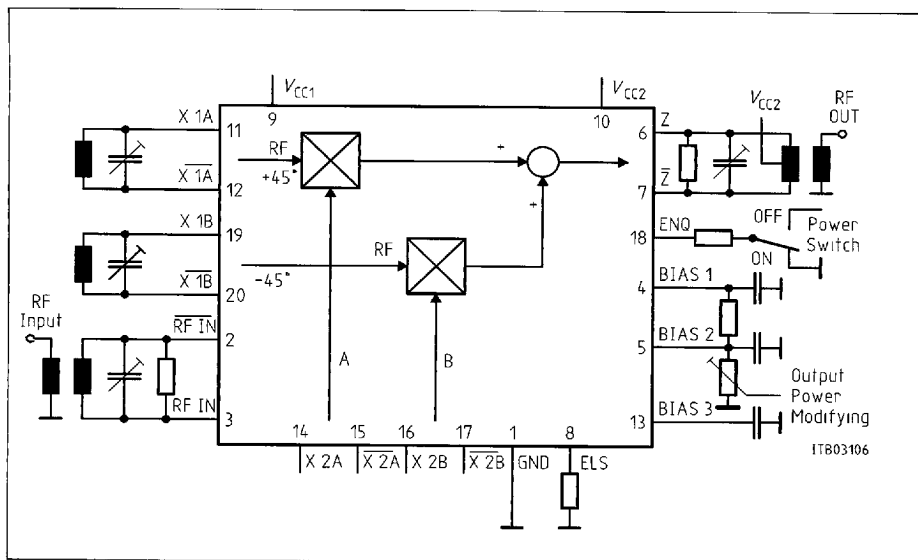
Pin Configuration (top view)



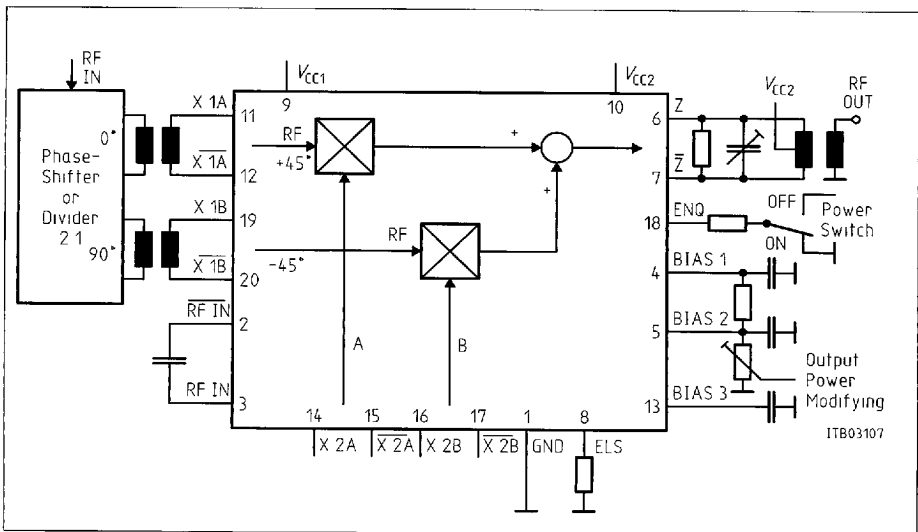
Pin Definitions and Functions

Pin No.	Symbol	Function
1	GND	Ground
2	$\overline{\text{RFIN}}$	Radio frequency input, inverted
3	RFIN	Radio frequency input
4	BIAS1	Output of internal bias voltage
5	BIAS2	Input bias voltage for output stage
6	Z	RF output, open collector
7	$\overline{\text{Z}}$	Inverted RF output, open collector
8	ELS	Emitter of level shifter, connect to GND
9	V_{CC1}	+ 5 V DC, determines BIAS1
10	V_{CC2}	+ 5 ... 7 V
11	X1A	Resonant circuit A
12	$\overline{\text{X1A}}$	Resonant circuit A, inverted
13	BIAS3	Connection for blocking capacitor
14	X2A	Modulating input A, open base
15	$\overline{\text{X2A}}$	Inverted modulating input A, open base
16	X2B	Modulating input B, open base
17	$\overline{\text{X2B}}$	Inverted modulating input B, open base
18	ENQ	Standby input; power ON: ENQ = GND
19	X1B	Resonant circuit B
20	$\overline{\text{X1B}}$	Resonant circuit B, inverted

8235605 0059199 49T



Block Diagram 1



Block Diagram 2

8235605 0059200 T31

Semiconductor Group

Functional Description

The modulator consists of two Gilbert multipliers the sum of whose drives a push-pull output power stage. With this 4-phase modulator it is possible to realize special RF-transmitters, which after filtering shift the phase but not the amplitude. Such continuous phase modulation, which shifts 90° per data time slot T , is called MSK (minimum shift keying) and GMSK, when there are Gauss-filters in the premodulation paths.

The modulation signal, is split into two orthogonal components A and B and fed through pins 14, 15, 16 and 17 to the differential inputs of the Gilbert cells. These have emitter series resistors to improve linearity.

The RF- or IF-carrier at pins 2, 3 is fed via two different paths through differential amplifiers to the Gilbert cells and on to the external resonant circuits at pins 11, 12, 19 and 20. Here two orthogonal carriers are produced, with enough power to switch the Gilbert cells. Both resonant circuits must be trimmed so that the resonant frequencies have offsets of $+1/2 B$ and $-1/2 B$ away from the middle of the used frequency band.

The bilateral 3 DB bandwidth of a resonant circuit is $B = f_0/Q$. The quality factor $Q = R/(L\omega_0)$ is limited by internal damping resistors $R = 500 \Omega$. The smaller the value of Q is, the wider will be the frequency interval in which a phase difference of approximately 90° is possible.

Functional Description (cont'd)

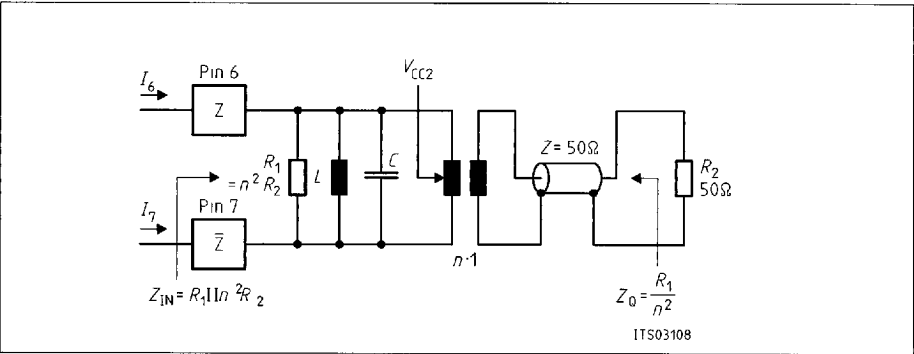
Options at 1 GHz

Block Diagram 1 The resonant circuits which produce this 90°-phase difference can not accurately be realized by $\lambda/4$ stub lines at high frequencies they must be combined with elements of quasi-transmission lines which can be trimmed.

Block Diagram 2 A phase shifter with outputs for 0° and 90° replaces the two trimmed resonant circuits. Now, for such a component which is usual in microwave applications, pins 11 and 12 and pins 19 and 20 are differential inputs. Pins 2 and 3 may remain open.

RF Output

Idealized model of output circuitry with transformer, resonant circuit and terminations R_1, R_2 :



If the currents $I_6 = I_7$ are sinusoidal with amplitude I , and assuming $R_1 = n^2 R_2$, the power $P(R_2) = (I/\sqrt{2})^2 n^2 R_2/4$ is transmitted to R_2 at the resonant frequency of L, C .

For $R_2 = 50 \Omega$ and $I = 5 \text{ mA}$, the conditions below follow

n	$P(R_2)$ [mW]	$10 \lg \frac{P(R_2)}{1 \text{ mW}}$	$Z_{IN} = R_1 n^2 R_2$	$\frac{\hat{V}}{2}$ at Z_{IN}	Voltage reserve till saturation of output stage
1	0.16	- 8 dBm	25 Ω	63 mV	1.54 V
2	0.63	- 2 dBm	100 Ω	250 mV	1.35 V
3	1.41	1.5 dBm	225 Ω	563 mV	1.04 V
4	2.50	4 dBm	400 Ω	1000 mV	0.6 V

Power into $R_2 = 50 \Omega$ and voltage swing of pins 6, 7 for sinusoidal signal $I = 5 \text{ mA}$.

Truth Table for Logic Tests

RFIN	$\overline{\text{RFIN}}$	X1A	$\overline{\text{X1A}}$	X1B	$\overline{\text{X1B}}$
L	H	L	H	L	H
H	L	H	L	H	L

Input transfer conditions,
without resonant circuit A and B

X1	X2	X1	X2	$I(R_{30})$	$I(R_{31})$	Z	$\overline{Z}$
L	L	L	L	$2I_o$	0	H	L
L	L	L	H	I_o	I_o	N	N
L	L	H	L	I_o	I_o	N	N
L	L	H	H	$2I_o$	0	H	L
L	H	L	L	I_o	I_o	N	N
L	H	L	H	0	$2I_o$	L	H
L	H	H	L	0	$2I_o$	L	H
L	H	H	H	I_o	I_o	N	N
H	L	L	L	I_o	I_o	N	N
H	L	L	H	0	$2I_o$	L	H
H	L	H	L	0	$2I_o$	L	H
H	L	H	H	I_o	I_o	N	N
H	H	L	L	$2I_o$	0	H	L
H	H	L	H	I_o	I_o	N	N
H	H	H	L	I_o	I_o	N	N
H	H	H	H	$2I_o$	0	H	L

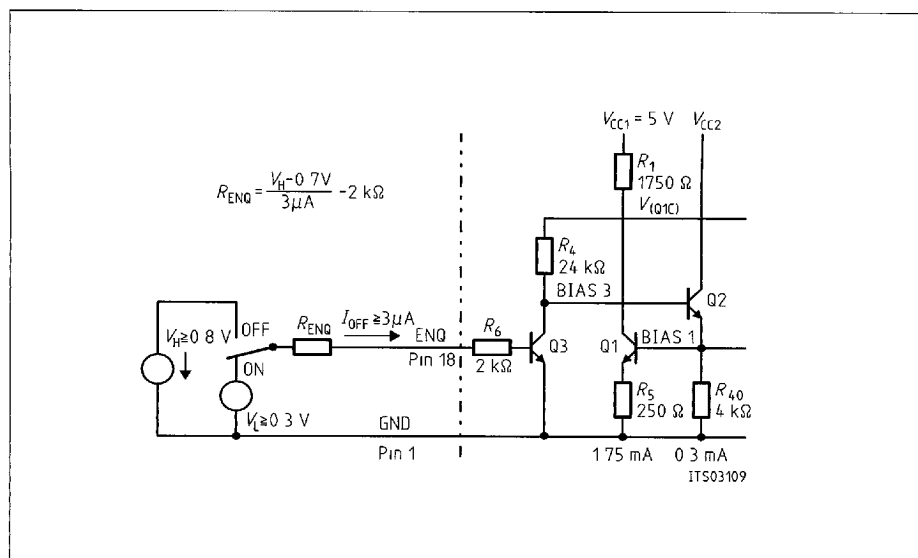
Logic transfer functions: N = neutral; DC balance

I_o = supply current of one Gilbert cell

For lower level this transfer function corresponds to the analog function (A, B, C positive):

$$V(X1A, \overline{X1A}) \times A \times V(X2A, \overline{X2A}) + V(X1B, \overline{X1B}) \times B \times V(X2B, \overline{X2B}) = C \times V(Z, \overline{Z})$$

8235605 0059203 740



Conditions of Power Switching

Power Status	$I(V_{CC1})$	$I(V_{CC2})$	I Output Stage	V_{BIAS1}	V_{BIAS3}	$V(Q1C)$
ON	1.75 mA	15 mA	11 mA	1.16 V	1.84 V	1.93 V
OFF	80 μA	3.6 nA	2.4 nA	0 V	0.29 V	$V_{CC1} = 5V$

Power ON-OFF-levels

The external reference at the modulator input may remain applied after power off.

8235605 0059204 687

Semiconductor Group

Absolute Maximum Ratings $T_A = -40$ to $85\text{ }^{\circ}\text{C}$

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	typ.		
Supply voltage with respect to GND, pin 1	V_{CC1}	- 0.3	7	V	Pin 9
	V_{CC2}	- 0.3	7	V	Pin 10
AC voltages at the differential inputs pins 11 and 12; 19 and 20; 2 and 3; 4 and 15; 16 and 17	V_{Diff}		500	mV	
Current out of pin 4	I_{BIAS1}		3	mA	
Junction temperature	T_j		125	$^{\circ}\text{C}$	
Storage temperature	T_{stg}	- 55	125	$^{\circ}\text{C}$	
Thermal resistance	R_{thSA}		90	K/W	

The pins 7-12,19,20 have no additional internal ESD protection circuitry

Operating Range

Supply voltage	V_{CC1}	4.9	5.1	V	$5\text{ V} \pm 2\%$
Ambient temperature	T_A	- 40	85	$^{\circ}\text{C}$	

AC/DC Characteristics

 $V_{CC1} = V_{CC2} = 5\text{ V}$; $T_A = 0$ to $70\text{ }^{\circ}\text{C}$

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Power consumption	P_{tot}		130		mW	

RF Input

Internal reference	V_{REF}		1.95		V	pin 2, 3
Differential input amplitude			60		mV	

Modulator Inputs, Pin 14, 15 and pin 16,17

External DC reference		2.1 1.9		2.5 2.7	V V	max. single control max. differential control
Control amplitude						till to limit $\hat{V} = 0.46\text{ V}$ if single control till to limit $\hat{V} = 0.23\text{ V}$ if differential control till to limit $\hat{V}/2$ for general application
Resonant circuits, circuit A: pins 11 and 12 circuit B: pins 19 and 20						
Internal DC level			V_{CC2} - 1.5		V	
RF differential mode				0.22	V	
Output swing pin 6, 7		V_{CC2} - 1.4			V	open collectors

Bias Voltages

Pin 4, output BIAS1			1.2		V	
Pin 5, input BIAS2		1	1.2	V_{BIAS1}	V	
Pin 13, output BIAS3			1.85		V	

8235605 0059206 45T

Semiconductor Group

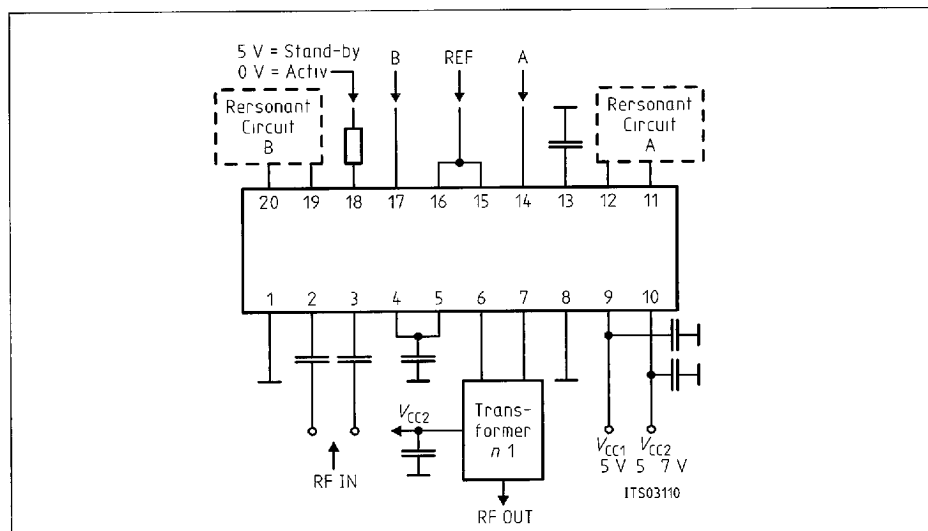
9

AC/DC Characteristics
 $V_{CC1} = 5\text{ V}$, $V_{CC2} = 5\text{ to }7\text{ V}$; $T_A = 0\text{ to }70\text{ }^{\circ}\text{C}$

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	

Differential Amplifier

RF input stage	I_{Q4}		1.75		mA
	I_{Q5}		1.75		mA
Gilbert cells	$I_{Q6} + I_{Q7}$		1.85		mA
	$I_{Q8} + I_{Q9}$		1.85		mA
Level shifters for output stages ¹⁾	$I_{Q10} + I_{Q11}$		2.9		mA
	$I_{Q12} + I_{Q13}$		2.9		mA
Output stage ²⁾	I_{Q14}		11		mA
Supply current	I_{Q1}		1.75		mA
	I_{R40}		0.3		mA
Current sum	ΣI		26.05		mA

**Application Circuit**
¹⁾ This currents may be reduced by an external resistor between pin 8 and pin 1.

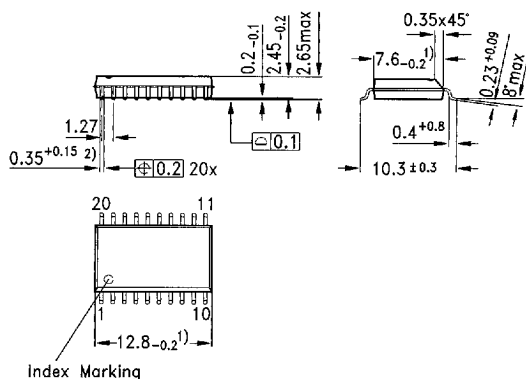
²⁾ If BIAS2 < BIAS1 this current will be reduced.

■ 8235605 0059207 396 ■

Semiconductor Group

10

Plastic Package, P-DSO-20 (SMD)
 (Plastic Dual Small Outline)



- 1) Does not include plastic or metal protrusions of 0.15 max per side
- 2) Does not include dambar protrusion of 0.05 max per side

GPS05094

Sorts of Packing

Package outlines for tubes, trays etc. are contained in our Data Book "Package Information"

SMD = Surface Mounted Device

■ 8235605 0059208 222 ■

Semiconductor Group

11

Dimensions in mm

B111-H6625-
G1-X-7600