Am27S25/27S25A/27S25SA

4096-Bit (512x8) Bipolar Registered PROM with Preset and Clear Inputs

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- 'SA' version offers ultrafast AC performance (25 ns set-up and 12 ns clock-to-output)
- On-chip edge-triggered registers — ideal for pipelined microprogrammed systems
- Versatile synchronous and asynchronous enables for simplified word expansion
- Buffered common Preset ($\overline{PS}$) and Clear ($\overline{CR}$) inputs
- Slim, 24-pin, 300-mil lateral center package occupies approximately 1/3 the board space required by standard discrete PROM and register
- Consumes approximately 1/2 the power of separate PROM/register combination for improved system reliability
- Platinum-Silicide fuses guarantee high reliability, fast programming, and exceptionally high programming yields (typ > 98%)

GENERAL DESCRIPTION

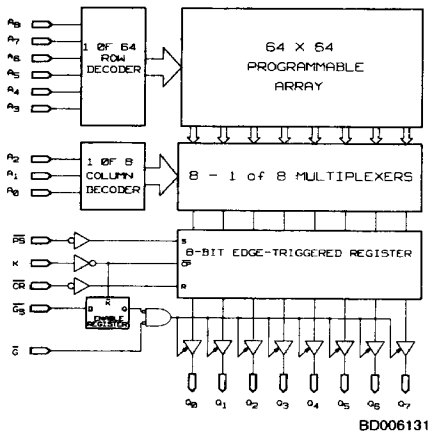
The Am27S25 (512 words by 8 bits) is a fully decoded, Schottky array, TTL Programmable Read-Only Memory (PROM), incorporating D-type master-slave data registers on chip. This device has three-state outputs compatible with low-power Schottky bus standards capable of satisfying the requirements of a variety of microprogrammable controls and state machines.

This device contains an 8-bit parallel data register in the array-to-output path which allows PROM data to be stored while other data is being addressed. This meets the requirements for pipelined microprogrammable control stores where instruction execute and instruction fetch are performed in parallel.

To offer the system designer maximum flexibility, this device contains both asynchronous and synchronous output enables as well as common asynchronous preset and clear register controls.

Upon power-up the outputs ($Q_0 - Q_7$) will be in a floating or high-impedance state.

BLOCK DIAGRAM



BD006131

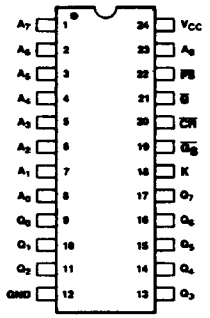
PRODUCT SELECTOR GUIDE

Part Number	Am27S25SA		Am27S25A		Am27S25	
Address Set-up Time (ns)	25	30	30	35	50	55
Clock-to-Ouput Delay (ns)	12	15	20	25	27	30
Operating Range	C	M	C	M	C	M

Publication # 03300 Rev. E Amendment /0
Issue Date: January 1989

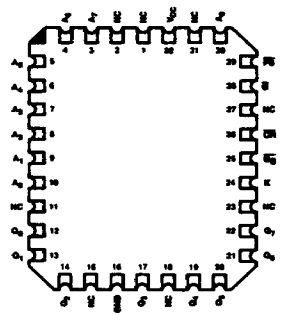
CONNECTION DIAGRAMS
Top View

DIPs*



CD001021

LCC



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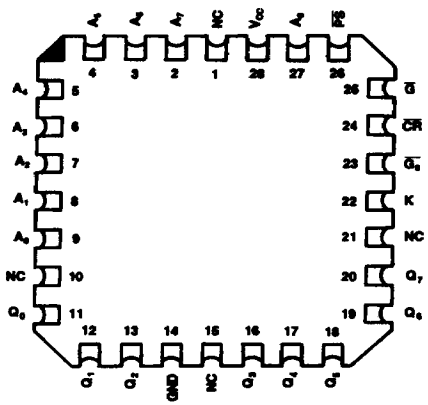
LCC**



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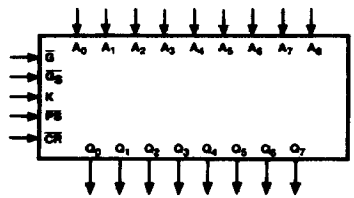
Note: Pin 1 is marked for orientation.
*Also available in a 24-pin Flatpack. Pinout identical to DIPs.
**Also available in a 28-pin square PLCC. Pinout identical to LCC.

LOGIC SYMBOL

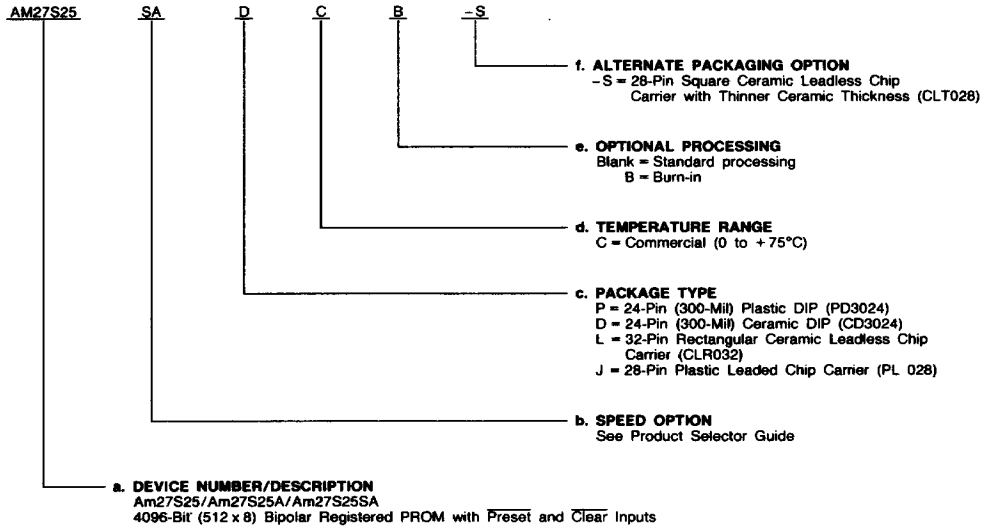


LS000113

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **a. Device Number**
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing
f. Alternate Packaging Option



Valid Combinations	
AM27S25	DC, DCB, PC, PCB, LC, LCB, LC-S, LCB-S JC, JCB
AM27S25A	
Am27S25SA	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

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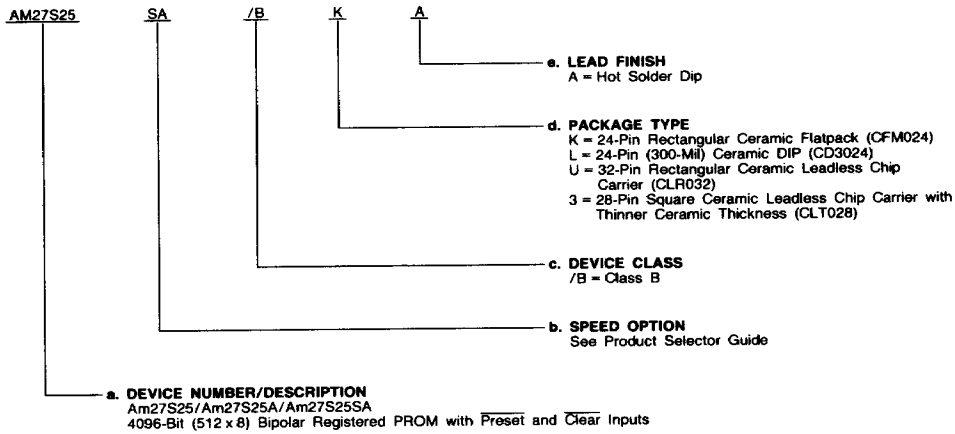
MILITARY ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of: **a. Device Number**
b. Speed Option (if applicable)
c. Device Class
d. Package Type
e. Lead Finish



Valid Combinations	
Am27S25	/BKA, /BLA, /BUA, /B3A
Am27S25A	
Am27S25SA	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

MILITARY BURN-IN

Military burn-in is in accordance with the current revisions of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.

PIN DESCRIPTION

$A_0 - A_8$ Address (Inputs)
The 9-bit field presented at the address inputs selects one of 512 memory locations to be read from.

K Clock
CP is used to load data into the parallel registers from the memory array. Data transfer occurs on the LOW-to-HIGH transition of CP.

$Q_0 - Q_7$ Data Port (Outputs, Three-State)
Parallel data output from the pipeline register. The disabled state of these outputs is floating or high-impedance.

$\overline{G}$ Asynchronous Output Enable
Provides direct control of the Q_n output three-state drivers, independent of CP.

$\overline{G_S}$ Synchronous Output Enable
Controls the state of the Q_n output three-state drivers, in conjunction with CP. This is useful where more than one registered PROM is bussed together for word depth expansion. In this case, the enable becomes the most significant address bit and, as such, must be synchronized with the data.

$\overline{PS}$ Asynchronous Preset
Control pin used to force the state of the output data registers HIGH, independent of CP. This can be used to generate a condition for system interrupt or initialization.

$\overline{CR}$ Asynchronous Clear
Control pin used to force the state of the output data registers LOW, independent of CP. This can be used to generate a condition for system interrupt or initialization.

V_{CC} Power Supply Pin
The most positive of the logic power supply pins.

GND Power Supply Pin
The most negative of the logic power supply pins.

FUNCTIONAL DESCRIPTION

When V_{CC} power is first applied, the synchronous enable ($\overline{G_S}$) flip-flop will be in the set condition causing the outputs ($Q_0 - Q_7$) to be in the OFF or high-impedance state. This occurs regardless of the state of the asynchronous enable input. A LOW-to-HIGH transition of the clock input (K) while $\overline{G_S}$ input is LOW is required after power-up in order to enable the ouputs to an active state. Reading data is accomplished by first applying the binary word address to the address inputs ($A_0 - A_8$) and a logic LOW to the synchronous enable ($\overline{G_S}$). During the address setup time, stored data is accessed and loaded into the master flip-flops of the data register. Since the synchronous enable setup time is less than the address setup requirement, additional decoding delays may occur in the enable path without reducing memory performance. Upon the next LOW-to-HIGH transition of the clock (K), data is transferred to the slave flip-flops which drive the output buffers. Provided that the asynchronous enable ($\overline{G}$) is also LOW, stored data will appear on the outputs ($Q_0 - Q_7$). If $\overline{G_S}$ is HIGH when the positive clock edge occurs, outputs go to the OFF or high-impedance state regardless of the state of $\overline{G}$. The outputs may be disabled at any time by switching $\overline{G}$ to a HIGH level. Following the positive clock edge the address and synchronous enable inputs are free to change; changes will not affect the outputs until another positive clock edge occurs. This unique feature allows the PROM decoders and sense amplifiers to access the next location while previously addressed data remains stable on the outputs. For less complex applications either enable may be effectively eliminated by tying it to ground.

The on-chip edge-triggered register simplifies system timing since the PROM clock may be derived directly from system clock without introducing dangerous race conditions. Other register timing requirements are similar to those of standard Schottky registers and are easily implemented.

The Am27S25 has buffered Asynchronous Preset ($\overline{PS}$) and Clear ($\overline{CR}$) inputs. These functions are common to all registers and are useful during power-up timeout sequences. With outputs enabled, the $\overline{PS}$ input asserted LOW will cause all outputs to be set to a logic 1 (HIGH) state. When the $\overline{CR}$ input is LOW, the internal flip-flops of the data register are reset and a logic 0 (LOW) will appear on all outputs. These functions will control the state of the data register, independent of all other inputs but exclusive of each other.

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ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Ambient Temperature with
Power Applied ..... −55 to +125°C
Supply Voltage ..... −0.5 to +7.0 V
DC Voltage Applied to Outputs
(Except During Programming) ..... −0.5 V to +V_{CC} Max.
DC Voltage Applied to Outputs
During Programming ..... 21 V
Output Current into Outputs During
Programming (Max. Duration of 1 sec) ..... 250 mA
DC Input Voltage ..... −0.5 to +5.5 V
DC Input Current ..... −30 to +5 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Ambient Temperature (T_A) ..... 0 to +75°C
Supply Voltage (V_{CC}) ..... +4.75 to +5.25 V

Military (M) Devices*
Case Temperature (T_C) ..... −55°C to +125°C
Supply Voltage (V_{CC}) ..... +4.5 to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

*Military products 100% tested at T_C = +25°C, +125°C, and −55°C.

DC CHARACTERISTICS over operating ranges unless otherwise specified (for APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions		Min.	Typ.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −2.0 mA V_{IN} = V_{IH} or V_{IL}		2.4			V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 16 mA V_{IN} = V_{IH} or V_{IL}				0.50	V
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs (Note 1)		2.0			V
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs (Note 1)				0.8	V
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = 0.45 V				−0.250	mA
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}				40	μA
I_{SC}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.0 V (Note 2)		−20		−90	mA
I_{CC}	Power Supply Current	All inputs = GND, V_{CC} = Max.				185	mA
V_I	Input Clamp Voltage	V_{CC} = Min., I_{IN} = −18 mA				−1.2	V
I_{CEX}	Output Leakage Current	V_{CC} = Max. V_E = 2.4 V	V_O = V_{CC}			40	μA
			V_O = 0.4 V			−40	
C_{IN}	Input Capacitance	V_{CC} = 5.00 V., T_A = 25°C V_{IN}/V_{OUT} = 2.0 V. @ f = 1 MHz (Note 4)			4		pF
C_{OUT}	Output Capacitance				8		

Notes: 1. V_{IL} and V_{IH} are input conditions of output tests and are not themselves directly tested. V_{IL} and V_{IH} are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
2. Only one output should be shorted at a time. Duration of the short circuit should not be more than one second.
3. These parameters are not 100% tested, but are periodically sampled at initial characterization and at any time the design is modified where capacitance may be affected.
4. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over operating ranges unless otherwise specified (for APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted*) (Note 1)

No.	JEDEC Parameter Symbol	Parameter Description		Am27S25SA Min.	Am27S25SA Max.	Am27S25A Min.	Am27S25A Max.	Am27S25 Min.	Am27S25 Max.	Unit
1	TAVKH	Address to K HIGH Setup Time	COM'L	25		30		50		ns
			MIL	30		35		55		
2	TKHAX	Address to K HIGH Hold Time	COM'L	0		0		0		ns
			MIL	0		0		0		
3	TKHQV1	Delay from K HIGH to Output Valid, for initially active outputs (HIGH or LOW) (Note 3)	COM'L	4	12		20		27	ns
			MIL	4	15		25		30	
4	TKHKL TKLKH	K Pulse Width (HIGH or LOW)	COM'L	15		20		20		ns
			MIL	20		20		20		
5	TGLQV	Asynchronous Output Enable LOW to Output Valid (HIGH or LOW)	COM'L		20		25		35	ns
			MIL		25		30		45	
6	TGHQZ	Asynchronous Output Enable HIGH to Output Hi-Z (See Note 2)	COM'L		20		25		35	ns
			MIL		25		30		45	
7	TGSVKH	$\overline{G_S}$ to K HIGH Setup Time	COM'L	10		10		15		ns
			MIL	10		10		15		
8	TKHGSX	$\overline{G_S}$ to K HIGH Hold Time	COM'L	0		5		5		ns
			MIL	0		5		5		
9	TKHQV2	Delay from K HIGH to Output Valid, for initially Hi-Z outputs	COM'L		20		25		35	ns
			MIL		25		30		45	
10	TKHQZ	Delay from K HIGH to Output Hi-Z (See Note 2)	COM'L		20		25		35	ns
			MIL		25		30		45	
11	TPSLQV TCRLQV	Delay from $\overline{PS}$ or $\overline{CR}$ LOW to Output Valid (HIGH or LOW)	COM'L		20		20		25	ns
			MIL		25		25		30	
12	TPSHKH TCRHKH	Asynchronous $\overline{PS}$ or $\overline{CR}$ Recovery Time	COM'L	15		20		20		ns
			MIL	20		25		25		
13	TPSLPSH TCRLCRH	Asynchronous $\overline{PS}$ or $\overline{CR}$ Pulse Width (LOW)	COM'L	15		20		20		ns
			MIL	20		25		25		

See also Switching Test Circuits.

Notes: 1. Tests are performed with input transition time of 5 ns or less, timing reference levels of 1.5 V, and input pulse levels of 0 to 3.0 V using test load in A. under Switching Test Circuits.
2. TGHQZ and TKHQZ are measured at steady state HIGH output voltage – 0.5 V and steady state LOW output voltage + 0.5 V output levels using the test load in B. under Switching Test Circuits.
3. Minimum delay is guaranteed by design and supported by characterization data.

*Subgroups 7 and 8 apply to functional tests.

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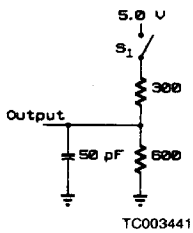
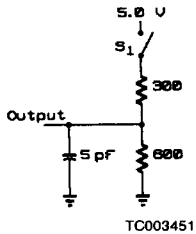
SWITCHING TEST CIRCUITS



A. Output Load for all tests except TGVQZ and TKHQZ

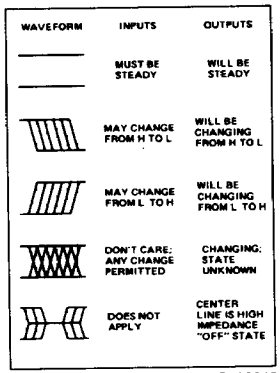


B. Output Load for TGVQZ and TKHQZ

Notes: 1. All device test loads should be located within 2" of device output pin.
2. S_1 is open for Output Data HIGH to Hi-Z and Hi-Z to Output Data HIGH tests. S_1 is closed for all other AC tests.
3. Load capacitance includes all stray and fixture capacitance.

SWITCHING WAVEFORMS

KEY TO SWITCHING WAVEFORMS



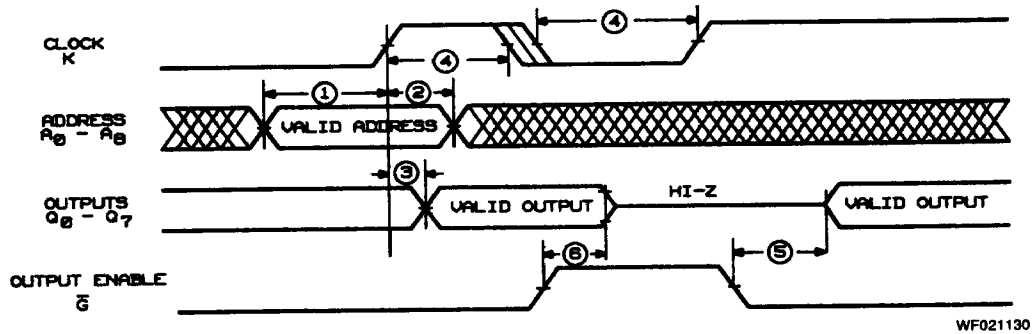


Diagram A. Using Asynchronous Enable

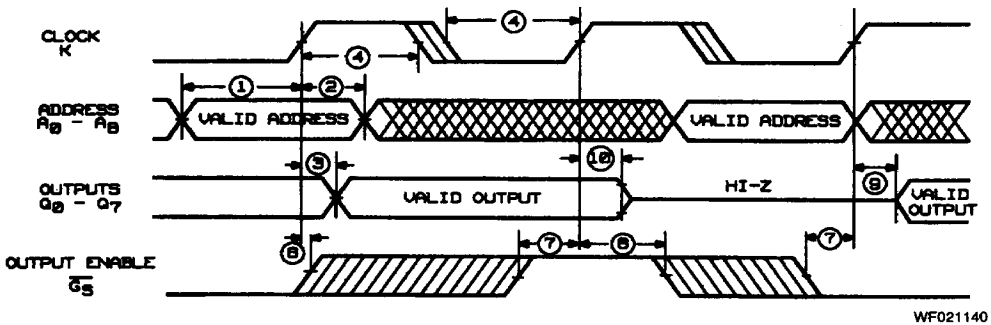


Diagram B. Using Synchronous Enable

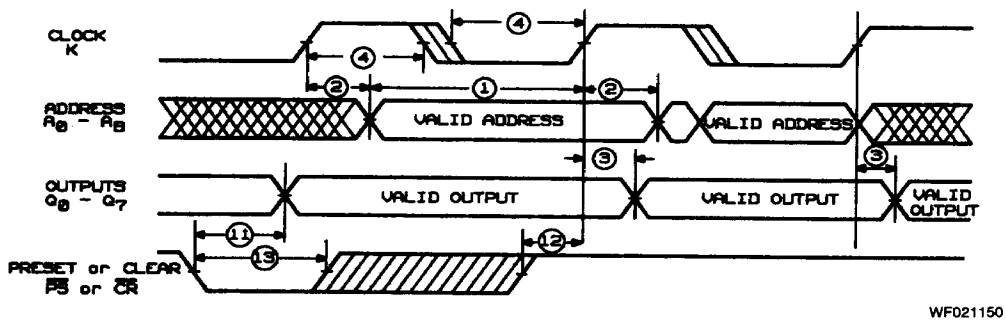


Diagram C. Using Asynchronous $\overline{\text{PRESET}}$ or $\overline{\text{CLEAR}}$

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