8-BIT MULTIPLYING DAC

GENERAL DESCRIPTION

The PNA7518 is a NMOS 8-bit multiplying digital-to-analogue converter (DAC) designed for video applications. The device converts a digital input signal into a voltage-equivalent analogue output at a sampling rate of 30 MHz.

The input signal is latched, then fed to a decoder which switches a transfer gate array (1 out of 256) to select the appropriate analogue signal from a resistor chain. Two external reference voltages supply the resistor chain. The multiplying capability is obtained by using the independent reference voltages.

The input latches are positive-edge triggered. The output impedance is approximately 0,5 kΩ depending on the applied digital code. An additional operational amplifier is required for the 75 Ω output impedance. Two's complement is selected when STC (pin 11) is HIGH or is not connected. STC inverts the most significant bit (MSB).

Features

- TTL input levels
- Positive-edge triggered
- Analogue voltage output at 30 MHz sampling rate
- Binary or two's complement input
- Output voltage accuracy to within ± ½ of the input LSB
- Multiplying capability
- 12 MHz bandwidth
- 8-bit resolution

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range		V_{DD}	4,5	–	5,5	V
Supply current		I_{DD}	–	–	80	mA
Reference voltage LOW		V_{refL}	0	–	2,0	V
Reference voltage HIGH		V_{refH}	0	–	2,0	V
Static non-linearity	note 1		–	–	± 0,5	LSB
Bandwidth at −3 dB	note 2	B	12	–	–	MHz
Clock frequency	T_{amb} = 25 °C; V_{DD} = 5 V	f_{CLK}	10	–	30	MHz
Total power consumption		P	–	–	470	mW

For explanation of notes see "Notes to the characteristics".

Applications

- Video data conversion
- CRT displays
- Waveform/test signal generation
- Colour/black-and-white graphics

PACKAGE OUTLINE

16-lead DIL; plastic (SOT38D)

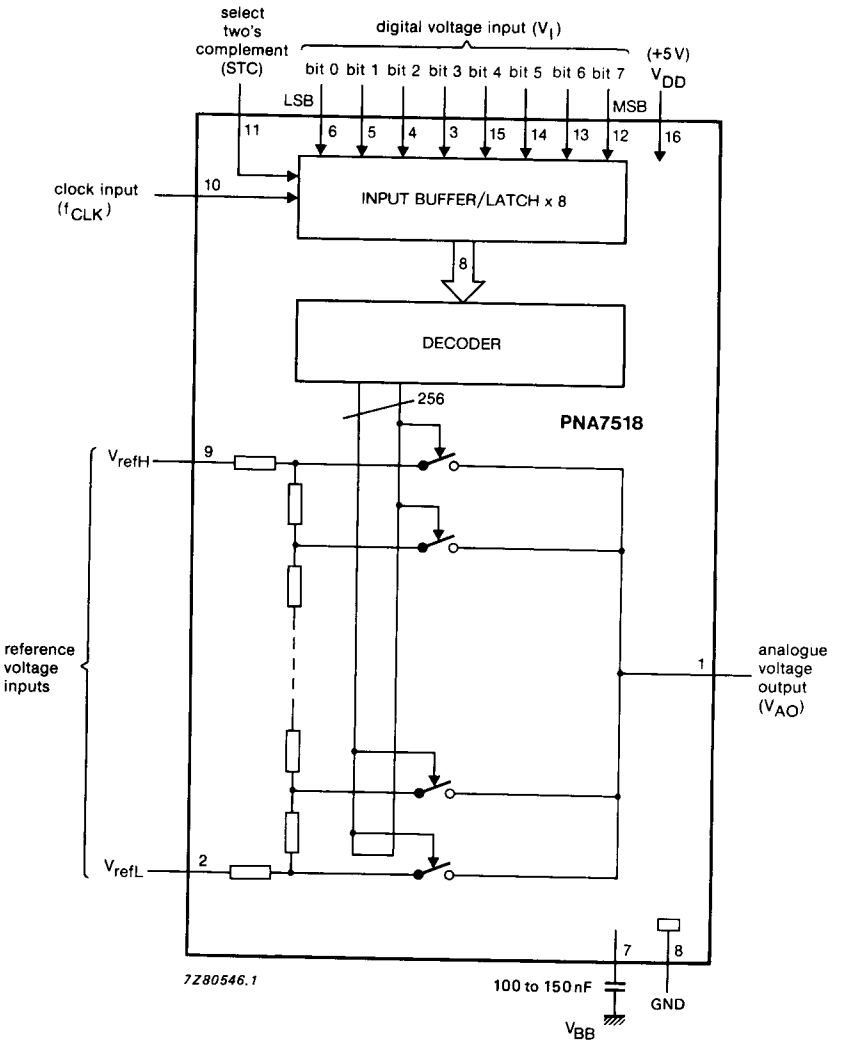

Fig. 1 Block diagram.

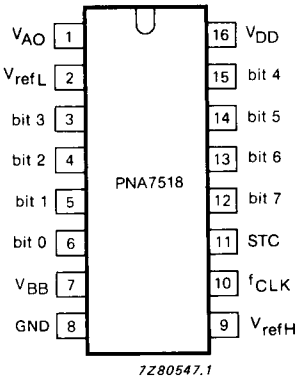

Fig. 2 Pinning diagram.

PINNING

1	V_{AO}	analogue output voltage
2	V_{refL}	reference voltage LOW
3	bit 3	digital voltage inputs (V_I)
4	bit 2	
5	bit 1	
6	bit 0	least-significant bit (LSB)
7	V_{BB}	back bias
8	GND	ground
9	V_{refH}	reference voltage HIGH
10	f_{CLK}	clock input
11	STC	select two's complement
12	bit 7	most-significant bit (MSB)
13	bit 6	digital voltage inputs (V_I)
14	bit 5	
15	bit 4	
16	V_{DD}	positive supply voltage

DEVELOPMENT DATA

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage range	V_{DD}	−0,5	7,0	V
Input voltage B0 to B7 and STC	V_I	−0,5	7,0	V
Output voltage	V_{AO}	−0,5	7,0	V
Total power dissipation	P_{tot}	–	800	mW
Storage temperature range	T_{stg}	−65	+ 150	°C
Operating ambient temperature range	T_{amb}	0	+ 70	°C
Temperature range with back bias	T_{BB}	−10	+ 80	°C
Clock frequency	f_{CLK}	10	–	kHz

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see "Handling MOS Devices").

CHARACTERISTICS

V_{DD} = 4,5 to 5,5 V; C_{BB} = 100 nF; T_{amb} = 0 to + 70 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage		V_{DD}	4,5	–	5,5	V
Supply current		I_{DD}	–	–	80	mA
Inputs B0 to B7, CLK, and STC						
Input voltage LOW		V_{IL}	0	–	0,8	V
Input voltage HIGH		V_{IH}	2	–	V_{DD}	V
Input leakage current (except STC)		I_{LI}	–	–	10	μA
STC input current		I_I	–	–	100	μA
Reference voltages						
Reference voltage LOW		V_{refL}	0	–	2	V
Reference voltage HIGH		V_{refH}	0	–	2	V
Reference ladder between V_{refL} and V_{refH}		R_{ref}	150	–	300	Ω
Linearity						
Static non-linearity	note 1		–	–	± 0,5	LSB
Clock input						
Clock frequency	T_{amb} = 25 °C; V_{DD} = 5 V	f_{CLK}	10	–	30	MHz
Bandwidth						
Bandwidth at −3 dB	note 2	B	12	–	–	MHz

Notes to the characteristics

1. Measured at R_{AO} = 200 kΩ; V_{refL} = 0 V; V_{refH} = 2 V and f_{CLK} = 28 MHz.
2. Measured at V_{DD} = 5 V; T_{amb} = 25 °C; V_{refL} = 0 V; V_{refH} = 2 V; f_{CLK} = 30 MHz; duty cycle = 0,5; rise and fall time = 3 ns and a 6 pF load at the analogue output. The analogue output signal is scanned by an external sample and hold circuit.

DEVELOPMENT DATA

APPLICATION INFORMATION

This section provides additional information to the characteristics. The values are measured on a sampling basis.

Table 1 Application characteristics

parameter	symbol	typ.	unit
Supply current	I_{DD}	50	mA
Power consumption	P	270	mW
Minimum clock frequency	f_{CLK}	10	kHz
Maximum clock frequency	f_{CLK}	45	MHz
Static non-linearity		± 0,25	LSB
Reference ladder	R_{ref}	210	Ω
Bandwidth	B	15	MHz
Set-up time	t_{SU}	3	ns
Input hold time	t_{HD}	4	ns
Propagation delay	t_{PD}	$1 \times t_{CLK} + 30$	ns

Where:

V_{DD} = 5 V; T_{amb} = 25 °C; V_{refL} = 0 V; V_{refH} = 2,0 V.

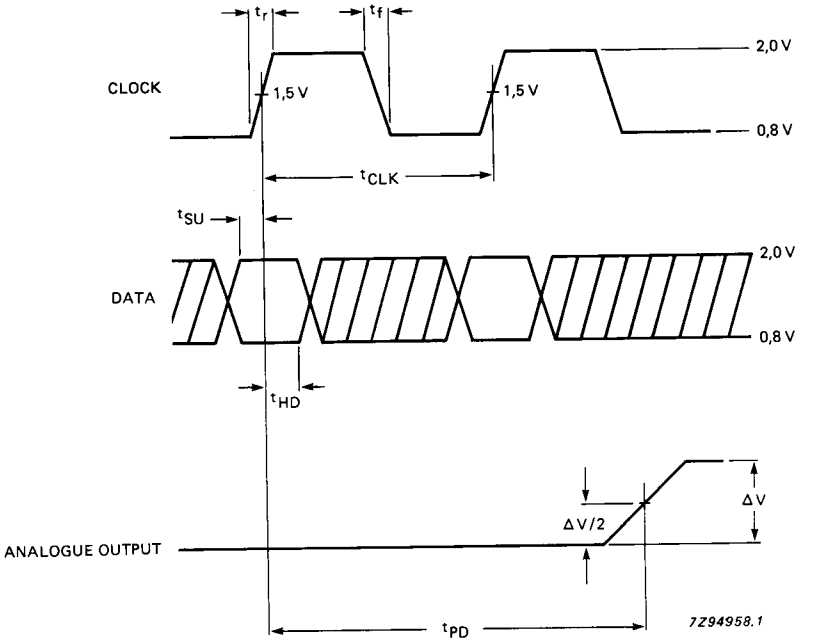

Fig. 3 Switching characteristics.