T-49-17-01

PRELIMINARY

DATA SHEET

ZyMOS

POACH/AT™

POACH 1/POACH 2

FEATURES

- Fully IBM PC AT™-Compatible
- Two Chip Set replaces the major logic functions of the IBM PC AT Motherboard including the functions of all the Microprocessor Peripherals:
  - — 8259A Programmable Interrupt Controller (Master)
  - — 8259A Programmable Interrupt Controller (Slave)
  - — 8254 Programmable Interval Timer
  - — 8284A Clock Generator
  - — 82284 Clock Generator & Ready Interface
  - — 82288 Bus Controller
  - — 8237 DMA Controller (Byte)
  - — 8237 DMA Controller (Word)
  - — 6818 Real Time Clock
  - — 74LS612 Memory Mapper
- Includes:
  - — Refresh Generation Logic
  - — Refresh/DMA Arbitration
  - — 10 bit Refresh Counter
  - — Address/Data Bus Control
  - — 16 to 8 bit Conversion Logic
- A High Integration 80286 Design Solution
- Numerical Processor Control
- Up to 12MHz System Clock Rate
- Single +5V Power Supply
- Low Power CHMOS-3
- Microprocessor Peripheral Functions are also available as standard cells in the ZyMOS cell library for unique design integration

DESCRIPTION

The ZyMOS POACH/AT (PC on a Chip) chip set is a two-chip implementation of the LSI/MSI/SSI logic controlling the IBM Personal Computer AT. The devices provide a low-power, highly integrated PC AT design solution that may also be applied to any 80286-based system. POACH 1 performs the functions of the 82284 Clock Generator & READY Interface, 82288 Bus Controller for 80286 processors, 6818 Real Time Clock/RAM, and the Master/Slave implementation of the dual 8259A Programmable Interrupt Controllers as well as Command Delay, Shut Down, Address/Data Bus Control and Ready Generation logic. POACH 2 includes the 8254 Programmable Interval Timer, 8284A Clock Generator, LS612 Memory Mapper and the dual 8237 DMA Controller functions as well as Refresh Generation and Refresh/DMA Arbitration Logic.

POACH/AT peripherals are fully compatible with those used in standard PC AT designs; the chip set is fully IBM PC AT-compatible. High-speed operation is possible by selecting the optimum RAM/buffer combination. Occupying only two 84-pin plastic leaded chip carriers on the AT motherboard, POACH/AT implementation results in a dramatic reduction in board size and power consumption.

APRIL 1988

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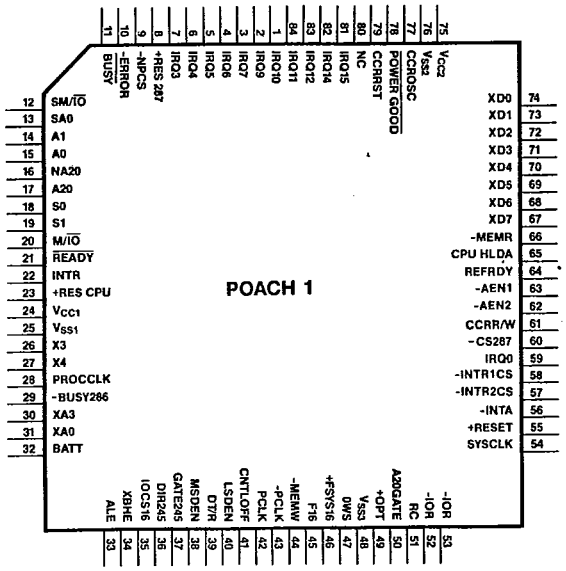
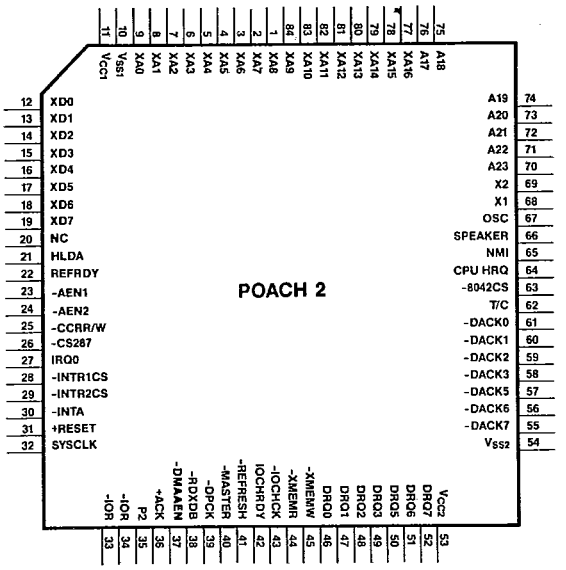
POACH 1/POACH 2



Pin Diagram POACH 1



Pin Diagram POACH 2

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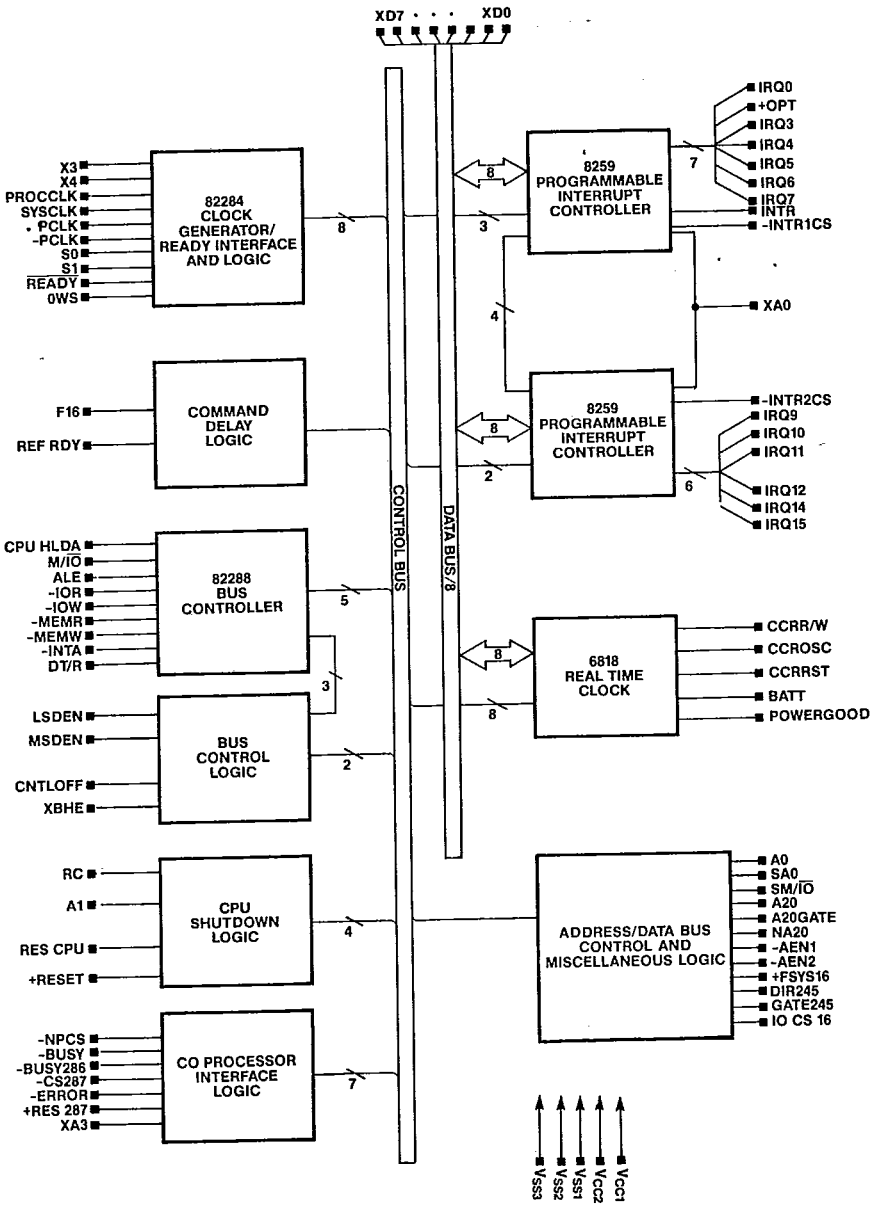

POACH 1—Block Diagram

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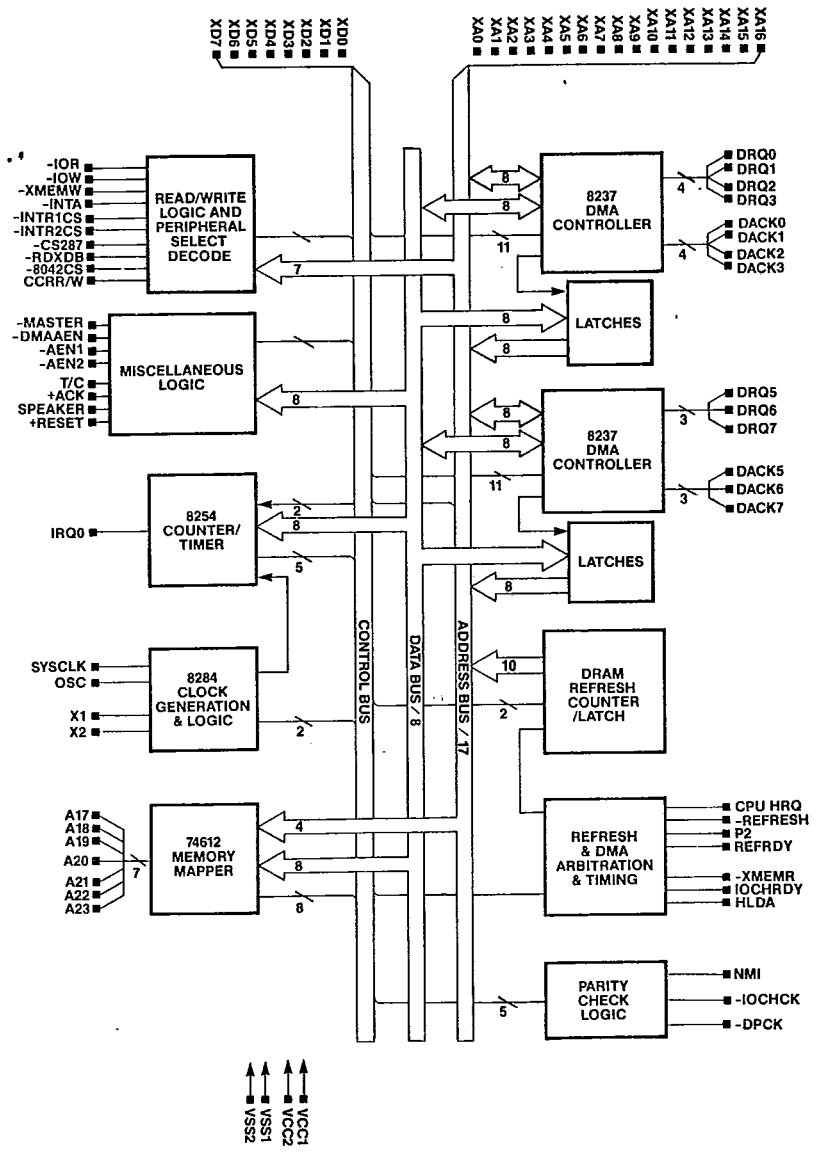

POACH 2—Block Diagram

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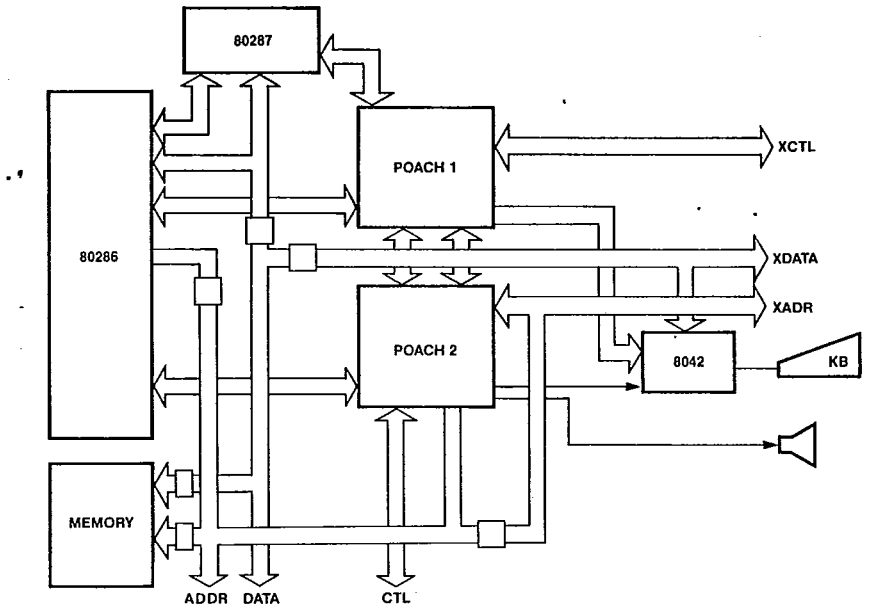

Block Diagram of POACH 1 and POACH 2 for PC/AT

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POACH 1 Pin Description

Pin No.	Symbol	Type	Description
15	A0	I	ADDRESS 0 input from the CPU. It is used to generate SA0.
14	A1	I	ADDRESS 1 input from the CPU. It is used in conjunction with M/IO, S0 and S1 to detect a CPU Shutdown condition.
17	A20	O	ADDRESS 20 is the A20 (NA20) line from the CPU after conditioning by the A20GATE signal. During a CPU Hold A20 goes to a high impedance state.
50	A20GATE	I	A20GATE from the Keyboard Controller is used to force A20 low. When A20GATE is low, A20 on the CPU Address Bus is forced low. When A20GATE is high, A20 follows the CPU Address 20. Tie directly to the P21 Pin of the Keyboard Controller.
62 63	-AEN2 -AEN1	I	ADDRESS ENABLE 1 & 2 from DMA's 1 & 2, respectively. The signal is the result of the DMAAEN pin NAND'd with -MASTER. Tie directly from the -AEN1 and -AEN2 pins of POACH 2.
33	ALE	O	ADDRESS LATCH ENABLE is an active high signal that controls the address latches used to hold addresses during bus cycles. ALE is held inactive for Halt bus cycles.
32	BATT	I	BATTERY Power to the Clock Calendar and RAM.
29	-BUSY286	O	-BUSY286 is an active low output indicating the operating condition of the 80287 coprocessor to the processor. It is normally tied to the processor -BUSY pin.
11	-BUSY	I	-BUSY is an active low input from the 80287 to indicate that it is currently executing a command. It is used to generate the -BUSY286 output signal.
77	CCROSC	I	CLOCK CALENDAR OSCILLATOR; 32.768 KHz signal.
79	CCRRST	I	CLOCK CALENDAR RESET signal for the Real Time Clock. This is an active low input.
61	CCRR/W	I	CLOCK CALENDAR READ/WRITE signal for the Real Time Clock. A high enables READ/WRITE operation to the real-time clock. Tie directly to the CCRR/W Pin of POACH 2.
41	CNTLOFF	O	CONTROL OFF is used to enable the low byte data bus latch during byte accesses. This signal is an active high.

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POACH 1 Pin Description (Continued)

Pin No.	Symbol	Type	Description
65	CPU HLDA	I	CPU HOLD ACKNOWLEDGE is an active high input from the processor. An active condition indicates that the CPU has relinquished the bus to another bus master in the system.
60	-CS287	I	CHIP SELECT 287 is used to derive the -NPCS signal. Tie directly to the -CS287 pin of POACH 2.
36	DIR245	O	DIRECTION-245 controls the high to low byte and low to high byte conversion during data transfers to and from 8-bit peripherals.
39	DT/$\overline{R}$	O	DATA TRANSMIT/RECEIVE establishes the data direction to and from the local data bus. When high, this output signals a CPU write bus cycle. A low indicates a CPU read bus cycle is being performed. This signal is always high when no bus cycle is active.
10	-ERROR	I	ERROR is an active low input from the numeric processor indicating that an unmasked error condition exists. Tie directly to the -ERROR Pin of the 80287.
45	F16	I	F16 is an active high input indicating a word memory access. It is used to inhibit command delays for memory accesses.
46	+FSYS16	I	A latched version of F16.
37	GATE245	O	GATE245 is an active low output. When active it enables the bus transceiver that performs the high to low byte conversion with the DIR245 signal. Conversion does not take place if A0 = 0 which indicates a word transfer.
56	-INTA	O	INTERRUPT ACKNOWLEDGE instructs an interrupting device that its interrupt request is being acknowledged. This signal is active low. -INTA is tri-stated when CPU HLDA is high and CNTLOFF is low. Tie directly to the -INTA pin of POACH 2.
22	INTR	O	INTERRUPT REQUEST is connected directly to the CPU's interrupt pin. INTR is active high, and is generated when a valid interrupt request has been asserted.
58	-INTR1CS	I	INTERRUPT CONTROLLER 1 (MASTER) CHIP SELECT is an active low output that is used to select the Interrupt Controller as an I/O device. This allows communication between the master interrupt controller and the CPU via the 'X' Data Bus. Tie directly to the -INTR1CS pin of POACH 2.

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POACH 1 Pin Description (Continued)

Pin No.	Symbol	Type	Description
57	-INTR2CS	I	INTERRUPT CONTROLLER 2 (SLAVE) CHIP SELECT is an active low output that is used to select the Interrupt Controller as an I/O device. This allows communication between the slave interrupt controller and the CPU via the 'X' data bus. Tie directly to the -INTR2CS Pin of POACH 2.
35	-IO CS 16	I	I/O 16-BIT CHIP SELECT signals the system that the current data transfer is a 16-bit, one wait-state, I/O cycle. It is derived from an address decode and is an active low signal.
53	-IOR	I/O	I/O READ signal instructs a selected I/O device to drive its data onto the data bus. The -IOR signal is active low. It is tri-stated when CPU HLDA is high and CNTLOFF is low.
52	-IOW	I/O	I/O WRITE signal instructs a selected I/O device to read the data on the data bus. The -IOW signal is active low. It is tri-stated when CPU HLDA is high and CNTLOFF is low.
59	IRQ0	I	INTERRUPT REQUEST 0 (system timer) receives interrupt requests from channel 0 of the timer/counter. Tie directly to the IRQ0 pin of POACH 2.
3-7 1-2 83-84 81-82	IRQ7-IRQ3 IRQ10-IRQ9 IRQ12-IRQ11 IRQ15-IRQ14	I I I I	INTERRUPT REQUESTS 3-7, 9-12, and 14-15 are used to signal the CPU that an I/O device needs attention. The interrupt requests are prioritized with IRQ9-IRQ12 and IRQ14-IRQ15 having the highest priority (IRQ9 highest) and IRQ3-IRQ7 having the lowest priority (IRQ7 lowest). IRQn signals are active high. The requesting signal is held high until the CPU acknowledges the interrupt request.
40	LSDEN	O	LEAST SIGNIFICANT DATA ENABLE is an active low output. When active, it enables the transceiver/receiver connected to the least significant byte of the local data bus.
66	-MEMR	I/O	MEMORY READ COMMAND instructs a memory device to drive data onto the data bus. This signal is active low. -MEMR is active on all memory read cycles. It is tri-stated when CPU HLDA is high and CNTLOFF Output is low.

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POACH 1 Pin Description (Continued)

Pin No.	Symbol	Type	Description
44	-MEMW	I/O	MEMORY WRITE COMMAND instructs a memory device to read the data on the data bus. This signal is active low. -MEMW is active on all memory write cycles. It is tri-stated when CPU HLDA is high and CNTLOFF Output is low.
38	MSDEN	O	MOST SIGNIFICANT DATA ENABLE is an active low output. When active, it enables the transceiver connected to the most significant byte of the local data bus.
20	M/$\overline{IO}$	I	MEMORY-$\overline{INPUT\ OUTPUT}$ is the M/$\overline{IO}$ signal from the CPU. When high, it indicates a memory access. When low, it indicates an I/O access. It is used to generate the memory and I/O signals for the system.
16	NA20	I	NA20 is the CPU address 20. POACH conditions this signal with A20GATE to produce A20. This pin is tied directly to the CPU A20 output.
80	NC		Do Not Connect.
9	-NPCS	O	NUMERICAL PROCESSOR CHIP SELECT is an active low output used to select the 80287 Numerical Processor. It is tied directly to the NPS1 pin of the 80287.
49	+OPT	I	KEYBOARD OUTPUT BUFFER FULL is an active high signal from the Keyboard Controller P24 Pin. The signal is an interrupt request (IRQ1) signaling a full keyboard buffer.
47	0WS	I	ZERO WAIT STATE option. When pulled active (low), the current processor cycle can be terminated.
42	PCLK	O	PERIPHERAL CLOCK is half the rate of PROCCLK. It is used to clock peripheral controllers, specifically XTAL1 of the Keyboard Controller.
43	-PCLK	O	PERIPHERAL CLOCK INVERTED is the inverse of PCLK. It has been made available specifically for XTAL2 of the Keyboard Controller.
28	PROCCLK	O	PROCESSOR CLOCK provides the clock signal for the CPU and 80287 Numerical Processor. It is equal to the frequency of the crystal across pins X3 and X4. Tie directly to the CLK Pins of the 80286 and 80287.
78	$\overline{POWER\ GOOD}$	I	POWER GOOD is an active low input that indicates that system power is sufficient to maintain the integrity of the system. If high, it will force a system reset.

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POACH 1 Pin Description (Continued)

Pin No.	Symbol	Type	Description
51	RC	I	RESET CPU from the keyboard controller P21 Pin.
21	$\overline{\text{READY}}$	O	$\overline{\text{READY}}$ is an active low output which signals that the current bus cycle is to be completed. S0, S1, POWER GOOD, and 0WS control the $\overline{\text{READY}}$.
64	REFRDY	I	REFRESH/IO-CHANNEL-READY is generated by POACH 2. It is used to preset the READY Interface Asynchronous READY ($\overline{\text{ARDY}}$).
8	+RES 287	O	RESET 80287 is the reset signal for the 80287 Numerical Processor.
23	RES CPU	O	RESET CPU is the reset signal for the CPU. Active high, RESCPU is generated when either POWERGOOD or RC become active, or when the CPU generates a HALT status by forcing M/$\overline{\text{IO}}$ high, S0, S1 and A1 low. If this signal is initiated by RC, or by M/$\overline{\text{IO}}$, S0, S1 and A1, it will remain active for 16 PROCCLK cycles.
55	+RESET	O	RESET (SYSTEM) is an active high output derived from the POWER GOOD input. +RESET is used to force the system into an initial state. When +RESET is active, $\overline{\text{READY}}$ will also be active (Low).
18, 19	S0, S1	I	STATUS inputs from the CPU. The status signals are used by the bus controller to determine the state of the CPU.
13	SA0	O	ADDRESS 0 of the CPU bus. SA0 outputs A0 from the CPU during local CPU cycles. During a CPU Hold SA0 goes to a high impedance state so that another master on the expansion bus can take control. During an interrupt acknowledge this signal will be forced low.
12	SM/$\overline{\text{IO}}$	I	SYSTEM MEMORY-INPUT OUTPUT is the M/$\overline{\text{IO}}$ signal from the CPU, conditioned by ALE.
54	SYSCLK	O	SYSTEM CLOCK is the result of PROCCLK divided by two, thus synchronized to the processor's T-states. It may be used to clock peripheral devices that must be synchronized to the CPU.
24 75	Vcc1 Vcc2		POWER: +5-Volt supply.
25 76 48	Vss1 Vss2 Vss3		GROUND.

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POACH 1 Pin Description (Continued)

Pin No.	Symbol	Type	Description
26 27	X3 X4	I O	CRYSTAL inputs used to generate PROCCLK and SYSCLK. The crystal frequency must be twice the processor clock frequency. Alternatively, an oscillator may be connected to X3.
31	XA0	I	ADDRESS 0 is used by the 8259A to decipher command words the CPU issues. XA0 works in conjunction with the read, write and chip select signals to the interrupt controller in determining whether the CPU wishes to issue a command or read the status of the controller.
30	XA3	I	ADDRESS 3 is used for generating the chip select and reset signals for the 80287.
34	XBHE	I/O	BUS HIGH ENABLE is an active low signal which is used by POACH 1 to generate the MSDEN signal.
67-74	XD7-XD0	I/O	Data Bus 0-7 for the peripheral bus. The direction of the bus is determined by the -RDXDB signal from POACH 2. Its used by the 8259A to decipher command words the CPU issues.

POACH 2 Pin Description

63	-8042CS	O	8042 CHIP SELECT is an active low, chip select signal for the Keyboard Controller.
70-76	A23-A17	O	A23-A17 are the Address bits 17-23 of the CPU Address bus. They are outputs directly from the Memory Mapper Pins MO1-MO7 and supply page information during DMA transfers. These outputs are tri-stated unless HLDA and -MASTER are high.
36	+ACK	O	ACKNOWLEDGE is an active low output. When active it enables the bus transceiver between the system and peripheral (XBUS) bus. +ACK is used in conjunction with -RDXDB which controls the direction of the bus transceiver.
23 24	-AEN1 -AEN2	O O	ADDRESS ENABLE FROM DMAs 1 & 2, respectively. The signal is the result of the DMA's AEN signal NAND'd with -MASTER. Tie directly to the -AEN1 and -AEN2 pins of POACH 1.
25	CCRR/W	O	CLOCK CALENDAR READ/WRITE signal for the real-time clock. A high enables READ/WRITE operations to the real-time clock. Tie directly to the CCRR/W pin of POACH 1.

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POACH 2 Pin Description (Continued)

Pin No.	Symbol	Type	Description
64	CPU HRQ	O	CPU HOLD REQUEST is an active high output indicating a DMA request to the CPU. It is also active during refresh cycles. CPU HRQ is normally connected to the 80286 HOLD Pin.
26	-CS287	O	CHIP SELECT 287 is used by POACH 1 to derive the -NPCS signal. Tie directly to the -CS287 pin of POACH 1.
61-58 57-55	-DACK0-3 -DACK5-7	O O	DMA ACKNOWLEDGE 0-3 and 5-7 are used to acknowledge DMA requests (DRQ0-3 & 5-7). The output signal is an active low.
37	-DMAAEN	O	DMA ADDRESS ENABLE is an active low signal and is active when an I/O device is making a DMA access to system memory or during refresh.
39	-DPCK	I	DATA PARITY CHECK is used to generate NMI. This input is active low.
46-49 50-52	DRQ0-3 DRQ5-7	I I	DMA REQUEST 0-3 & 5-7 are synchronous channel requests used by peripheral devices and I/O processors to gain DMA service. The requests are prioritized with DRQ0 having the highest and DRQ7 having the lowest priorities. A DRQ line must be held active (high) until the corresponding DACK line goes active.
21	HLDA	I	HOLD ACKNOWLEDGE is an active high input that is equivalent to CPU HLDA. An active condition indicates that the CPU has relinquished the bus to another bus master in the system.
30	-INTA	I	INTERRUPT ACKNOWLEDGE instructs an interrupting device that its interrupt is being acknowledged, and the device may place its interrupt vector onto the data bus. This input signal is active low. -INTA is used by POACH 2 in the generation of -RDXDB. From POACH 1 Pin 56.
28	-INTR1CS	O	INTERRUPT CONTROLLER 1 (MASTER) CHIP SELECT is an active low output that is used by POACH 1 to select the Interrupt Controller as an I/O device. This allows communication between the Master Interrupt Controller and the CPU via the 'X' Data Bus. Tie directly to the -INTR1CS pin of POACH 1.
29	-INTR2CS	O	INTERRUPT CONTROLLER 2 (SLAVE) CHIP SELECT is an active low output that is used by POACH 1 to select the Interrupt Controller as an I/O device. This allows communication between the Slave Interrupt Controller and the CPU via the 'X' Data Bus. Tie directly to the -INTR2CS Pin of POACH 1.

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POACH 2 Pin Description (Continued)

Pin No.	Symbol	Type	Description
43	-IOCHCK	I	I/O CHANNEL CHECK is an active low input. It is used to indicate an uncorrectable system error. It provides the system with parity error information about memory or devices on the I/O channel.
42	IOCHRDY	I	I/O CHANNEL READY is generated by an I/O device. When low it indicates a 'not ready' condition and forces the insertion of wait states in I/O or Memory accesses by the I/O device. When active (high), it will allow the completion of a memory or an I/O access by the I/O device.
33	-IOR	I/O	I/O READ signal instructs a selected I/O device to drive its data onto the data bus. The -IOR signal is active low. It is used for data transfers between the CPU and by DMA transfers.
34	-IOW	I/O	I/O WRITE signal instructs a selected I/O device to read the data on the data bus. The -IOW signal is active low. It is used for data transfers between the CPU and by DMA transfers.
27	IRQ0	O	INTERRUPT REQUEST 0 (System Timer) from Channel 0 of the Timer/Counter. Tie directly to the IRQ0 Pin of POACH 1.
40	-MASTER	I	-MASTER is an active low input used in conjunction with a DRQ line to gain control of the system. A DMA controller or processor on the I/O channel may issue a DRQ to a DMA channel and receive a -DACK. The I/O processor may then activate -MASTER which will allow it to control the system address, data, and control lines.
20	NC		Do Not Connect.
65	NMI	O	NON-MASKABLE INTERRUPT is an active high output that is connected to the CPU NMI pin.
67	OSC	O	OSCILLATOR output is the clock frequency of the crystal connected accross X1-X2. It is the OSC output from the Clock Generator.
35	P2	O	P2 is an active high output indicating that a valid refresh address is available on the XA bus.

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POACH 2 Pin Description (Continued)

Pin No.	Symbol	Type	Description
38	-RDXDB	O	READ X-DATA BUS controls the direction of the bidirectional buffer between the least significant byte of the 'S' Data Bus and the 'X' Data Bus. -RDXDB is used in conjunction with +ACK to control XBUS activity. When +ACK is active and -RDXDB is low, data is to be read from the peripheral bus. When +ACK is active and -RDXDB is high, data is to be written to the peripheral bus.
22	REFRDY	O	REFRESH/IO-CHANNEL-READY is generated by +REFRESH OR'd with IOCHRDY. It is used by POACH 1 to preset the Clock Generator & Ready Interface Asynchronous Ready (ARDY).
41	-REFRESH	I/O	REFRESH is an active low output used to initiate a refresh cycle for the dynamic RAMs.
31	+RESET	I	RESET (SYSTEM) is an active high input from POACH 1. +RESET is used to force POACH 2, as well as the system, into an initial state. From POACH 1 Pin 55.
66	SPEAKER	O	SPEAKER DATA is an output of the Programmable interval timer tone signal used to drive the speaker.
32	SYSCLK	I	SYSTEM CLOCK input from POACH 1. It is used to synchronize POACH 2 to the system. From POACH 1 SYSCLK Pin.
62	T/C	O	TERMINAL COUNT provides a pulse when the terminal count for any DMA channel is reached.
11 53	Vcc1 Vcc2		POWER: +5-volt supply.
10 54	Vss1 Vss2		GROUND.
68 69	X1 X2	I O	CRYSTAL inputs for the internal oscillator used to generate clocking for I/O devices. A parallel resonant fundamental frequency mode crystal is required. An alternative oscillator may be connected to X1.
1-9 84 77-83	XA8-XA0 XA9 XA16-XA10	I/O I/O O	XBUS ADDRESSES 0-16 are the peripheral addresses for the local I/O bus.
12-19	XD0-XD7	I/O	Data Bus 0-7 for the peripheral bus. The direction of the bus is determined by the -RDXDB signal from POACH 2.

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POACH 2 Pin Description (Continued)

Pin No.	Symbol	Type	Description
44	-XMEMR	I/O	MEMORY READ signal indicating a DMA read operation from peripheral devices or memory.
45	-XMEMW	O	MEMORY WRITE signal indicating a DMA write operation to peripheral devices or memory. It is tri-stated except during DMA transfers.

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POACH 1/POACH 2

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ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias ..... 0°C to 70°C
Storage Temperature ..... -65°C to 150°C
Voltage on any pin with respect to ground ..... -0.5V to V_{CC} + 0.5V
Power Dissipation ..... 1 Watt

**Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

POACH/AT DC CHARACTERISTICS

(V_{CC} = 5V ± 5%, T_A = 0°C to 70°C)

Symbol	Parameter	Condition	Value			Units	Notes
			Min	Typ	Max		
INPUTS							
V_{IL1}	Input Low Voltage				0.5	V	1
V_{IH1}	Input High Voltage		2.0			V	1
V_{IL2}	Special Input Low Voltage				0.5	V	2
V_{IH2}	Special Input High Voltage		4.5			V	2
I_{IL1}	Input Low Current	V_{IN} = 0V	-100			μA	3
I_{IL2}	Special Input Low Current	V_{IN} = 0V	-10			μA	4
I_{IH}	Input High Current	V_{IN} = V_{CC}			10	μA	
OUTPUTS							
I_{OL1}	Output Low Current	V_{OL} = 0.45V	4	20		mA	5
I_{OL2}	Output Low Current	V_{OL} = 0.45V	16	35		mA	6
I_{OL3}	Open Drain Output Low Current	V_{OL} = 0.45V	18	36		mA	7
I_{OH}	Output High Current	V_{OH} = 2.4V		-20	-4	mA	8
I_{OZ}	Off State Current	V_O = 0 to V_{CC}	-10		10	μA	9

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POACH/AT DC CHARACTERISTICS (Continued)

(V_{CC} = 5V ± 5%, T_A = 0°C to 70°C)

Symbol	Parameter	Condition	Value			Units	Notes
			Min	Typ	Max		
SUPPLY							
I_{CC1}	POACH 1 Operating Supply Current	f_{SYSCLK} = 10MHz f_{SYSCLK} = 12MHz		28 32	55 60	mA mA	10
I_{STAT1}	POACH 1 Static Supply Current			60		µA	11
I_{BATT}	POACH 1 Battery Supply Current	V_{BATT} = 5V V_{BATT} = 2.8V		10	25 20	µA µA	12
V_{BATT}	POACH 1 Battery Supply Voltage		2.8			V	12
I_{CC2}	POACH 2 Operating Supply Current	f_{SYSCLK} = 10MHz f_{SYSCLK} = 12MHz		26 30	45 50	mA mA	13

Notes:

1. Includes all inputs, and I/O pin inputs except for POACH 1 pins $\overline{\text{POWERGOOD}}$, X3, CCRRST, CCROSC and POACH 2 pins X1, IOCHRDY and -REFRESH.
2. Special input pins include the crystal input pins and inputs needed for battery backup. On POACH 1 these signals are $\overline{\text{POWERGOOD}}$, X3, CCRRST and CCROSC. On POACH 2 they are signals X1, IOCHRDY and -REFRESH. Note that CCROSC is the only signal that should switch in the battery back up mode. For backup operation with $V_{BATT} < 4.75V$ CCROSC input levels V_{IL}/V_{IH} should be 10% and 90% of V_{BATT}, respectively.
3. All input pins include a high impedance pullup with the static protection network except for the special inputs $\overline{\text{POWERGOOD}}$, X3, CCROSC, CCRRST and X1. I/O pins do not have this pullup.
4. Includes pin $\overline{\text{POWERGOOD}}$, X3, CCROSC and CCRRST of POACH 1; and X1 of POACH 2.
5. Includes all outputs, and I/O pin outputs except for POACH 1 pins PROCCLK, SYSCLK, -IOR, -IOW, -MEMR, -MEMW, INTA, ALE, SA0, and POACH 2 pins -IOR, -IOW, OSC and -REFRESH.
6. Includes outputs PROCCLK, SYSCLK, -IOR, -IOW, -MEMR, -MEMW, INTA, ALE, SA0 of POACH 1 and -IOR, -IOW and OSC of POACH 2.
7. For the -REFRESH output of POACH 2.
8. Includes all outputs and I/O pin outputs except for -REFRESH of POACH 2.
9. For all 3-state and I/O pin outputs.
10. Includes I_{BATT} current with $V_{BATT} = V_{CC}$, and f_{CCROSC} = 32.768 KHz.
11. Inputs not switching at $V_{IN} = V_{CC}$, except f_{CCROSC} = 32.768 KHz. Includes I_{BATT} current with $V_{BATT} = V_{CC}$.
12. Tested with CCROSC input toggling at 32.768 KHz and CCRRST = V_{BATT}, all other inputs and V_{CC} supply pins open.
13. Tested with input X1 switching at 14.3181 MHz.

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POACH 1 AC CHARACTERISTICS

(V_{DD} = 5V ± 5%, T_A = 0°C to 70°C)

Symbol Figure	Parameter	10 MHz			12 MHz			Units	Notes
		Min	Typ	Max	Min	Typ	Max		
53-15	0WS Setup Time to PROCCLKI	30	26		30	22		ns	
54-15	0WS Hold Time from PROCCLKI	15	10		15	6		ns	
69-22	A0 Setup Time to ALE	30	18		25	11		ns	
	A0 Hold Time from ALE	0	0		0	0		ns	
26-6	A1 Setup Time to S1, S0	27	17		22	10		ns	
27-6	A1 Hold Time from S1, S0	0	0		0	0		ns	
43-13	A20 Delay from NA20		20	27		14	22	ns	
44-13	A20 Delay from A20GATE		30	37		24	32	ns	
45-13	A20 Disable Delay from CPUHLDAI			35			30	ns	4
46-13	A20 Enable Delay from CPUHLDAI			35			30	ns	
72-24	-AEN1, -AEN2 Setup Time to SYSCLKI		15			15		ns	
73-24	-AEN1, -AEN2 Hold Time from SYSCLKI		0			0		ns	
17-3	ALE Active Delay from PROCCLKI		18	25		16	23	ns	
18-3	ALE Inactive Delay from PROCCLKI		20	30		15	25	ns	
68-21	$\overline{\text{BUSY286}}$ Delay		25	35		20	35	ns	
	CCROSC High Time	25			25			µs	5
	CCROSC Low Time	25			25			µs	5
	CCROSC Input Rise/Fall Time			20			20	ns	
39-10,11	CCRR/W Setup Time to IOR/IOWI		0			0		ns	
40-10,11	CCRR/W Hold Time from IOR/IOWI		17			15		ns	
	CCRRST Pulse Width	100			83			ns	
67-20	CNTLOFF Delay from PROCCLKI		22	30		17	25	ns	
70-23	CPUHLDA Setup Time to PROCCLKI		20			18		ns	
71-23	CPUHLDA Hold Time from PROCCLKI		0			0		ns	
47-14	DIR245 Delay from -IOR, -IOW		12	17		6	15	ns	
49-14	DIR245 Delay from -MEMR, -MEMW		12	17		6	15	ns	
55-16	DT/R Delay High from PROCCLKI		35	45		29	40	ns	
56-16	DT/R Delay Low from PROCCLKI		30	45		22	40		
60-16	F16 Setup Time to PROCCLKI	30	15		30	12		ns	
61-16	F16 Hold Time from PROCCLKI	0	-5		0	-10		ns	

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POACH 1 AC CHARACTERISTICS (Continued)
(V_{DD} = 5V ± 5%, T_A = 0°C to 70°C)

Symbol -Figure	Parameter	10 MHz			12 MHz			Units	Notes
		Min	Typ	Max	Min	Typ	Max		
72-24	+FSYS16 Setup Time to SYSCLKI		15			15		ns	
73-24	+FSYS16 Hold Time from SYSCLKI		0			0		ns	
48-14	GATE245 Delay from -IOR, -IOW		15	22		11	20	ns	
50-14	GATE245 Delay from -MEMR, -MEMW		15	22		11	20	ns	
37-9	Interrupt Request Pulse Width	100			100			ns	8
29-7,8	-IOR, -IOW active delay from PROCCLKI			45			35	ns	
30-7,8	-IOR, -IOW inactive delay from PROCCLKI			45			35	ns	
	-IOR, -IOW enable/disable delay from PROCCLKI		35			35		ns	
	-INTA active delay from PROCCLKI			45			35	ns	
	-INTA inactive delay from PROCCLKI			45			35	ns	
	-INTA enable/disable delay from PROCCLKI		35			35		ns	
38-9	INTR Delay from Interrupt		95	175		67	150	ns	
33-7,8	-INTR1CS, -INTR2CS Setup Time to -IOR, -IOWI		0			0		ns	
34-7,8	-INTR1CS, -INTR2CS Hold Time from -IOR, -IOWI		0			0		ns	
72-24	-IO CS 16 Setup Time to SYSCLKI	85			75			ns	
73-24	-IO CS 16 Hold Time from SYSCLKI	0			0			ns	
57-16	LSDEN, MSDEN Active Delay from PROCCLKI		28	45		23	40	ns	
58-16	LSDEN, MSDEN Inactive Delay from PROCCLKI		25	35		20	30	ns	
66-19	LSDEN, MSDEN Delay from -NPCS		10			10		ns	
84-16	-MEMR, -MEMW active delay from PROCCLKI	5		45	5		35	ns	
85-16	-MEMR, -MEMW inactive delay from PROCCLKI	5		45	5		35	ns	
	-MEMR, -MEMW enable/disable delay from PROCCLKI		35			35		ns	
64-17	MSDEN Delay from XHBE		19	27		16	25	ns	
62-16	M/$\overline{IO}$ Setup Time to PROCCLKI	28	20		25	17		ns	
63-16	M/$\overline{IO}$ Hold Time from PROCCLKI	0	-10		0	-15		ns	

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POACH 1 AC CHARACTERISTICS (Continued)
(V_{DD} = 5V ± 5%, T_A = 0°C to 70°C)

Symbol -Figure	Parameter	10 MHz			12 MHz			Units	Notes
		Min	Typ	Max	Min	Typ	Max		
65-18	-NPCS Delay		30	40		26	35	ns	
11-2	PCLK, -PCLK High Time	45			35			ns	
12-2	PCLK, -PCLK Low Time	45			35			ns	
13-2	PCLK, -PCLK Delay from PROCCLK			45			40	ns	
14-2	PCLK, -PCLK Rise/Fall times			7.5			5	ns	
19-4	$\overline{\text{POWER GOOD}}$ Setup Time to PROCCLKI	26			26			ns	3
	$\overline{\text{POWER GOOD}}$ Hold Time from PROCCLKI	50			41			ns	3
8-4	$\overline{\text{POWER GOOD}}$ Rise/Fall Times			20			20	ns	
5-2	PROCCLK Delay from X3			40			35	ns	
6-2	PROCCLK High Time	16			13			ns	
7-2	PROCCLK Low Time	12			11			ns	
9-2	PROCCLK Rise/Fall Times			8			8	ns	
22-5	RC Setup Time to SYSCLKI		30			30		ns	3
23-5	RC Pulse Width	100	20		83	15		ns	
51-15	$\overline{\text{READY}}$ Active Delay from PROCCLKI		20	22		14	18	ns	
52-15	$\overline{\text{READY}}$ Inactive Delay		20	70		15	60	ns	
	REFRDY Pulse Width	50			40			ns	
74-25	RES 287 Delay		20	60		8	50	ns	
21-4	RES CPU Delay from SYSCLKI		35	60		30	50	ns	
20-4	+RESET Delay from PROCCLKI		30	50		30	50	ns	
41-12	SA0 Enable Time from CPU HLDA			60			50	ns	
42-12	SA0 Disable Time from CPU HLDA			60			50	ns	4
15-3	S1, S0 Setup Time to PROCCLKI	28	21		22	17		ns	
16-3	S1, S0 Hold Time from PROCCLKI	0	-5		0	-11		ns	
10-2	SYSCLK Delay from PROCCLKI		25	30		15	25	ns	
1-2	X3 Period	50			41.6			ns	
2-2	X3 Low Time	17			15			ns	
3-2	X3 High Time	23			20			ns	
4-2	X3 Rise/Fall Times			5			3	ns	
35-8,11	XD0-XD7 Delay Time from -IORI			45			40	ns	
36-8,11	XD0-XD7 Hold Time from -IORI			17			15	ns	
31-7	XD0-XD7 Setup Time to -IOWI	100			83			ns	
32-7	XD0-XD7 Hold Time from -IOWI	0			0			ns	

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POACH 2 AC CHARACTERISTICS

(V_{DD} = 5V ± 5%, T_A = 0°C to 70°C)

Symbol -Figure	Parameter	10 MHz			12 MHz			Units	Notes
		Min	Typ	Max	Min	Typ	Max		
96-27	-8042CS delay from XA_X		50	60		40	48	ns	
98-28	A17-A23 delay from SYSCLK↑			150			125	ns	
99-28	A17-A23 enable delay from HLDA or -MASTER			100			83	ns	
97-28	A17-A23 disable delay from HLDA or -MASTER			100			83	ns	4
100-29	+ACK delay from HLDA		36	45		30	40	ns	
101-29	+ACK delay from -MASTER		36	45		31	40	ns	
109-30	-AEN1, -AEN2 delay from SYSCLK↑		90	130		75	115	ns	
94-27	CCRR/W delay from XA_X			60			48	ns	
102-29	CCRR/W delay from HLDA or -MASTER			50			41	ns	
108-30,39	CPU HRQ delay from SYSCLK↑		62	80		52	70	ns	
95-26	-CS287 delay from XA_X			60			48	ns	
103-29	-CS287 delay from HLDA or -MASTER			50			41	ns	
113-30	-DACK0-3, -DACK5-7 delay from SYSCLK↑		76	110		63	100	ns	
110-30	-DMAAEN delay from SYSCLK↑		98	140		75	120	ns	
	-DMAAEN delay from -MASTER							ns	
132-32	-DPCK setup time to -XMEMR↑	8			6			ns	
133-32	-DPCK hold time from -XMEMR↑	5			5			ns	
107-30	-DRQ0-3, -DRQ5-7 setup time to SYSCLK↑		-15	0		-18	0	ns	3,7
	HLDA setup time to SYSCLK↑	70	45		65	12		ns	
	HLDA hold time from SYSCLK↑	0	0		0	0		ns	
28-7	-INTR1CS, -INTR2CS delay from XA_X		38	60		32	41	ns	
104-29	-INTR1CS, -INTR2CS delay from HLDA or -MASTER		38	60		32	41	ns	
134-33	-IOCHCK pulse width		25			20		ns	
	IOCHRDY setup time to SYSCLK↑ (during refresh)	25	5		25	1		ns	
	IOCHRDY hold time to SYSCLK↑ (during refresh)	25	10		25	6		ns	

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POACH 2 AC CHARACTERISTICS (Continued)
(V_{DD} = 5V ± 5%, T_A = 0°C to 70°C)

Symbol -Figure	Parameter	10 MHz			12 MHz			Units	Notes
		Min	Typ	Max	Min	Typ	Max		
114-30	-IOR, -IOW active delay from SYSCLK↑ (during DMA transfers)		87	125		73	100	ns	
115-30	-IOR, -IOW inactive delay from SYSCLK↑ (during DMA transfers)		94	115		78	100	ns	
116-30	-IOR, -IOW float to inactive delay from SYSCLK↑ (during DMA transfers)		100	120		80	100	ns	
117-30	-IOR, -IOW inactive to float delay from SYSCLK↑ (during DMA transfers)		140	170		130	156	ns	4
152-37	-IOW active pulse width (during CPU transfers)	90			75			ns	
137-34	IRQ0 delay from X1		48			42		ns	
	NMI delay from -XMEMR↑		50	100		37	83	ns	
135-33	NMI delay from -IOCHCK↑		50	100		40	83	ns	
143-35	OSC low time	20			20			ns	
144-35	OSC high time	20			20			ns	
145-35	OSC rise/fall times			15			15	ns	
146-35	OSC delay from X1			30			24	ns	
	P2 delay from SYSCLK↑		30			25		ns	
148-36	-RDXDB inactive delay from -IOR		55	100		30	83	ns	
149-36	-RDXDB delay from -INTA		55			45		ns	
	REFRDY delay from IOCHRDY		31	50		25	41	ns	
157-39	-REFRESH delay from HLDA		17	28		15	24	ns	
158-39	-REFRESH delay from SYSCLK↑		52	100		45	83	ns	
	+RESET active pulse width	200			160			ns	
138-34	SPEAKER delay from X1		46			43		ns	
91-26	SYSCLK period	100			83			ns	
92-26	SYSCLK low time	40	25		30	13		ns	
93-26	SYSCLK high time	40	20		30	10		ns	
124-30	TC delay from SYSCLK↑		90	110		73	100	ns	
140-35	X1 low time	30			30			ns	
141-35	X1 high time	30			30			ns	
142-35	X1 rise/fall times			5			5	ns	

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POACH 2 AC CHARACTERISTICS (Continued)

(V_{DD} = 5V ± 5%, T_A = 0°C to 70°C)

Symbol -Figure	Parameter	10 MHz Min	10 MHz Typ	10 MHz Max	12 MHz Min	12 MHz Typ	12 MHz Max	Units	Notes
150-37	XA_X input setup time to -IOW↑ (during CPU transfers to POACH 2)	100	0		83	0		ns	
151-37	XA_X input hold time from -IOW↑ (during CPU transfers to POACH 2)	45	28		40	20		ns	
	XA_X output hold time from -IOR↑ (during CPU transfers from POACH 2)	100	40		67	20		ns	
111-30	XA_X valid delay from SYSCLK↑ (during DMA transfers)		120	160		81	150	ns	
159-30	XA_X valid delay from SYSCLK↑ (during REFRESH)		48	90		40	75	ns	
112-30	XA_X disable delay from SYSCLK↑ (during DMA transfers)		85	150		70	130	ns	4
153-37	XD_X input setup time to -IOW↑	100	50		83	20		ns	
153-37	XD_X input hold time from -IOW↑	17	10		15	0		ns	
155-38	XD_X output delay from -IOR↓		100	125		84	100	ns	
156-38	XD_X output hold time from -IOR↑	17	40	70	15	35	60	ns	
125-31	-XMEMR active delay from SYSCLK↑		80	110		65	100	ns	
126-31	-XMEMR inactive delay from SYSCLK↑		85	110		72	100	ns	
127-31	-XMEMR enable/disable delay from SYSCLK↑		120			120		ns	4
121-30	-XMEMW active delay from SYSCLK↑		60	110		42	100	ns	
122-30	-XMEMW inactive delay from SYSCLK↑		88	110		75	100	ns	
123-30	-XMEMW enable/disable delay from SYSCLK↑		120			120		ns	4

Notes:

1. To provide clearly understood information, the complex timing diagrams depict operation in a standard IBM PC AT system design. Combinational logic data paths are shown with less complex timing diagrams. The signal source (POACH, PROCESSOR, LOGIC, etc.) follows the signal name.
2. Typical AC specification values are given for V_{CC} = 5V and T_A = 27°C.
3. This signal is an asynchronous input. The timing specification is provided for testing purposes only to assure recognition at a specific clock edge.
4. The output float or high impedance condition occurs when output current is less than I_{OZ} in magnitude.
5. The frequency of CCROSC sets the count rate for the real time clock. CCROSC frequency, accuracy and stability, should be maintained as close as possible to 32.768Hz to insure the validity of time and date information.
6. Input rise and fall times are assumed to be less than 20ns unless otherwise specified.
7. DRQ_X must be held active with $DACK_X$ is returned.
8. The interupt request inputs include IRQ0, IRQ3-7, IRQ9-12, IRQ14-15, and +OPT.
9. Address XA_{0-15} are output for byte DMA operations. XA_{0-16} are output for word DMA operations, with XA0 low.
10. A minimum of 16 PROCCLK cycles must occur before POWERGOOD becomes valid.

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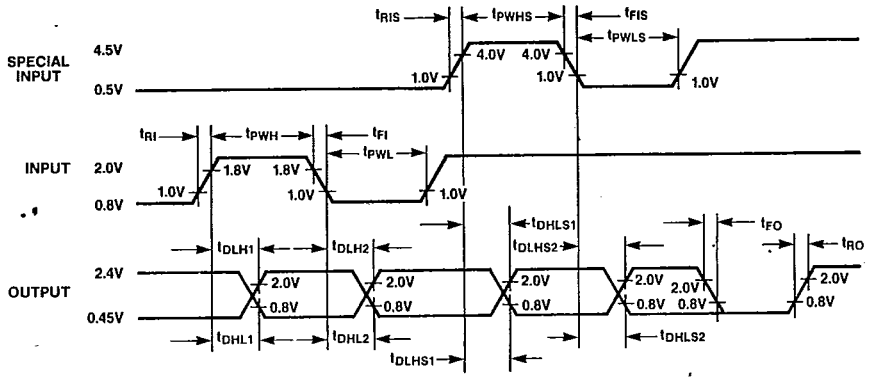

Figure 1A. Delay Time and Pulse Width Measurements

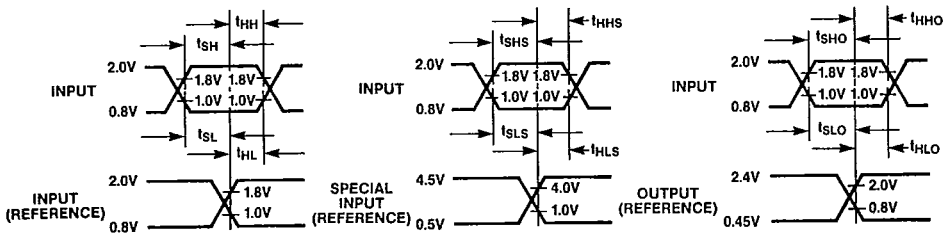

Figure 1B. Setup/Hold Time Measurements

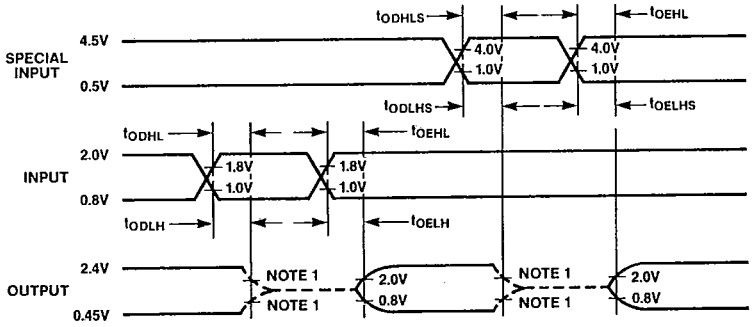

Figure 1C. Output Enable/Disable Time Measurement

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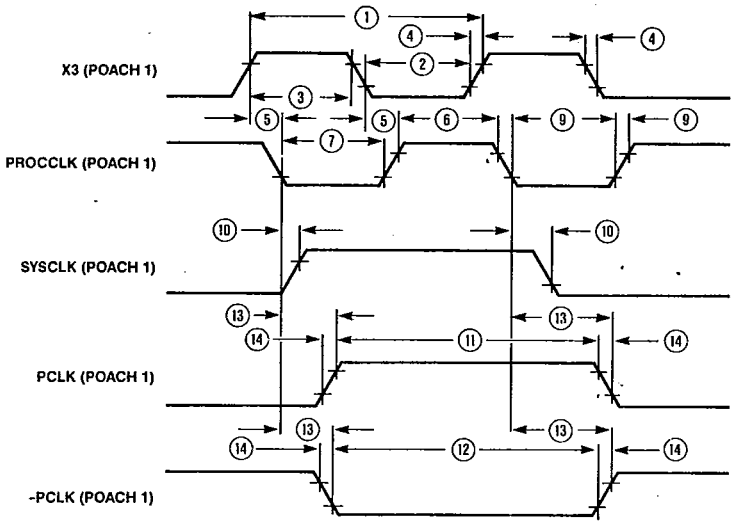

Figure 2. POACH 1 Clock Timing

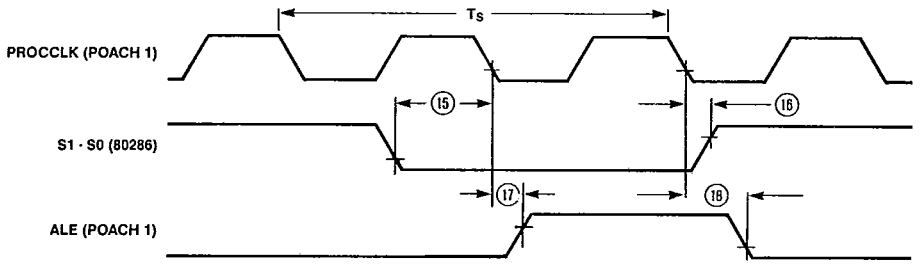

Figure 3. POACH 1 Status and ALE Timing

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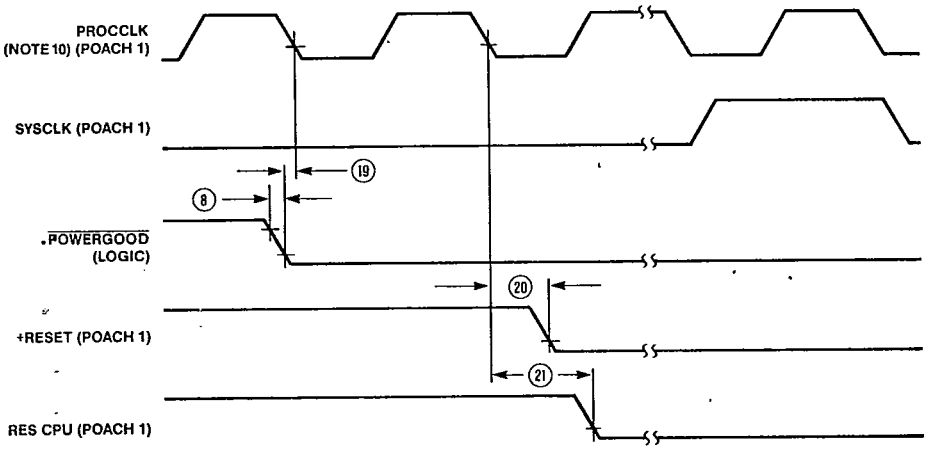

Figure 4. POACH 1 Power on Initiated Reset

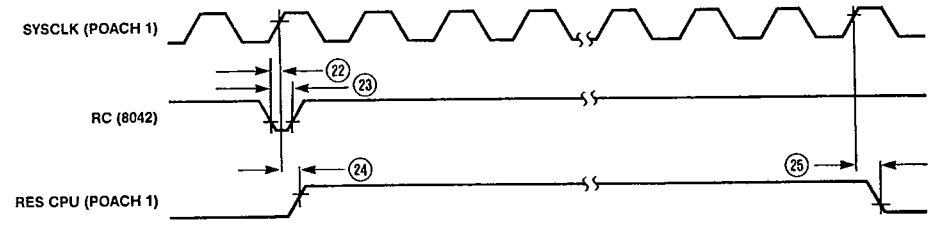

Figure 5. POACH 1 Keyboard Initiated Reset

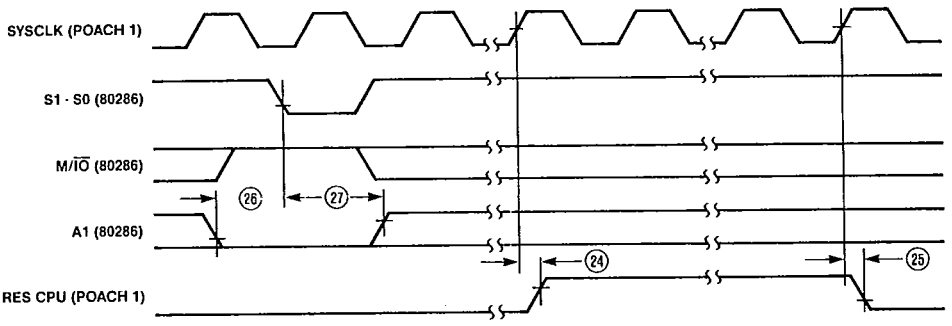

Figure 6. POACH 1 Processor Shutdown Initiated Reset

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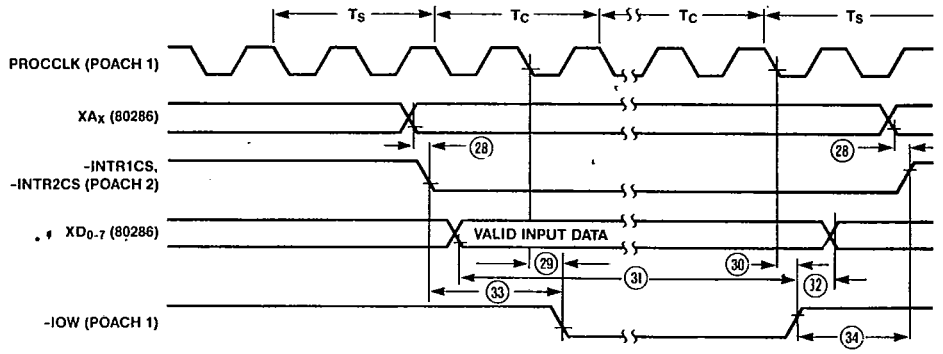

Figure 7. POACH 1 8254 Bus Write Timing

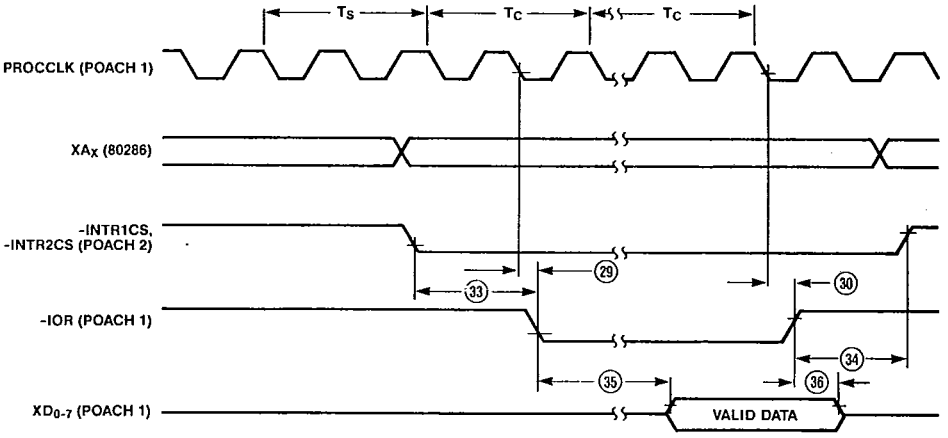

Figure 8. POACH 1 8254 Bus Read Timing

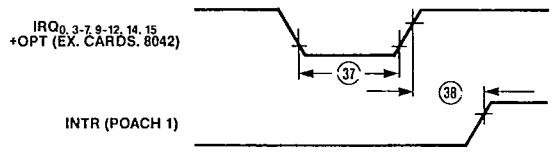

Figure 9. Interrupt Request Timing

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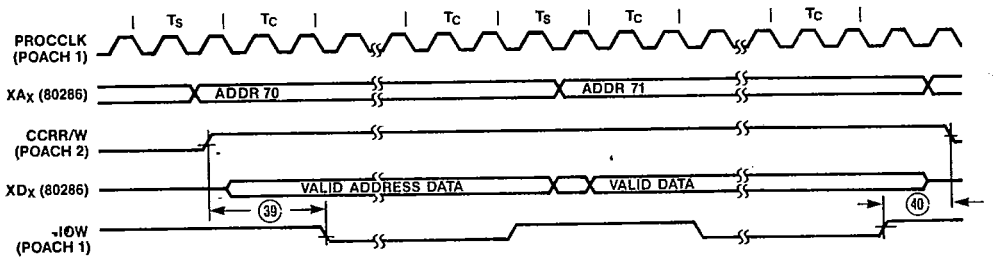

Figure 10. POACH 1 6818 Write Cycle

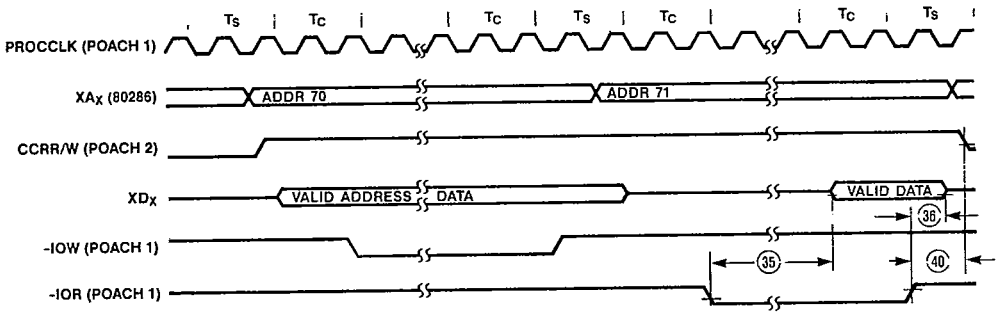

Figure 11. POACH 1 6818 Read Cycle

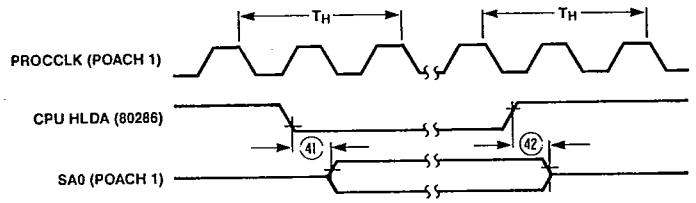

Figure 12. POACH 1 SA0 Timing

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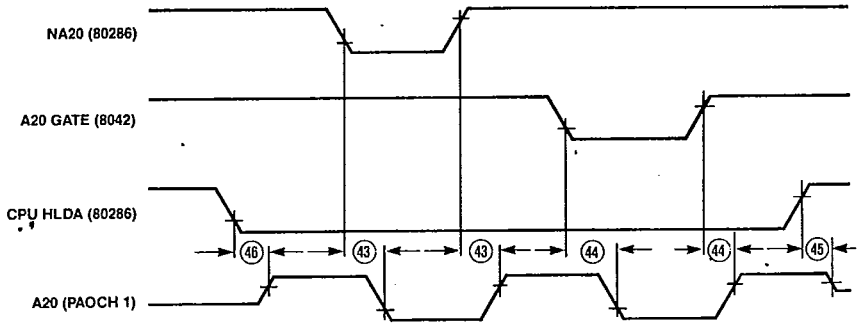

Figure 13. POACH 1 A20 Timing

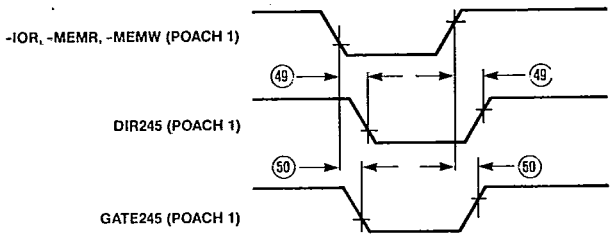

Figure 14. POACH 1 DIR245, GATE245 Timing

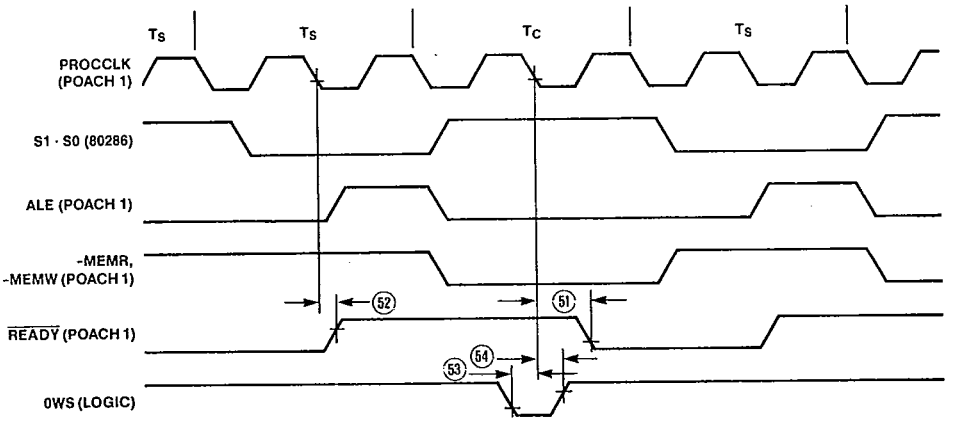

Figure 15. POACH 1 Zero Wait State Timing

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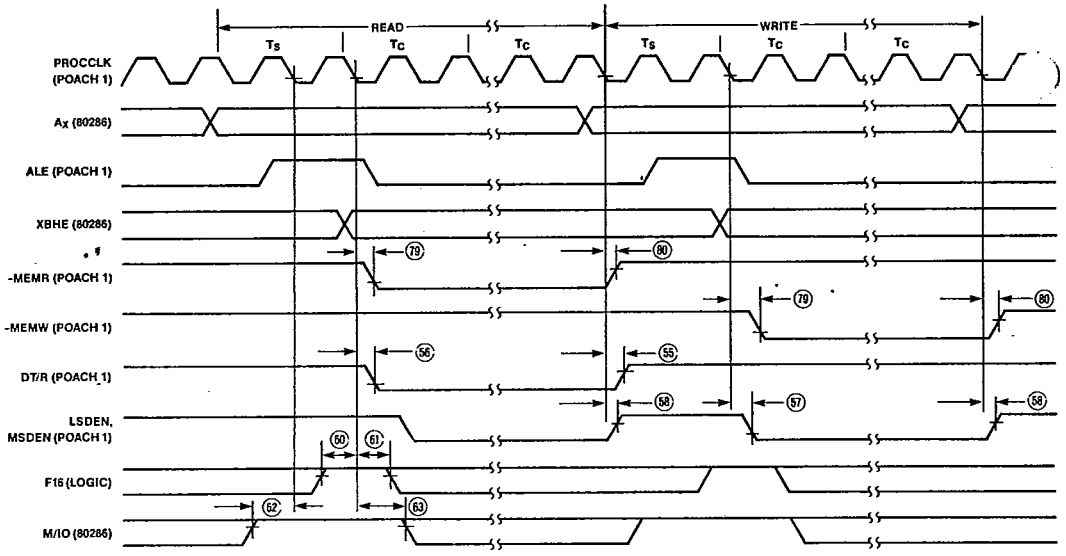

Figure 16. Memory Read/Write Cycles

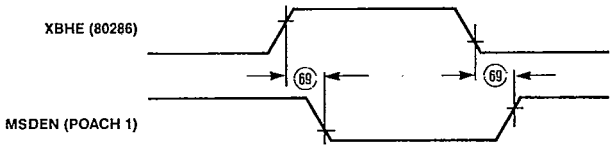

Figure 17. POACH 1 XHBE Timing

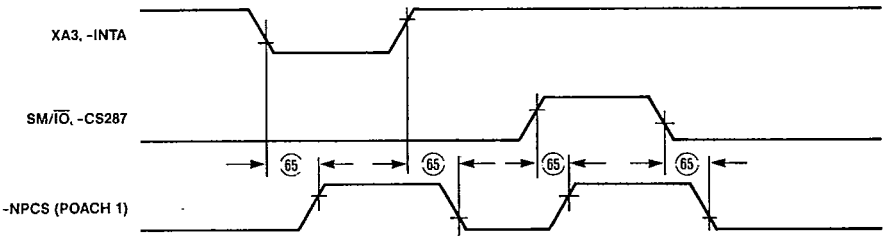

Figure 18. POACH 1 NPCS Timing

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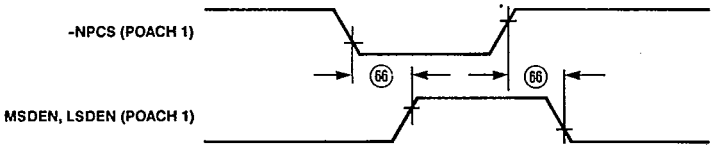

Figure 19. POACH 1 MSDEN, LSDEN Timing

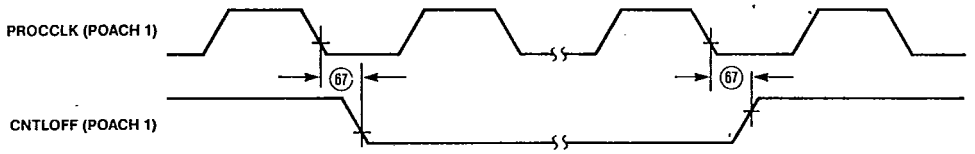

Figure 20. CNTLOFF Timing

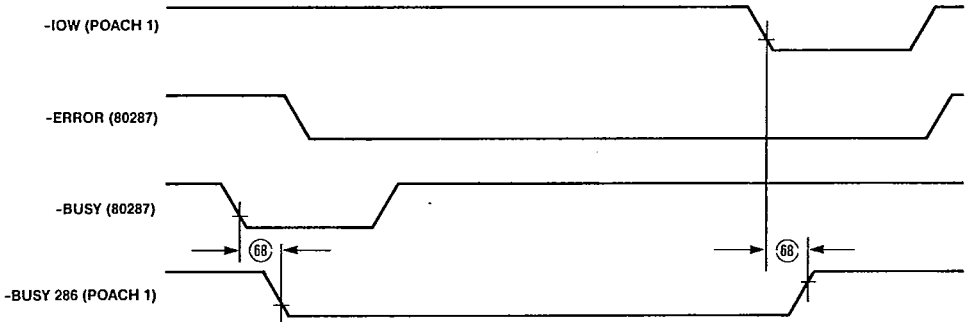

Figure 21. -BUSY286 Timing

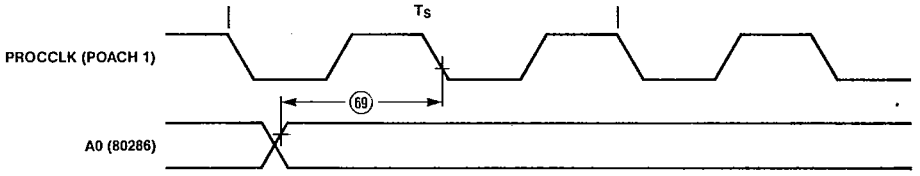

Figure 22. POACH 1 A0 Timing

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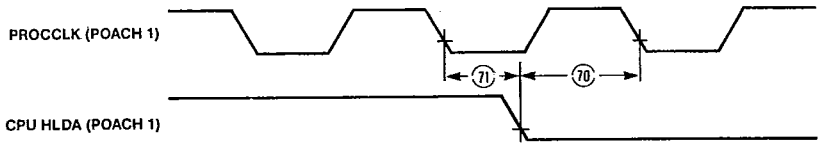

Figure 23. POACH 1 CPU HLDA Timing

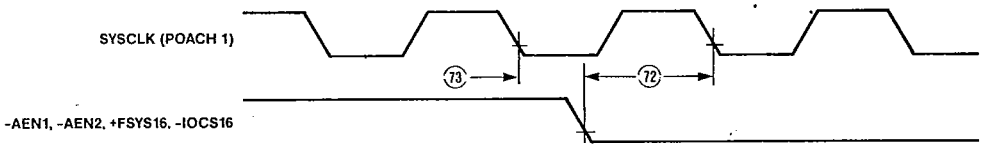

Figure 24. Bus Control Signal Timing

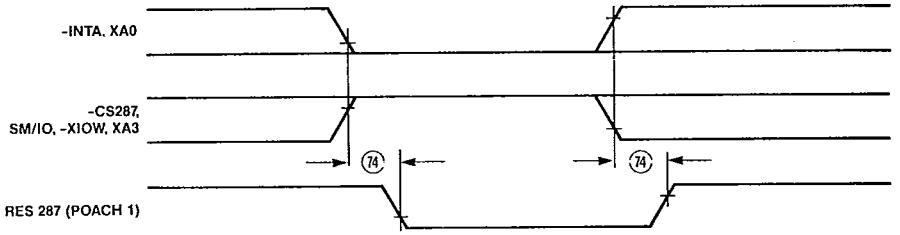

Figure 25. RES 287 Timing

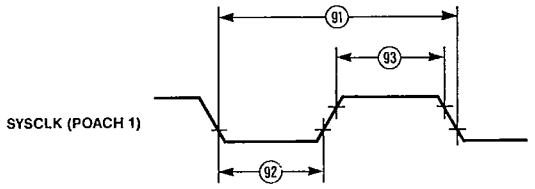

Figure 26. POACH 2 SYSCLK Timing

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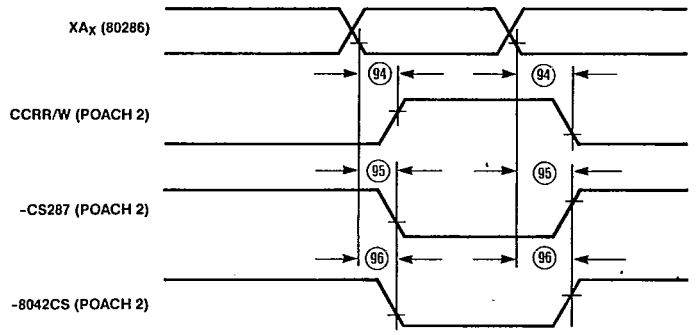

Figure 27. POACH 2 CCRR/W and CS287 Timing

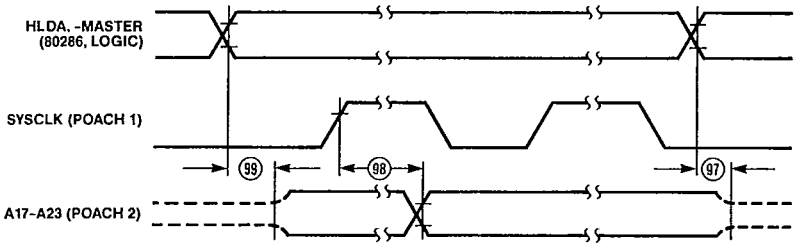

Figure 28. POACH 2 A18 to A23 Timing

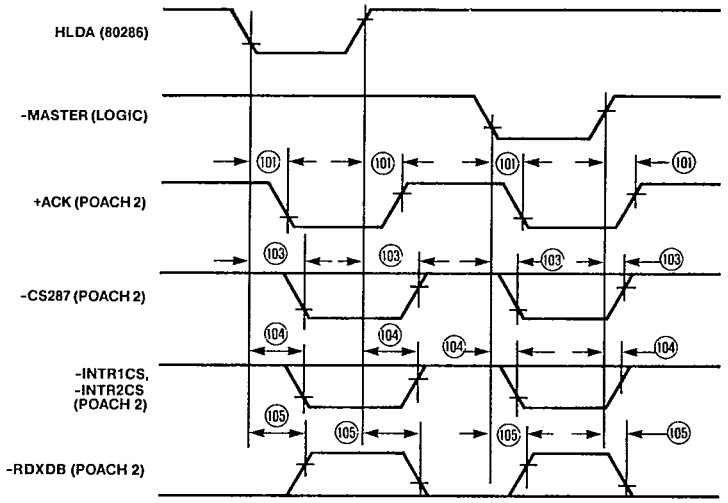

Figure 29. POACH 2 HLDA & -MASTER Timing

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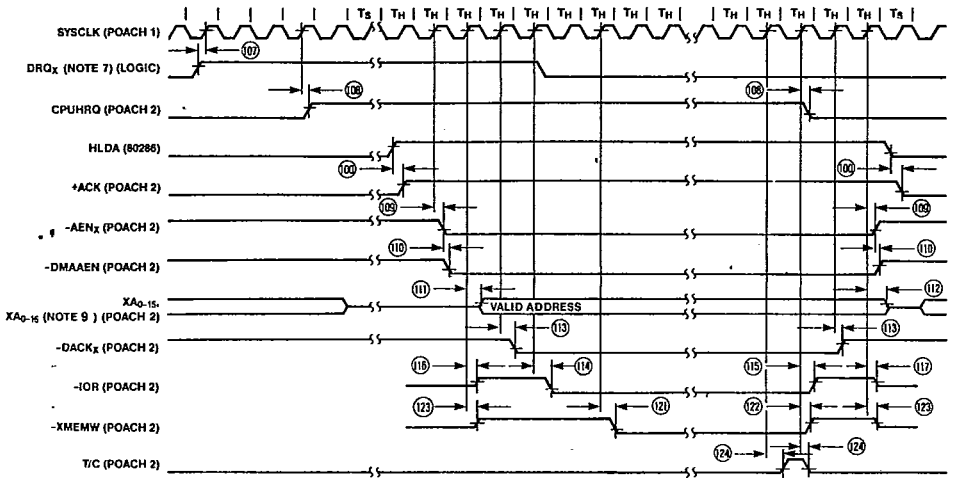

Figure 30. POACH 2 DMA I/O Read Timing (Single Transfer Shown)

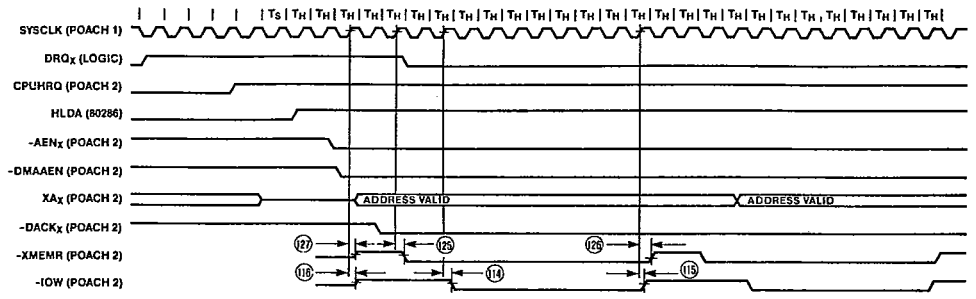

Figure 31. POACH 2 DMA I/O Write Timing (Block Transfer Shown)

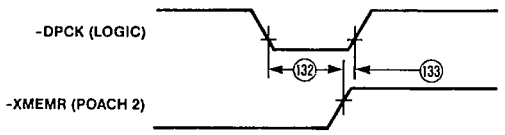

Figure 32. POACH 2 DPCK Timing

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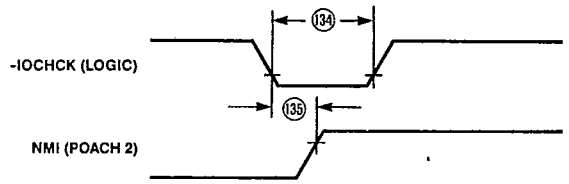

Figure 33. POACH 2 IOCHCK and NMI Timing

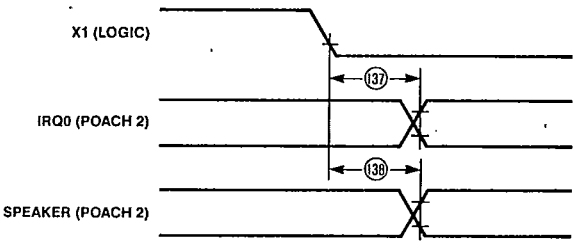

Figure 34. POACH 2 IRQ0 and SPEAKER Timing

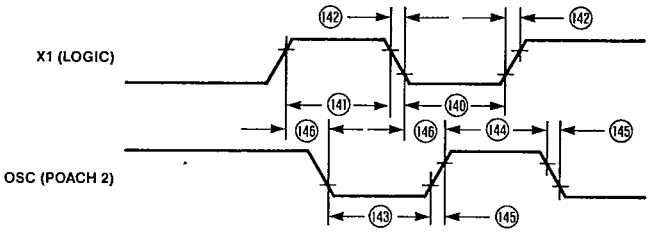

Figure 35. X1 and OSC Timing

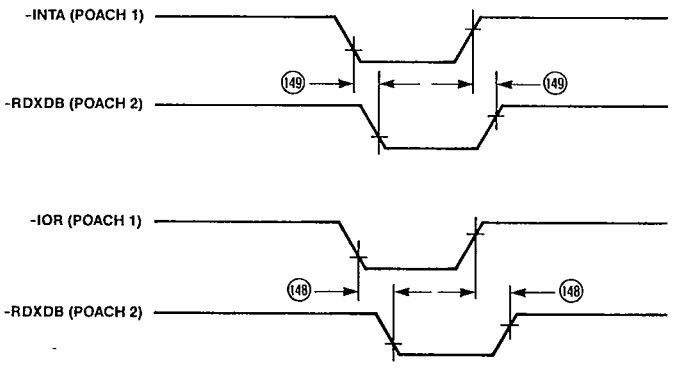

Figure 36. POACH 2 RDXDB Timing

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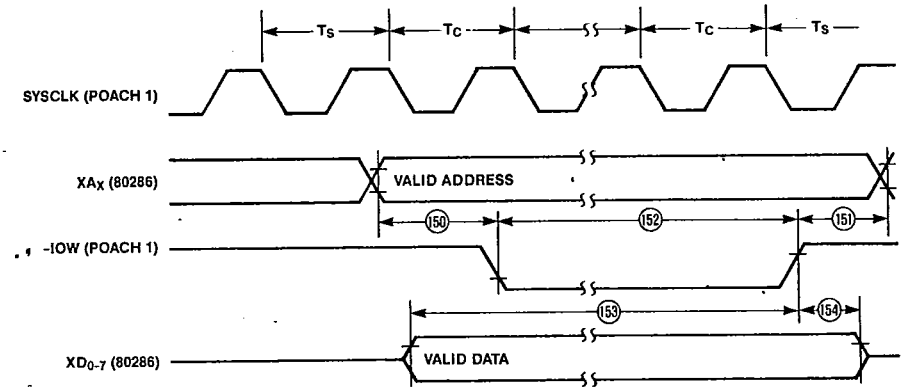

Figure 37. POACH 2 CPU Write Timing

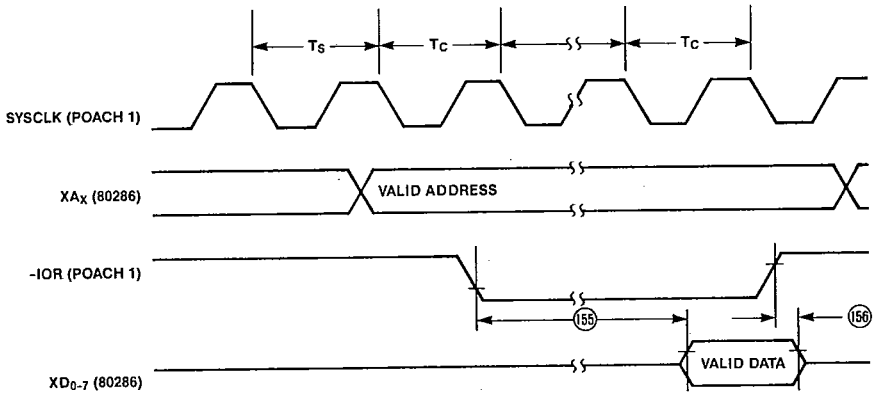

Figure 38. POACH 2 CPU Read Timing

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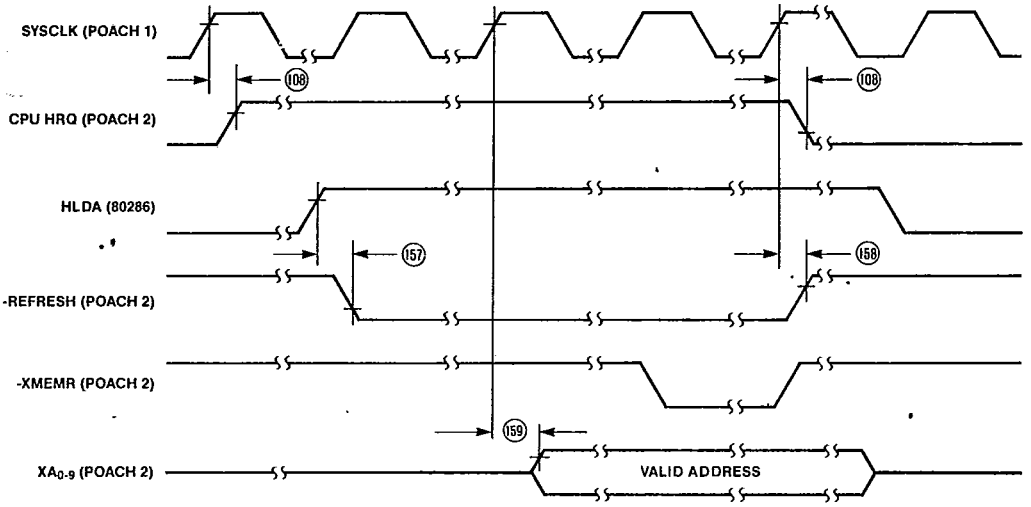
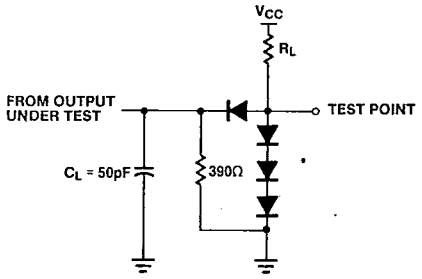
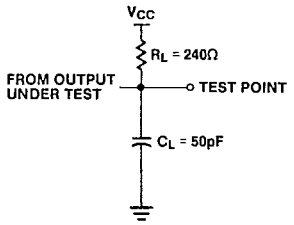


Figure 39. POACH 2 REFRESH Timing

TEST LOADS



Output Load Circuit



Load Circuit for Open-Collector Output

R_L = 620 ohms for all outputs except the following.

R_L = 220 ohms for:

POACH 1 pins	PROCCLK	-MEMR
	-IOR	-MEMW
	-IOW	INTA
	SA0	ALE
	SYSCLK	
POACH 2 pins	-IOR	OSC
	-IOW	

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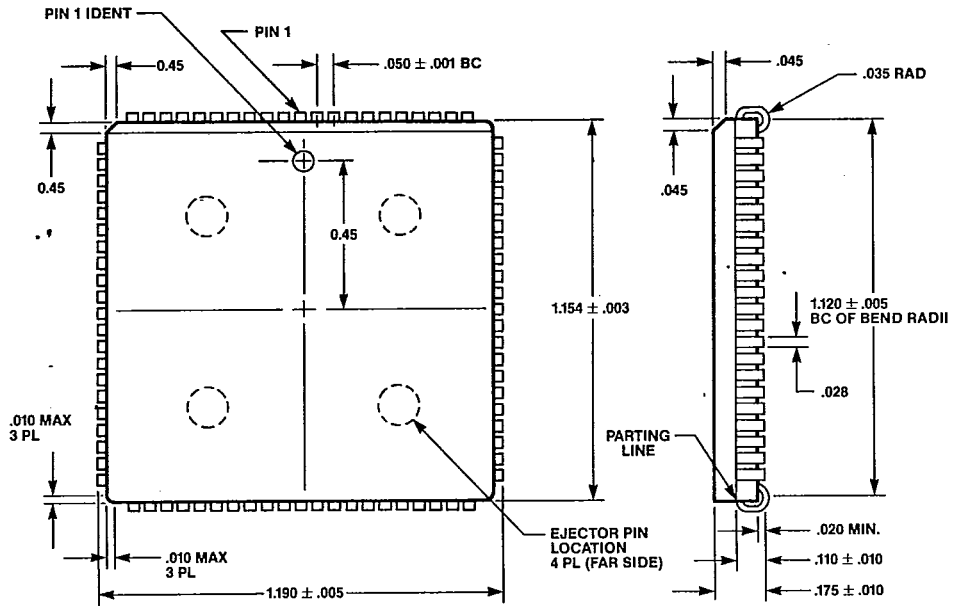
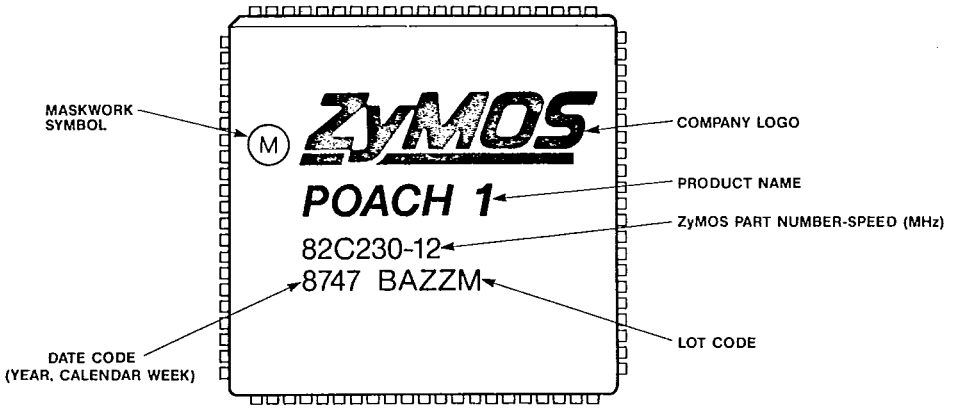
POACH 1/POACH 2



84L PLCC PACKAGE DIMENSIONS



MARKING DETAILS

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