



# Am27X020

2 Megabit (262,144 x 8-Bit) CMOS ExpressROM Device

## DISTINCTIVE CHARACTERISTICS

- **As an OTP EPROM alternative:**
  - Factory optimized programming
  - Fully tested and guaranteed
- **As a Mask ROM alternative:**
  - Shorter leadtime
  - Lower volume per code
- **Fast access time**
  - 75 ns
- **Single +5 V power supply**
- **Compatible with JEDEC-approved EPROM pinout**
- **±10% power supply tolerance**
- **High noise immunity**
- **Low power dissipation**
  - 100  $\mu$ A maximum CMOS standby current
- **Available in Plastic Dual In-Line Package (PDIP), Plastic Leaded Chip Carrier (PLCC), and Thin Small Outline Package (TSOP)**
- **Latch-up protected to 100 mA from -1 V to  $V_{CC} + 1$  V**
- **Versatile features for simple interfacing**
  - Both CMOS and TTL input/output compatibility
  - Two line control functions

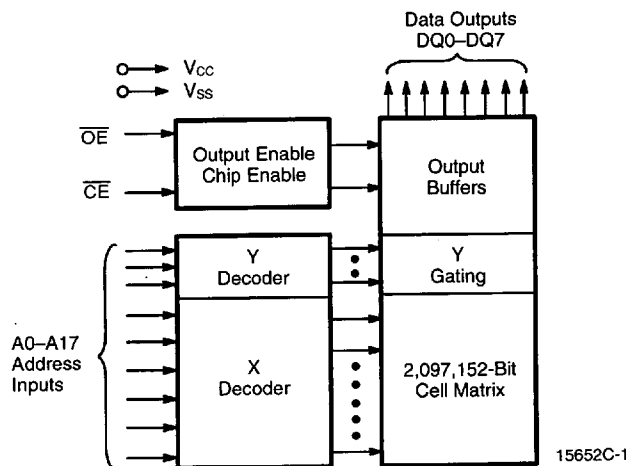
## GENERAL DESCRIPTION

The Am27X020 is a factory programmed and tested OTP EPROM. It is programmed after packaging prior to final test. Every device is rigorously tested under AC and DC operating conditions to your stable code. It is organized as 262,144 by 8 bits and is available in plastic dual in-line (PDIP), plastic leaded chip carrier (PLCC), and thin small outline (TSOP) packages. ExpressROM devices provide a board-ready memory solution for medium to high volume codes with short leadtimes. This offers manufacturers a cost-effective and flexible alternative to OTP EPROMs and mask programmed ROMs.

Access times as fast as 75 ns allow operation with high-performance microprocessors with reduced WAIT states. The Am27X020 offers separate Output Enable ( $\overline{OE}$ ) and Chip Enable ( $\overline{CE}$ ) controls, thus eliminating bus contention in a multiple bus microprocessor system.

AMD's CMOS process technology provides high speed, low power, and high noise immunity. Typical power consumption is only 100 mW in active mode, and 100  $\mu$ W in standby mode.

## BLOCK DIAGRAM

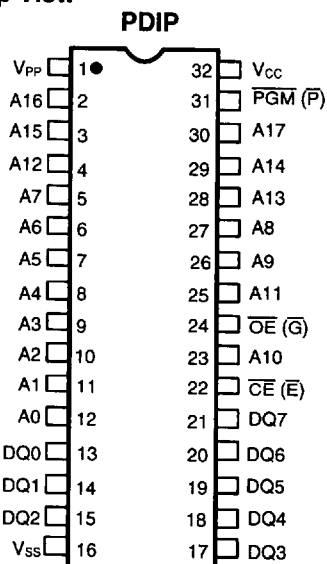


# PRODUCT SELECTOR GUIDE

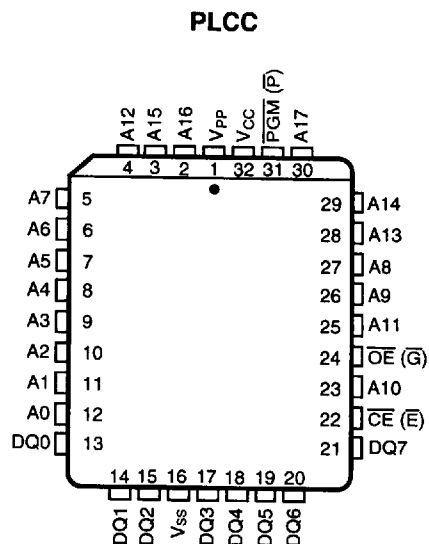
Family Part No.	Am27X020					
Ordering Part No:						
V <sub>CC</sub> ±5%						-255
V <sub>CC</sub> ±10%	-75	-90	-120	-150	-200	
Max Access Time (ns)	70	90	120	150	200	250
$\overline{CE}$ ( $\overline{E}$ ) Access (ns)	70	90	120	150	200	250
$\overline{OE}$ ( $\overline{G}$ ) Access (ns)	40	50	50	65	75	100

## CONNECTION DIAGRAMS

### Top View



15652C-2

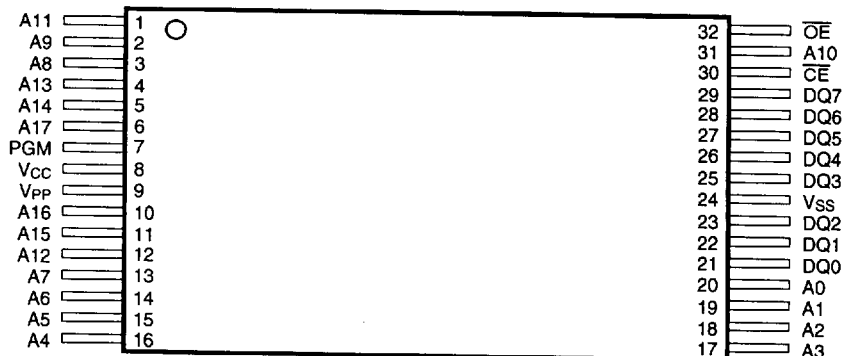


15652C-3

### Note:

1. JEDEC nomenclature is in parentheses.

### TSOP\*



### Standard Pinout

15652C-4

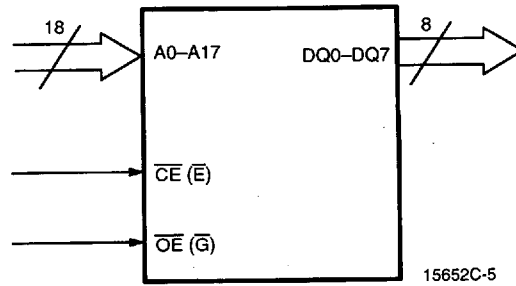
\*Contact local AMD sales office for package availability



## PIN DESIGNATIONS

A0-A17	= Address Inputs
$\overline{CE}$ ( $\overline{E}$ )	= Chip Enable Input
DQ0-DQ7	= Data Inputs/Outputs
DU	= No External Connection (Do Not Use)
NC	= No Internal Connection
$\overline{OE}$ ( $\overline{G}$ )	= Output Enable Input
$\overline{PGM}$ ( $\overline{P}$ )	= Program Enable Input
V <sub>CC</sub>	= V <sub>CC</sub> Supply Voltage
V <sub>PP</sub>	= Program Voltage Input
V <sub>SS</sub>	= Ground

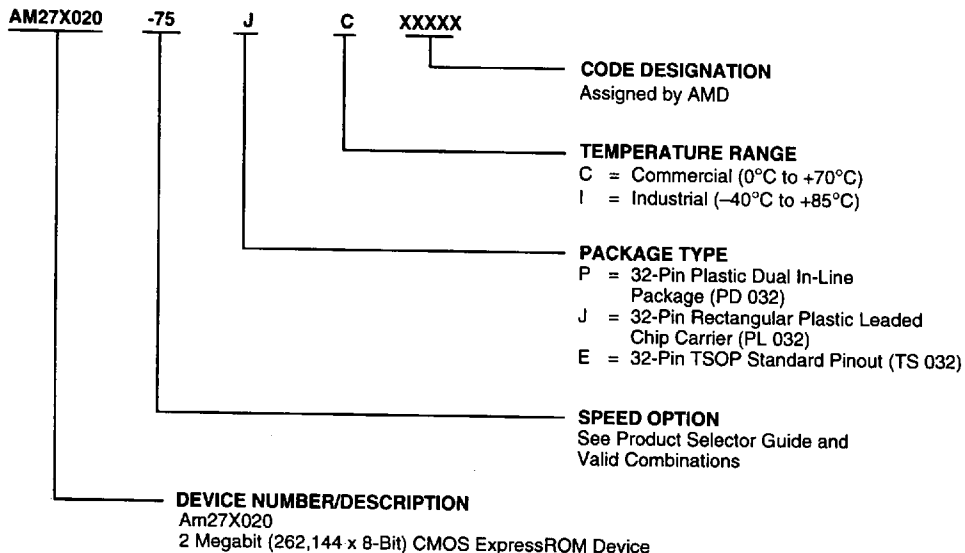
## LOGIC SYMBOL



## ORDERING INFORMATION

### Standard Products

AMD standard products are available in several packages and operating ranges. The ordering number (Valid Combination) is formed by a combination of:



Valid Combinations	
AM27X020-75	PC, JC, PI, JI, EC, EI
AM27X020-90	
AM27X020-120	
AM27X020-150	
AM27X020-200	
AM27X020-255	

#### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

## FUNCTIONAL DESCRIPTION

### Read Mode

The Am27X020 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ( $\overline{CE}$ ) is the power control and should be used for device selection. Output Enable ( $\overline{OE}$ ) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time ( $t_{ACC}$ ) is equal to the delay from  $\overline{CE}$  to output ( $t_{CE}$ ). Data is available at the outputs  $t_{OE}$  after the falling edge of  $\overline{OE}$ , assuming that  $\overline{CE}$  has been LOW and addresses have been stable for at least  $t_{ACC}-t_{OE}$ .

### Standby Mode

The Am27X020 has a CMOS standby mode which reduces the maximum  $V_{CC}$  current to 100  $\mu$ A. It is placed in CMOS-standby when  $\overline{CE}$  is at  $V_{CC} \pm 0.3$  V. The Am27X020 also has a TTL-standby mode which reduces the maximum  $V_{CC}$  current to 1.0 mA. It is placed in TTL-standby when  $\overline{CE}$  is at  $V_{IH}$ . When in standby mode, the outputs are in a high-impedance state, independent of the  $\overline{OE}$  input.

### Output OR-Tieing

To accommodate multiple memory connections, a two-line control function is provided to allow for:

- Low memory power dissipation
- Assurance that output bus contention will not occur

It is recommended that  $\overline{CE}$  be decoded and used as the primary device-selecting function, while  $\overline{OE}$  be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

### System Applications

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. At a minimum, a 0.1  $\mu$ F ceramic capacitor (high frequency, low inherent inductance) should be used on each device between  $V_{CC}$  and  $V_{SS}$  to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit board traces on ExpressROM device arrays, a 4.7  $\mu$ F bulk electrolytic capacitor should be used between  $V_{CC}$  and  $V_{SS}$  for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

## MODE SELECT TABLE

Mode	Pins	$\overline{CE}$	$\overline{OE}$	PGM	$V_{PP}$	Outputs
Read		$V_{IL}$	$V_{IL}$	X	X	DOUT
Output Disable		X	$V_{IH}$	X	X	Hi-Z
Standby (TTL)		$V_{IH}$	X	X	X	Hi-Z
Standby (CMOS)		$V_{CC} \pm 0.3$ V	X	X	X	Hi-Z

#### Note:

1. X = Either  $V_{IH}$  or  $V_{IL}$

**ABSOLUTE MAXIMUM RATINGS**

Storage Temperature	
OTP Products	−65°C to +125°C
All Other Products	−65°C to +150°C
Ambient Temperature	
with Power Applied	−55°C to +125°C
Voltage with Respect to $V_{SS}$	
All pins except $V_{CC}$	−0.6 V to $V_{CC} + 0.6$ V
$V_{CC}$	−0.6 V to +7.0 V

**Note:**

1. Minimum DC voltage on input or I/O pins is −0.5 V. During transitions, the inputs may overshoot  $V_{SS}$  to −2.0 V for periods of up to 20 ns. Maximum DC voltage on input and I/O pins is  $V_{CC} + 0.5$  V which may overshoot to  $V_{CC} + 2.0$  V for periods up to 20 ns.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

**OPERATING RANGES****Commercial (C) Devices**

Ambient Temperature ( $T_A$ ) . . . . . 0°C to +70°C

**Industrial (I) Devices**

Ambient Temperature ( $T_A$ ) . . . . . −40°C to +85°C

**Supply Read Voltages**

$V_{CC}$  for Am27X020-XX5 . . . . . +4.75 V to +5.25 V

$V_{CC}$  for Am27X020-XX0 . . . . . +4.50 V to +5.50 V

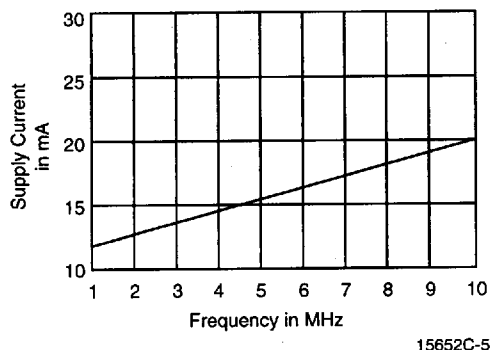
Operating ranges define those limits between which the functionality of the device is guaranteed.

# DC CHARACTERISTICS over operating range unless otherwise specified (Notes 1, 2 and 4)

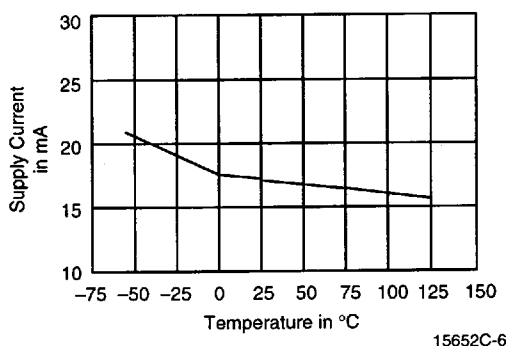
Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
$V_{OH}$	Output HIGH Voltage	$I_{OH} = -400 \mu A$	2.4		V
$V_{OL}$	Output LOW Voltage	$I_{OL} = 2.1 \text{ mA}$		0.45	V
$V_{IH}$	Input HIGH Voltage		2.0	$V_{CC} + 0.5$	V
$V_{IL}$	Input LOW Voltage		-0.5	+0.8	V
$I_{LI}$	Input Load Current	$V_{IN} = 0 \text{ V to } +V_{CC}$		1.0	$\mu A$
$I_{LO}$	Output Leakage Current	$V_{OUT} = 0 \text{ V to } +V_{CC}$		5.0	$\mu A$
$I_{CC1}$	$V_{CC}$ Active Current (Note 3)	$\overline{CE} = V_{IL}$ , $f = 10 \text{ MHz}$ , $I_{OUT} = 0 \text{ mA}$		30	mA
$I_{CC2}$	$V_{CC}$ TTL Standby Current	$\overline{CE} = V_{IH}$		1.0	mA
$I_{CC3}$	$V_{CC}$ CMOS Standby Current	$\overline{CE} = V_{CC} \pm 0.3 \text{ V}$		100	$\mu A$

## Notes:

- $V_{CC}$  must be applied simultaneously or before  $V_{PP}$ , and removed simultaneously or after  $V_{PP}$ .
- Caution:** The Am27X020 must not be removed from (or inserted into) a socket when  $V_{CC}$  or  $V_{PP}$  is applied.
- $I_{CC1}$  is tested with  $\overline{OE} = V_{IH}$  to simulate open outputs.
- Minimum DC Input Voltage is -0.5 V. During transitions, the inputs may overshoot to -2.0 V for periods less than 20 ns. Maximum DC Voltage on output pins is  $V_{CC} + 0.5 \text{ V}$ , which may overshoot to  $V_{CC} + 2.0 \text{ V}$  for periods less than 20 ns.



**Figure 1. Typical Supply Current vs. Frequency**  
 $V_{CC} = 5.5 \text{ V}$ ,  $T = 25^\circ \text{C}$



**Figure 2. Typical Supply Current vs. Temperature**  
 $V_{CC} = 5.5 \text{ V}$ ,  $f = 10 \text{ MHz}$

**CAPACITANCE**

Parameter Symbol	Parameter Description	Test Conditions	PD 032		PL 032		TS 032		Unit
			Typ	Max	Typ	Max	Typ	Max	
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0	10	12	8	10	10	12	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = 0	12	15	9	12	12	14	pF

**Notes:**

1. This parameter is only sampled and not 100% tested.
2. T<sub>A</sub> = +25°C, f = 1 MHz.

**SWITCHING CHARACTERISTICS over operating range unless otherwise specified (Notes 1, 3 and 4)**

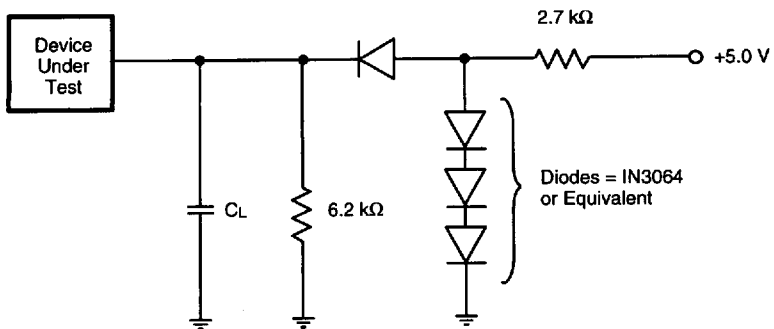
Parameter Symbols		Parameter Description	Test Conditions	Am27X020						Unit	
JEDEC	Standard			-75	-90	-120	-150	-200	-255		
tAVQV	tACC	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$	Min Max	— 70	— 90	— 120	— 150	— 200	— 250	ns
tELQV	tCE	Chip Enable to Output Delay	$\overline{OE} = V_{IL}$	Min Max	— 70	— 90	— 120	— 150	— 200	— 250	
tGLQV	tOE	Output Enable to Output Delay	$\overline{CE} = V_{IL}$	Min Max	— 40	— 50	— 50	— 65	— 75	— 100	ns
tEHQZ tGHQZ	tDF (Note 2)	Chip Enable HIGH or Output Enable HIGH, whichever comes first, to Output Float		Min Max	0 25	0 30	0 30	0 30	0 40	0 60	
tAXQX	tOH	Output Hold from Addresses, $\overline{CE}$ , or $\overline{OE}$ , whichever occurred first		Min Max	0 —	0 —	0 —	0 —	0 —	0 —	ns

**Notes:**

1. V<sub>CC</sub> must be applied simultaneously or before V<sub>PP</sub>, and removed simultaneously or after V<sub>PP</sub>.
2. This parameter is only sampled and not 100% tested.
3. **Caution:** The Am27X020 must not be removed from (or inserted into) a socket or board when V<sub>PP</sub> or V<sub>CC</sub> is applied.
4. Output Load: 1 TTL gate and C<sub>L</sub> = 100 pF  
 Input Rise and Fall Times: 20 ns  
 Input Pulse Levels: 0.45 V to 2.4 V  
 Timing Measurement Reference Level: 0.8 V and 2 V for inputs and outputs



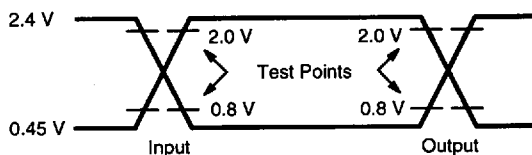
## SWITCHING TEST CIRCUIT



15652C-7

$C_L = 100\text{ pF}$  including jig capacitance

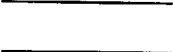



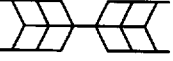
## SWITCHING TEST WAVEFORM



15652C-8

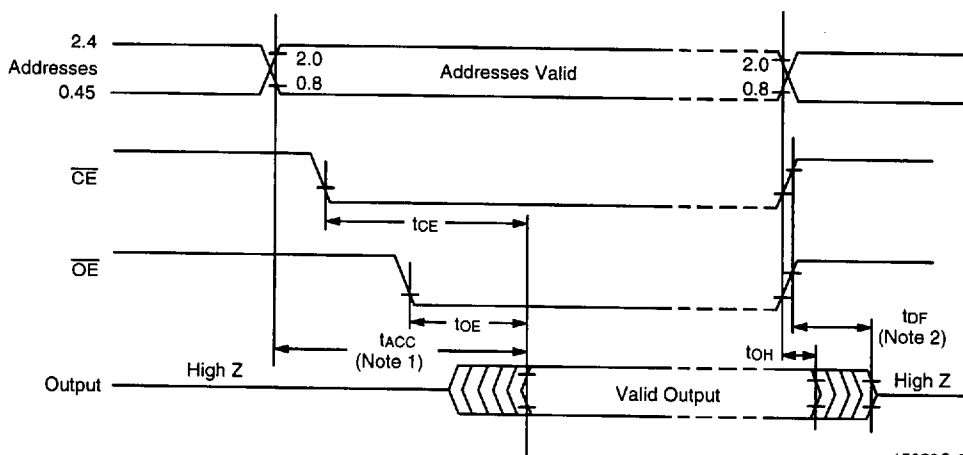
AC Testing: Inputs are driven at  $2.4\text{ V}$  for a Logic "1" and  $0.45\text{ V}$  for a Logic "0." Input pulse rise and fall times are  $\leq 20\text{ ns}$ .

# KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010

## SWITCHING WAVEFORMS



15652C-9

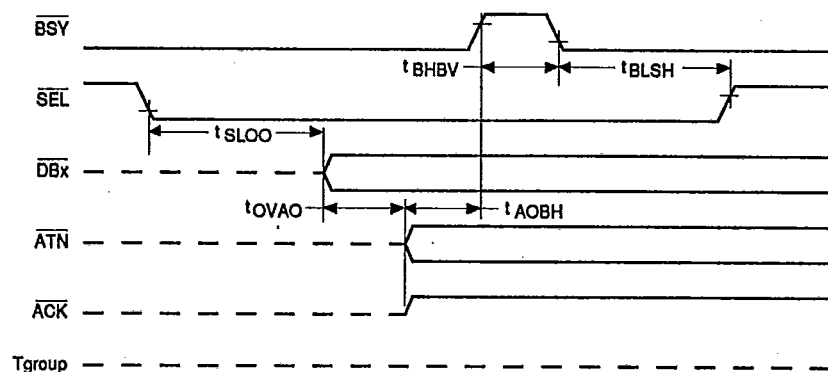
### Notes:

- $\overline{OE}$  may be delayed up to  $t_{ACC} - t_{OE}$  after the falling edge of the addresses without impact on  $t_{ACC}$ .
- $t_{OF}$  is specified from  $\overline{OE}$  or  $\overline{CE}$ , whichever occurs first.

SELECTING A TARGET (AS AN INITIATOR)

T-52-33-27

Symbol	Characteristic	Min	Max	Units
$t_{SLOO}$	SEL Out Low to "OR-ED" ID Out	1.2		us
$t_{OVAO}$	"OR-ED" ID Out Valid to ACK, ATN Out	100		ns
$t_{AOBH}$	ACK, ATN Out Valid to BSY Out High	100		ns
$t_{BHBV}$	BSY Out High to BSY In Low, Valid	400		ns
$t_{BLSH}$	BSY In Low to SEL Out High	100		ns

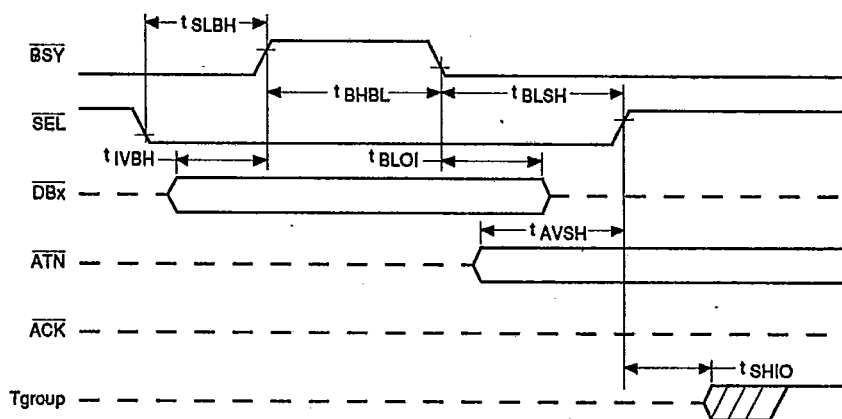


NOTE: Tgroup = signals driven by a Target =  $\overline{I/O}$ ,  $\overline{C/D}$ ,  $\overline{MSG}$ ,  $\overline{REQ}$

11853-027A

RESPONSE TO SELECTION (AS A TARGET)

Symbol	Characteristic	Min	Max	Units
$t_{SLBH}$	SEL In Low to $\overline{BSY}$ In High			ns
$t_{IVBH}$	"OR-ED" ID Valid In to $\overline{BSY}$ In High	0		ns
$t_{BHBL}$	SEL Low, ID Valid, $\overline{BSY}$ High to $\overline{BSY}$ Low	0.4	200	us
$t_{BLOI}$	BSY Out Low to "OR-ED" ID Invalid In	0		ns
$t_{BLSH}$	BSY Out Low to SEL In High	0		ns
$t_{AVSH}$	ATN Valid In to SEL In High	0		ns
$t_{SHIO}$	SEL In High to Tgroup Out	100		ns



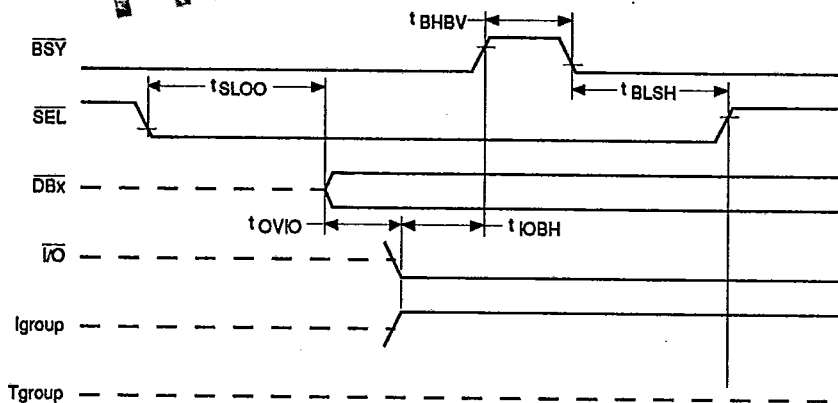
NOTE: Tgroup = signals driven by a Target =  $\overline{I/O}$ ,  $\overline{C/D}$ ,  $\overline{MSG}$ ,  $\overline{REQ}$

11853-028A

## RESELECTING AN INITIATOR (AS A TARGET)

T-52-33-27

Symbol	Characteristic	Min	Max	Units
$t_{SLOO}$	SEL Out Low to "OR-ED" ID Out	2		$\mu s$
$t_{OVIO}$	"OR-ED" ID Out Valid to I/O & Tgroup Out Valid	100		ns
$t_{IOBH}$	I/O & Tgroup Out Valid to BSY Out High	100		ns
$t_{BHBV}$	BSY Out High to BSY In Low Valid	400		ns
$t_{BLSH}$	BSY In Low to SEL Out High	100		ns

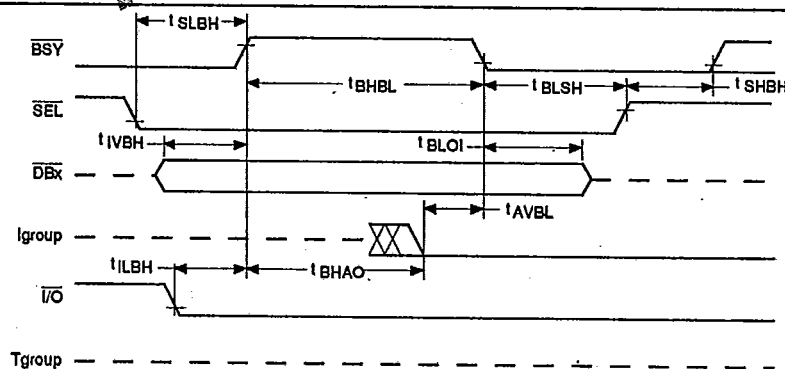


NOTE: Tgroup = signals driven by a Target =  $\overline{C/D}$ , MSG, REQ  
Igroup = signals driven by an Initiator = ATN, ACK

11853-028A

## RESPONSE TO RESELECTION (AS AN INITIATOR)

Symbol	Characteristic	Min	Max	Units
$t_{SLBH}$	SEL In Low to BSY In High	0		ns
$t_{IVBH}$	"OR-ED" ID Valid In to BSY In High	0		ns
$t_{ILBH}$	I/O In Low to BSY In High	0		ns
$t_{BHAO}$	SEL Low, ID Valid, BSY High to Igroup Out	100		ns
$t_{AVBL}$	Igroup Valid Out to BSY Out Low	100		ns
$t_{BHBL}$	BSY In High to BSY Out Low	0.4	200	$\mu s$
$t_{BLOI}$	BSY Out Low to "OR-ED" ID Invalid In	0		ns
$t_{BLSH}$	BSY Out Low to SEL In High	0		ns
$t_{SHBH}$	SEL In High to BSY Out High	0		ns



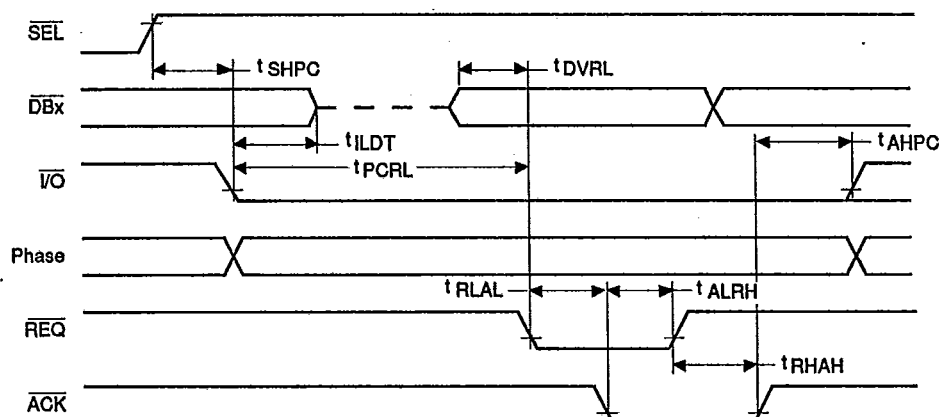
Tgroup = signals driven by a Target =  $\overline{C/D}$ , MSG, REQ  
Igroup = signals driven by an Initiator = ATN, ACK  
\*\*\* BSY will still be driven by the reselecting target.

11853-030A

## RECEIVE ASYNCHRONOUS INFORMATION TRANSFER IN (ACTING AS AN INITIATOR)

T-52-33-27

Symbol	Characteristic	Min	Max	Units
$t_{SHPC}$	$\overline{SEL}$ In High to Phase Change In	0		ns
$t_{ILDT}$	$\overline{I/O}$ In Low to Data Bus TRISTATE	0	125	ns
$t_{PCRL}$	Phase Change In to $\overline{REQ}$ In Low	400		ns
$t_{DVRL}$	Data Valid In to $\overline{REQ}$ In Low	0		ns
$t_{RLAL}$	$\overline{REQ}$ In Low to $\overline{ACK}$ Out Low	0	175	ns
$t_{ALDI}$	$\overline{ACK}$ Out Low to Data Invalid In	0		ns
$t_{ALRH}$	$\overline{ACK}$ Out Low to $\overline{REQ}$ In High	0		ns
$t_{RHAH}$	$\overline{REQ}$ In High to $\overline{ACK}$ Out High	0	175	ns
$t_{AHPC}$	$\overline{ACK}$ Out High to Phase Change In	0		ns



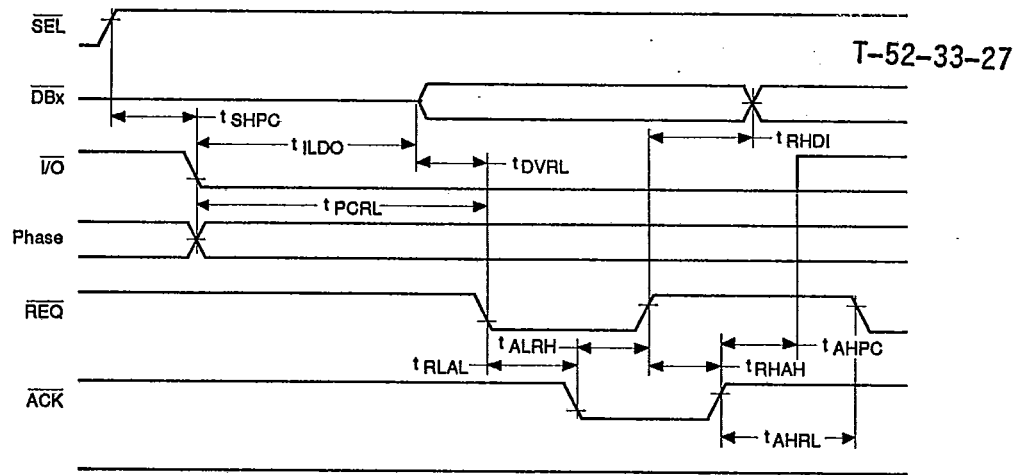
ATN

NOTE: Phase = signals that define the bus phase  $\overline{C/D}$ , MSG

11853-031A

## SEND ASYNCHRONOUS INFORMATION TRANSFER IN (ACTING AS A TARGET)

Symbol	Characteristic	Min	Max	Units
$t_{SHPC}$	$\overline{SEL}$ In High to Phase Change Out	100		ns
$t_{ILDO}$	$\overline{I/O}$ Out Low to Data Out	800		ns
$t_{DVRL}$	Data Out Valid to $\overline{REQ}$ Out Low	55		ns
$t_{PCRL}$	Phase Change Out to $\overline{REQ}$ Out Low	500		ns
$t_{RLAL}$	$\overline{REQ}$ Out Low to $\overline{ACK}$ In Low	0		ns
$t_{ALRH}$	$\overline{ACK}$ In Low to $\overline{REQ}$ Out High	0	175	ns
$t_{ALDI}$	$\overline{ACK}$ In Low to Data Out Invalid	0		ns
$t_{RHAH}$	$\overline{REQ}$ Out High to $\overline{ACK}$ In High	0		ns
$t_{AHPC}$	$\overline{ACK}$ In High to Phase Change Out	100		ns
$t_{AHRL}$	$\overline{ACK}$ In High to $\overline{REQ}$ Out Low	0	175	ns

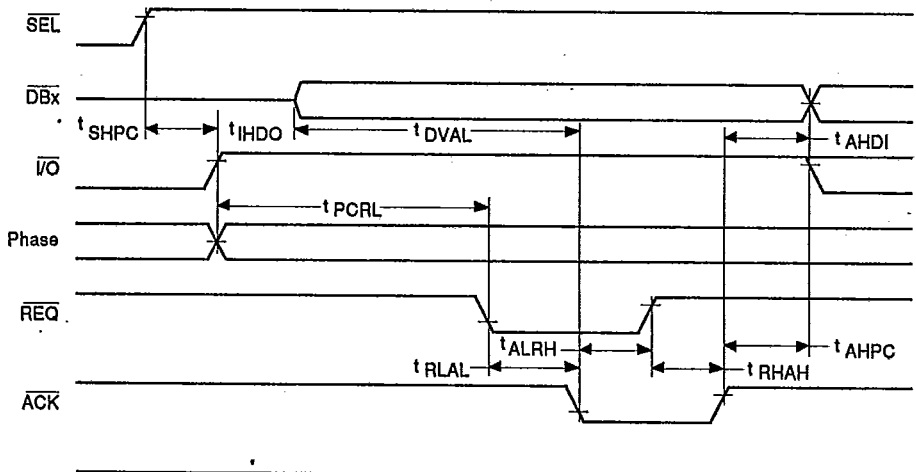


ATN NOTE: Phase = signals that define the bus phase  $\overline{C/D}$ ,  $\overline{MSG}$

11853-032A

SEND ASYNCHRONOUS INFORMATION TRANSFER OUT (ACTING AS AN INITIATOR)

Symbol	Characteristic	Min	Max	Units
$t_{SHPC}$	SEL In High to Phase Change In	0		ns
$t_{IHDO}$	I/O In High to Data Out	0		ns
$t_{PCRL}$	Phase Change In to REQ In Low	400		ns
$t_{RLAL}$	REQ In Low to ACK Out Low	0	175	ns
$t_{DVAL}$	Data Out Valid to ACK Out Low	55		ns
$t_{ALRH}$	ACK Out Low to REQ In High	0		ns
$t_{RHAH}$	REQ In High to ACK Out High	0	175	ns
$t_{RHDI}$	REQ In High to Data Out Invalid	0		ns
$t_{AHPC}$	ACK Out High to Phase Change In	0		ns



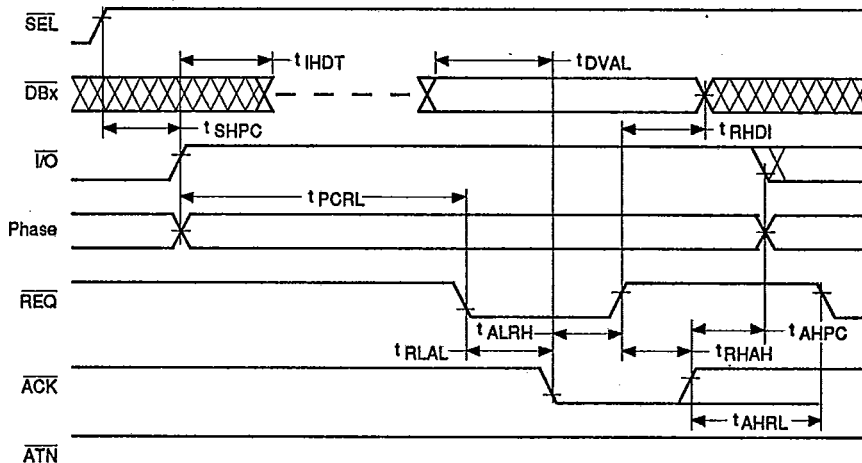
ATN NOTE: Phase = signals that define the bus phase  $\overline{C/D}$ ,  $\overline{MSG}$

11853-033A

## RECEIVE ASYNCHRONOUS INFORMATION TRANSFER OUT (ACTING AS A TARGET)

Symbol	Characteristic	Min	Max	Units
$t_{SHPC}$	$\overline{SEL}$ In High to Phase Change Out	100		ns
$t_{IHDT}$	$\overline{I/O}$ Out High to Data Bus TRISTATE	0		ns
$t_{PCRL}$	Phase Change to $\overline{REQ}$ Out Low	500		ns
$t_{RLAL}$	$\overline{REQ}$ Out Low to $\overline{ACK}$ In Low	0		ns
$t_{DVAL}$	Data In Valid to $\overline{ACK}$ In Low	0		ns
$t_{ALRH}$	$\overline{ACK}$ In Low to $\overline{REQ}$ Out High	0	175	ns
$t_{RHDI}$	$\overline{REQ}$ Out High to Data In Invalid	0		ns
$t_{RAHA}$	$\overline{REQ}$ Out High to $\overline{ACK}$ In High	0		ns
$t_{AHPC}$	$\overline{ACK}$ In High to Phase Change Out	0		ns
$t_{AHRL}$	$\overline{ACK}$ In High to $\overline{REQ}$ Out Low	0	175	ns

T-52-33-27

NOTE: Phase = signals that define the bus phase  $\overline{C/D}$ ,  $\overline{MSG}$ 

11853-034A

## RECEIVE SYNCHRONOUS INFORMATION TRANSFER IN (ACTING AS AN INITIATOR)

Symbol	Characteristic	Min	Max	Units
$t_{DVRL}$	Data Valid In to $\overline{REQ}$ In Low	0		ns
$t_{RLDI}$	$\overline{REQ}$ In Low to DATA Invalid	45		ns
$t_{RLRH}$	$\overline{REQ}$ In Low to $\overline{REQ}$ In High	50		ns
$t_{RHRL}$	$\overline{REQ}$ In High to $\overline{REQ}$ In Low	50		ns
$t_{ALAH}$	$\overline{ACK}$ Out Low to $\overline{ACK}$ Out High	Tcyc-10		ns
$t_{AHAL}$	$\overline{ACK}$ Out High to $\overline{ACK}$ Out Low	Tcyc-25		ns
$t_{AHPC}$	$\overline{ACK}$ Out High to Phase Change	0		ns

Parameters  $t_{SHPC}$ ,  $t_{IHDT}$ , and  $t_{PCRL}$  are also applicable and are identical to those in Receive Asynchronous Information Transfer In (Acting as an Initiator), top of page 37.