Am2847 • Am2896

Quad 80-Bit and Quad 96-Bit Static Shift Registers

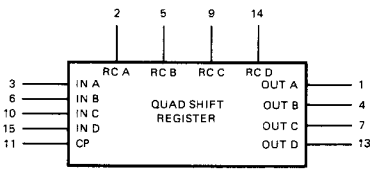
Distinctive Characteristics

- Plug-in replacement for 2532B, TMS3120, TMS 3409, MK1007, 3347
- Internal recirculates on each register
- Single TTL compatible clock
- Outputs sink two TTL loads
- Operation guaranteed from DC to 3 MHz
- 100% reliability assurance testing in compliance with MIL-STD-883

FUNCTIONAL DESCRIPTION

The Am2847 and Am2896 are quad 80-and 96-bit static MOS shift registers. Each device contains four shift registers, each with a TTL-compatible input, output, and recirculate control. When the RC signal is LOW, the corresponding register accepts data from its data input; when RC is HIGH, the data at the register output is written back in at the input. The four registers are driven by a common TTL compatible clock input. The registers shift on the HIGH-to-LOW transition of the clock. Storage is dynamic while the clock is HIGH and static while the clock is LOW, so the clock may be stopped indefinitely in the LOW state. Each register output can drive two TTL unit loads.

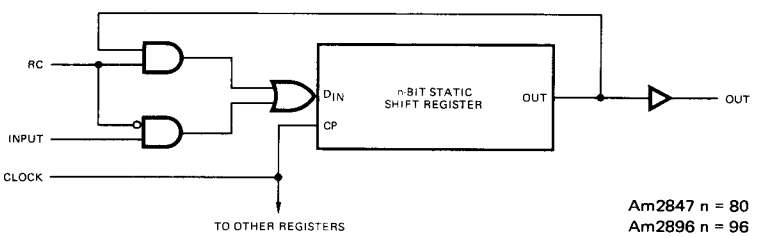
LOGIC SYMBOL



V_{SS} = Pin 16
V_{DD} = Pin 8
V_{GG} = Pin 12

MOS-435

LOGIC BLOCK DIAGRAM
(One Register Shown)



Am2847 n = 80
Am2896 n = 96

MOS-436

ORDERING INFORMATION

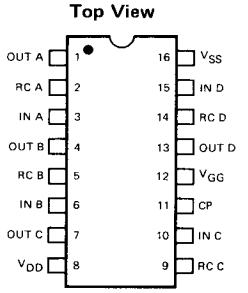
Am2847 Quad 80-Bit

Package Type	Temperature Range	Order Number
16-Pin Molded DIP	0°C to +70°C	AM2847PC
16-Pin Hermetic DIP	0°C to +70°C	AM2847DC
16-Pin Hermetic DIP	−55°C to +125°C	AM2847DM

Am2896 Quad 96-Bit

16-Pin Molded DIP	0°C to +70°C	AM2896PC
16-Pin Hermetic DIP	0°C to +70°C	AM2896DC
16-Pin Hermetic DIP	−55°C to +125°C	AM2896DM

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

MOS-437

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MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +160°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{DD} Supply Voltage	V_{SS} −10V to V_{SS} +0.3V
V_{GG} Supply Voltage	V_{SS} −20V to V_{SS} +0.3V
DC Input Voltage	V_{SS} −20V to V_{SS} +0.3V

OPERATING RANGE

Part Number	Ambient Temperature	V_{SS}	V_{DD}	V_{GG}
Am2847DM Am2896DM	−55°C to +125°C	5.0V ±5%	0V	−12V ±5%
Am2847PC, DC Am2896PC, DC	0°C to +70°C	5.0V ±5%	0V	−12V ±5%

ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

Parameters	Description	Test Conditions		Min.	Typ. (Note 1)	Max.	Units
V_{OH}	Output HIGH Voltage	I_{OH} = −0.5mA		2.4			Volts
V_{OL}	Output LOW Voltage	I_{OL} = 3.2mA	0°C to 70°C			0.4	Volts
		I_{OL} = 2.4mA	−55° to 125°C				
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		V_{SS} −1.0		V_{SS} +0.3	Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs		V_{SS} −18.5		0.8	Volts
I_{LI}	Input Leakage Current	V_{IN} = −5.0V, all other pins connected to V_{SS}				1.0	µA
I_{IL}	Input LOW Current	V_{IN} = 0.4V			−1.0	−1.6	mA
I_{IH}	Input HIGH Current	V_{IN} = V_{SS} −1.0V		−0.1			mA
I_{DD}	V_{DD} Power Supply Current	Output open, f = 2.5MHz	0°C to 70°C		25	35	mA
			−55°C to 125°C			45	
I_{GG}	V_{GG} Power Supply Current		0°C to 70°C		10	15	
			−55°C to 125°C			20	

Note: 1. Typical Limits are at V_{SS} = 5.0V, V_{GG} = −12V, 25°C ambient.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

Parameters	Description	Test Conditions		Min.	Typ.	Max.	Units
f	Clock Frequency	0°C to 70°C		0		3.0	MHz
		−55°C to 125°C				2.5	
$t_{\phi pw}H$	Clock HIGH Time	0°C to 70°C		.140		100	µs
		−55°C to 125°C		.150		10	
$t_{\phi pw}L$	Clock LOW Time	0°C to 70°C		.140		∞	µs
		−55°C to 125°C		.180			
t_r, t_f	Clock Rise and Fall Times			10		200	ns
t_s	Set-Up Time, D or RC Inputs (see definitions)	t_r = t_f = 10ns	0°C to 70°C	120			ns
			−55°C to 125°C	120			
t_h	Hold Time, D or RC Inputs (see definitions)	t_r = t_f = 10ns	0°C to 70°C	40			ns
			−55°C to 125°C	60			
t_{pd}	Delay, Clock to Output LOW or HIGH	R_L = 4k, C_L = 10pF	0°C to 70°C	(Note 3)		200	ns
			−55°C to 125°C			280	
C_{in}	Capacitance, Data Clock and RC Inputs (Note 2)	f = 1MHz, V_{IN} = V_{SS}			3.0	7.0	pF
C_ϕ	Capacitance, Clock Input (Note 2)	f = 1MHz, V_{IN} = V_{SS}			3.0	7.0	pF

Notes: 2. This parameter is periodically sampled but not 100% tested. It is guaranteed by design.
3. At any temperature, t_{pd} min. is always much greater than t_h(D) max.

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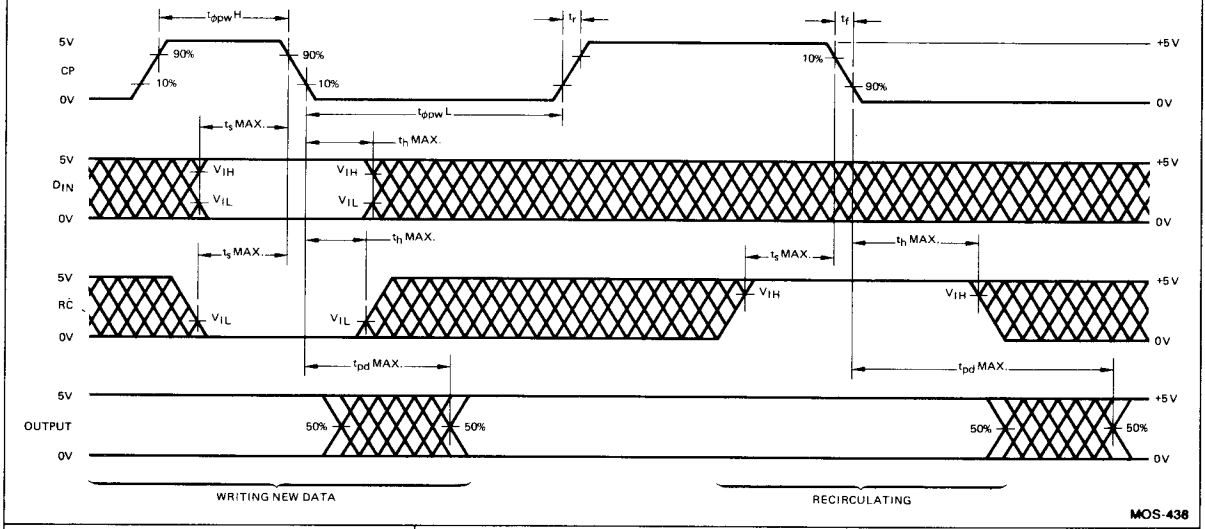
TIMING DIAGRAM

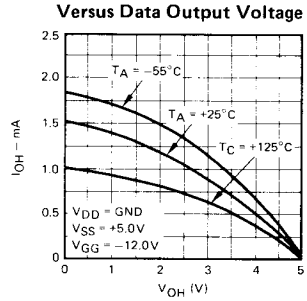


KEY TO TIMING DIAGRAM

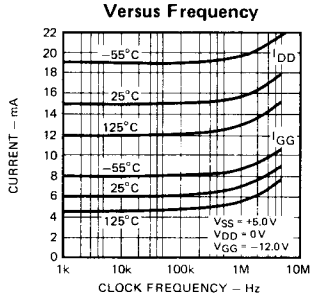
WAVEFORM	INPUTS	OUTPUTS
———	MUST BE STEADY	WILL BE STEADY
▨	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
▨	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
▨	DON'T CARE: ANY CHANGE PERMITTED	CHANGING: STATE UNKNOWN

PERFORMANCE CURVES

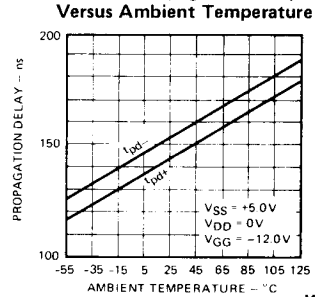
Typical Data Output HIGH Current Versus Data Output Voltage



Typical Power-Supply Currents Versus Frequency



Typical Propagation Delay Versus Ambient Temperature



DEFINITION OF TERMS

STATIC SHIFT REGISTER A shift register that is capable of maintaining stored data without being continuously clocked. Most static shift registers are constructed with dynamic master and static slave flip-flops. The data is stored dynamically while the clock is HIGH and is transferred to the static slaves while the clock is LOW. The clock may be stopped indefinitely in the LOW state, but there are limitations on the time it may reside in the HIGH state.

SET-UP and HOLD TIMES The shift register will accept the data that is present on its input around the time the clock goes from HIGH-to-LOW. Because of variations in individual devices, there is some uncertainty as to exactly when, relative to this clock transition, the data will be stored. The set-up and hold times define the limits on this uncertainty. To guarantee storing the correct data, the data inputs should not be changed between the maximum set-up time before the clock transition and the maximum hold time after the clock transition. Data changes within this interval may or may not be detected.

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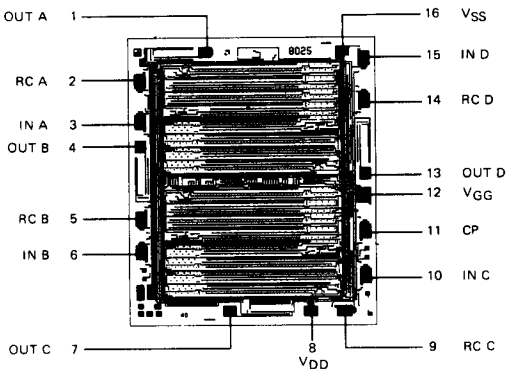
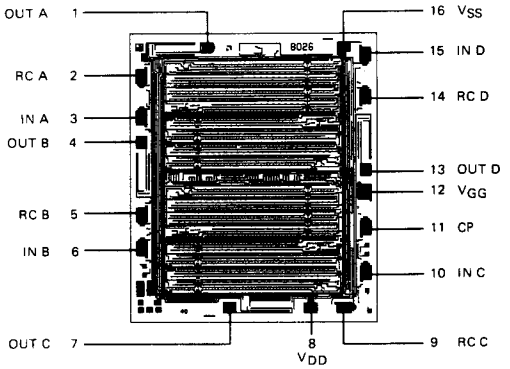
Metallization and Pad Layouts

Am2847



DIE SIZE 0.106" X 0.128"

Am2896



DIE SIZE 0.106" X 0.128"

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