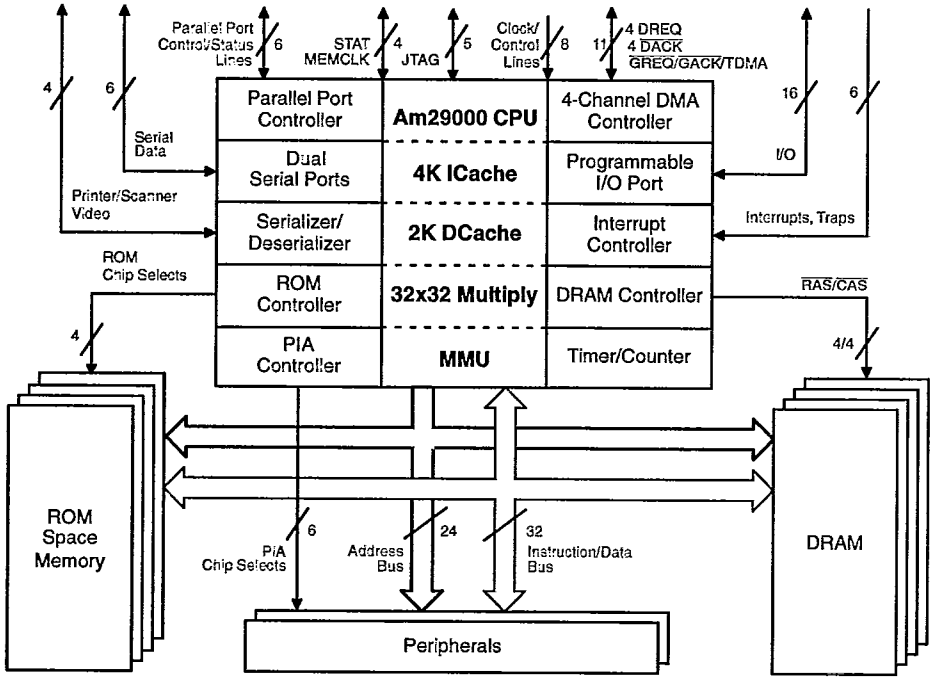
ADVANCE INFORMATION

Am29240™, Am29245™, and Am29243™

High-Performance RISC Microcontrollers

Advanced Micro Devices

Am29240 MICROCONTROLLER BLOCK DIAGRAM



DISTINCTIVE CHARACTERISTICS

Am29240 Microcontroller

- Completely integrated system for embedded applications
- Full 32-bit architecture
- 4-Kbyte two-way set-associative instruction cache
- 2-Kbyte two-way set-associative data cache
- Single cycle 32-bit multiplier for faster integer math; two-cycle Multiply Accumulate (MAC) function
- 16-entry on-chip Memory Management Unit (MMU) with one Translation Look-Aside Buffer
- 4-Gbyte virtual address space, 304-Mbyte physical space implemented
- Glueless system interfaces with on-chip wait state control
- 25 million instructions per second (MIPS) sustained at 33 MHz
- Four banks of ROM, each separately programmable for 8-, 16-, or 32-bit interface
- Four banks of DRAM, each separately programmable for 16- or 32-bit interface
- Single-cycle ROM burst-mode and DRAM page-mode access
- 4-channel double-buffered DMA controller with queued reload
- 6-port peripheral interface adapter
- 16-line programmable I/O port

Publication #: 17787 Rev. B Amendment: /0
Issue Date: July 1993

- Two serial ports (UARTs)
- Bidirectional parallel port controller
- Bidirectional bit serializer/deserializer (video interface)
- Interrupt controller
- Full- and double-speed internal clock
- Fully pipelined
- Three-address instruction architecture
- 192 general purpose registers
- 20-, 25-, and 33-MHz operating frequencies
- Traceable Cache™ instruction and data cache tracing feature
- IEEE Std. 1149.1–1990 (JTAG) compliant Standard Test Access Port and Boundary Scan Architecture
- Binary compatibility with all 29K Family microprocessors and microcontrollers
- Fully static system clock capabilities
- 3.3 V–5 V operating range
- CMOS technology/TTL compatible

Am29245 Microcontroller

The low-cost Am29245 microcontroller is similar to the Am29240 microcontroller, without the data cache and 32-bit multiplier. It includes the following features:

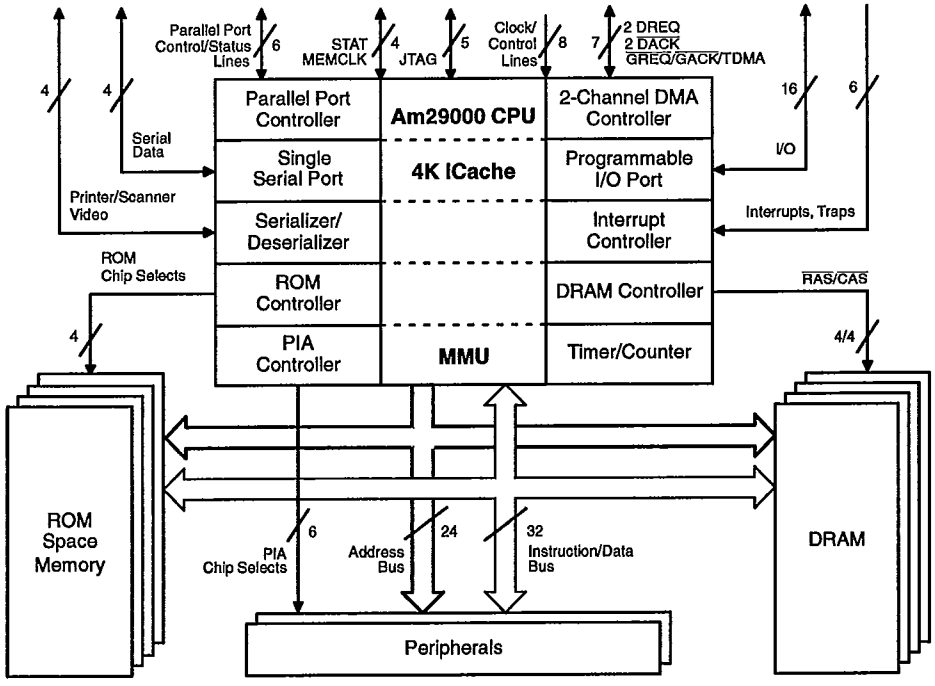
- One serial port (UART)
- Two-channel DMA controller
- 16-MHz operating frequency

Am29243 Microcontroller

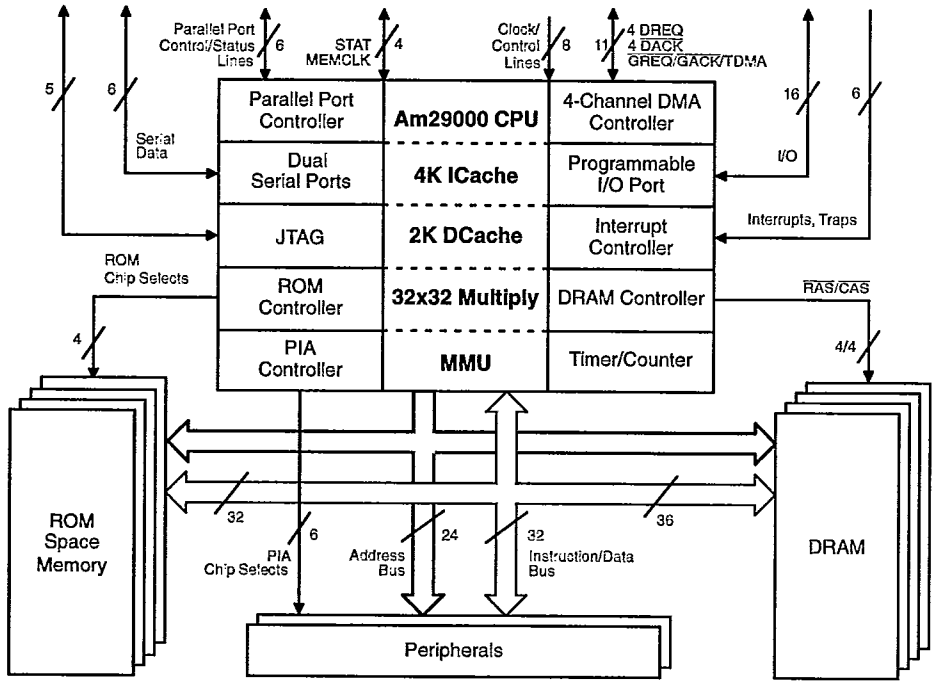
The Am29243 data microcontroller is similar to the Am29240 microcontroller, without the video interface. It includes the following additional features:

- DRAM parity
- 32-entry on-chip MMU with dual Translation Look-Aside Buffers (TLBs)

Am29245 MICROCONTROLLER BLOCK DIAGRAM



Am29243 MICROCONTROLLER BLOCK DIAGRAM



GENERAL DESCRIPTION

The Am29240 microcontroller series is an enhanced bus-compatible extension of the Am29200™ RISC microcontroller family, with two to four times the performance. The Am29240 microcontroller series includes the Am29240 microcontroller, the low-cost Am29245 microcontroller, and the Am29243 data microcontroller. The on-chip caches, MMU, faster integer math, and extended DMA addressing capability of the Am29240 microcontroller series allow the embedded systems designer to provide increasing levels of performance and software compatibility throughout a range of products (see Table 1).

Based on a static low-voltage design, these CMOS-technology devices offer a complete set of system peripherals and interfaces commonly used in embedded applications. Compared to CISC processors, the Am29240 microcontroller series offers better performance, more efficient use of low-cost memories, lower system cost, and complete design flexibility for the designer. Coupled with hardware and software development tools from AMD® and the AMD Fusion29K℠ partners, the Am29240 microcontroller series provides the embedded product designer with the cost and performance edge required by today's marketplace.

Am29240 Microcontroller

For general purpose embedded applications, such as mass storage controllers, communications, digital signal processing, networking, industrial control, pen-based systems, and multimedia, the Am29240 microcontroller provides a high-performance solution with a low total system cost. The memory interface of the Am29240 microcontroller provides even faster direct memory access than the Am29200 microcontroller. This performance improvement minimizes the effect of memory latency, allowing designers to use low-cost memory with simpler memory designs. On-chip instruction and data caches provide even better performance for time-critical code. Other on-chip functions include: a ROM controller, DRAM controller, peripheral interface adapter controller, DMA controller, programmable I/O port, parallel port controller, serial ports, and an interrupt controller. For a complete description of the technical features, on-chip peripherals, programming interface, and instruction set, please refer to the *Am29240, Am29245, and Am29243 RISC Microcontrollers User's Manual and Data Sheet* (order #17741C).

The Am29240 microcontroller is available in a 196-pin plastic quad flat-pack (PQFP) package. Of the available 196 pins, 150 are signal inputs and outputs, 36 are power and ground connections, and 10 are no-connects.

Am29245 Microcontroller

The low-cost Am29245 microcontroller is designed for embedded applications in which cost and space constraints, along with increased performance requirements, are primary considerations. In addition, the Am29245 microcontroller provides an easy upgrade path for Am29200 and Am29205™ microcontroller-based products.

The Am29245 microcontroller is available in a 196-pin PQFP package. Of the available 196 pins, 144 are signal inputs and outputs, 36 are power and ground connections, and 16 are no-connects.

Am29243 Microcontroller

With DRAM parity support and a full MMU, the Am29243 data microcontroller is recommended for communications applications that require high-speed data movement and fast protocol processing in a fault-tolerant environment.

Both the Am29243 and Am29240 microcontrollers support fly-by DMA at 100 Mbytes/sec for LANs and switching applications, and a two-cycle Multiply Accumulate function for DSP applications. The low power requirements make either microcontroller a good choice for field-deployed devices.

The Am29243 microcontroller is available in a 196-pin PQFP package. Of the available 196 pins, 150 are signal inputs and outputs, 36 are power and ground connections, and 8 are no-connects.

RELATED AMD PRODUCTS

29K Family Devices

Part No.	Description
Am29000™	32-Bit RISC Microprocessor
Am29005™	Low-Cost 32-Bit RISC Microprocessor with No MMU and No BTC
Am29030™	32-Bit RISC Microprocessor with 8-Kbyte Instruction Cache
Am29035™	32-Bit RISC Microprocessor with 4-Kbyte Instruction Cache
Am29050™	32-Bit RISC Microprocessor with On-Chip Floating Point
Am29200	32-Bit RISC Microcontroller
Am29205	Low-Cost RISC Microcontroller with 16-Bit Bus Interface

29K™ Family Development Support Products

Contact your local AMD representative for information on the complete set of development support tools. The following software and hardware development products are available on several hosts:

- Optimizing compilers for common high-level languages
- Assembler and utility packages
- Source- and assembly-level software debuggers
- Target-resident development monitors
- Simulators
- Execution boards

Third-Party Development Support Products

The Fusion29K Program of Partnerships for Application Solutions provides the user with a vast array of products designed to meet critical time-to-market needs. Products/solutions available from the AMD Fusion29K Partners include

- Silicon products
- Software generation and debug tools
- Hardware development tools
- Board level products
- Laser printer solutions
- Multiuser, kernel, and real-time operating systems
- Graphics solutions
- Networking and communication solutions
- Manufacturing support
- Custom software consulting, support, and training

Table D-1 Product Comparison—Am29200 Microcontroller Family

FEATURE	Am29205 Microcontroller	Am29200 Microcontroller	Am29245 Microcontroller	Am29240 Microcontroller	Am29243 Microcontroller
Instruction Cache	—	—	4 Kbytes	4 Kbytes	4 Kbytes
Data Cache	—	—	—	2 Kbytes	2 Kbytes
Integer Multiplier	Software	Software	Software	32 x 32-bit	32 x 32-bit
MMU	—	—	1 TLB 16 Entry	1 TLB 16 Entry	2 TLBs 32 Entry
Data Bus Width					
Internal	32 bits	32 bits	32 bits	32 bits	32 bits
External	16 bits	32 bits	32 bits	32 bits	32 bits
ROM Interface					
Banks	3	4	4	4	4
Width	16 bits only	8, 16, 32 bits	8, 16, 32 bits	8, 16, 32 bits	16, 32 bits
ROM Size (Max/Bank)	4 Mbytes	16 Mbytes	16 Mbytes	16 Mbytes	16 Mbytes
Boot-up ROM Width	16 bits	8, 16, 32 bits	8, 16, 32 bits	8, 16, 32 bits	8, 16, 32 bits
Burst-mode access	Not Supported	Supported	Supported	Supported	Supported
DRAM Interface					
Banks	4	4	4	4	4
Width	16 bits only	16, 32 bits	16, 32 bits	16, 32 bits	8, 16, 32 bits
Size: 32-bit mode	—	16 Mbytes/bank	16 Mbytes/bank	16 Mbytes/bank	16 Mbytes/bank
Size: 16-bit mode	8 Mbytes/bank	8 Mbytes/bank	8 Mbytes/bank	8 Mbytes/bank	8 Mbytes/bank
Video DRAM	Not Supported	Supported	Supported	Supported	Not Supported
Initial/Burst Access Cycles	3/2	3/2	2/1	2/1	2/1
On-Chip DMA					
Width (ext. peripherals)	8, 16 bits	8, 16, 32 bits	8, 16, 32 bits	8, 16, 32 bits	8, 16, 32 bits
Externally Controlled	1 Channel	2 Channels	2 Channels	4 Channels	4 Channels
$\overline{\text{GREQ}}$/$\overline{\text{GACK}}$ Access	No	Yes	Yes	Yes	Yes
$\overline{\text{GREQ}}$/$\overline{\text{GACK}}$ Burst	No	No	Yes	Yes	Yes
TDMA	No	Yes	Yes	Yes	Yes
Double-Frequency CPU Option	No	No	No	Yes	Yes
Low Voltage Operation	No	No	Yes	Yes	Yes
PIA					
PIA Ports	2	6	6	6	6
Data Width	8, 16 bits	8, 16, 32 bits	8, 16, 32 bits	8, 16, 32 bits	8, 16, 32 bits
Cycles	3	3	2	2	2
Programmable I/O Port					
Signals	8	16	16	16	16
Serial Ports					
Ports	1 Port	1 Port	1 Port	2 Ports	2 Ports
$\overline{\text{DSR}}$	Not Supported	Supported	Supported	1 Port Supported	1 Port Supported
$\overline{\text{DTR}}$	Not Supported	Supported	Supported	1 Port Supported	1 Port Supported
Interrupt Controller					
External Interrupt Pins	2	4	4	4	4
External Trap and Warn Pins	0	3	3	3	3
Parallel Port Controller	Yes	Yes	Yes	Yes	Yes
Full-Word Transfer	No	Yes	Yes	Yes	Yes
JTAG Testing	No	Yes	Yes	Yes	Yes
Serializer/Deserializer	Yes	Yes	Yes	Yes	No
DRAM Parity	No	No	No	No	Yes
Pin Count and Package	100 PQFP	168 PQFP	196 PQFP	196 PQFP	196 PQFP
Processor Clock Rate	16 MHz	16, 20 MHz	16 MHz	20, 25, 33 MHz	20, 25, 33 MHz

KEY FEATURES AND BENEFITS

The Am29240 microcontroller series extends the line of RISC microcontrollers based on the 29K architecture, providing performance upgrades to the Am29205 and Am29200 microcontrollers. The RISC microcontroller product line allows users to benefit from the very high performance of the 29K architecture, while also capitalizing on the very low system cost made possible by the integration of processor and peripherals.

The Am29240 microcontroller series expands the price/performance range of systems that can be built with the 29K Family. The Am29240 microcontroller series is fully software compatible with the Am29000, Am29005, Am2903, Am29035, and Am29050 microprocessors, as well as the Am29200 and Am29205 microcontrollers. It can be used in existing 29K Family microcontroller applications without software modifications.

On-Chip Caches

The Am29240 microcontroller series incorporates a 4-Kbyte, two-way instruction cache that supplies most processor instructions without wait states at the processor frequency. For best performance, the instruction cache supports critical-word-first reloading with fetch-through, so that the processor receives the required instruction and the pipeline restarts with minimum delay. The instruction cache has a valid bit per word to minimize the reload overhead. All cache array elements are visible to software for testing and preload.

The Am29240 and Am29243 microcontrollers incorporate a 2-Kbyte, two-way set-associative data cache. The data cache appears in the execute stage of the processor pipeline, so that loaded data is available immediately to the next instruction. This provides the maximum performance for loads without requiring load scheduling. The data cache performs critical-word-first, wrap-around, burst-mode refill with load-through. This minimizes the time the processor waits on external data as well as minimizing the reload time. The data cache uses a write-through policy with a two-entry write buffer. Byte, half-word, and word reads and writes are supported. All cache array elements are visible to software for testing and preload.

Single-Cycle Multiplier

The Am29240 and Am29243 microcontrollers incorporate a full combinatorial multiplier that accepts two 32-bit input operands and produces a 32-bit result in a single cycle. The multiplier can produce a 64-bit result in two cycles. The multiplier permits maximum performance without requiring instruction scheduling, since the latency of the multiply is the same as the latency of other integer operations. High-performance multiplication benefits imaging, signal processing, and state modeling applications.

Complete Set of Common System Peripherals

The Am29240 microcontroller series minimizes system cost by incorporating a complete set of system facilities commonly found in embedded applications, eliminating the cost of additional components. The on-chip functions include: a ROM controller, a DRAM controller, a peripheral interface adapter, a DMA controller, a programmable I/O port, a parallel port, two serial ports, and an interrupt controller. A video interface is also included in the Am29240 and Am29245 microcontrollers for printer, scanner, and other imaging applications. These facilities allow many simple systems to be built using only the Am29240 microcontroller series, external ROM, and/or DRAM memory.

ROM Controller

The ROM controller supports four individual banks of ROM or other static memory, each with its own timing characteristics. Each ROM bank may be a different size and may be either 8, 16, or 32 bits wide. The ROM banks can appear as a contiguous memory area of up to 64 Mbyte in size. The ROM controller also supports byte, half-word, and word writes to the ROM memory space for devices such as flash EPROMs and SRAMs.

DRAM Controller

The DRAM controller supports four separate banks of dynamic memory. Each bank may be a different size and may be either 16 or 32 bits wide. The DRAM banks can appear as a contiguous memory area of up to 64 Mbyte in size. To further enhance the performance, the DRAM controller supports two-cycle accesses, with single-cycle page-mode and burst-mode accesses.

Peripheral Interface Adapter

The Peripheral Interface Adapter (PIA) permits glueless interfacing to as many as six external peripheral chips. The PIA allows for additional system features implemented by external peripheral chips.

DMA Controller

The DMA controller provides up to four channels for transferring data between the DRAM and internal or external peripherals. The DMA channels are double buffered to relax constraints on reload time.

I/O Port

The I/O port permits direct access to 16 individually programmable external input/output signals. Eight of these signals can be configured to cause interrupts.

Parallel Port

The parallel port implements a bidirectional IBM PC-compatible parallel interface to a host processor.

Serial Port

The serial port implements up to two full-duplex UARTs.

Serializer/Deserializer

The serializer/deserializer (video interface) permits direct connection to a number of laser marking engines, video displays, or raster input devices such as scanners.

Interrupt Controller

The interrupt controller generates and reports the status of interrupts caused by on-chip peripherals.

Wide Range of Price/Performance Points

To reduce design costs and time-to-market, the product designer can use the Am29200 microcontroller family and one basic system design as the foundation for an entire product line. From this design, numerous implementations of the product at various levels of price and performance may be derived with minimum time, effort, and cost.

The Am29240 RISC microcontroller series supports this capability through various combinations of on-chip caches, programmable memory widths, programmable wait states, burst-mode and page-mode access support, bus compatibility, and 29K Family software compatibility. A system can be upgraded without hardware and software redesign using various memory architectures.

Within the Am29240 microcontroller series, the external interfaces operate at frequencies in the range of 16 to 25 MHz, and the processor operates at frequencies in the range of 16 to 33 MHz. The internal processor core can operate either at the interface frequency or twice this frequency. For example, the processor can operate at 33 MHz while the interface operates at 16.5 MHz.

The ROM controller accommodates memories that are either 8, 16, or 32 bits wide, and the DRAM controller accommodates dynamic memories that are either 16 or 32 bits wide. This unique feature provides a flexible interface to low-cost memory as well as a convenient, flexible upgrade path. For example, a system can start with a 16-bit memory design and can subsequently improve performance by migrating to a 32-bit memory design. One particular advantage is the ability to add memory in half-megabyte increments. This provides significant cost savings for applications that do not require larger memory upgrades.

The Am29200, Am29205, Am29240, Am29245, and Am29243 microcontrollers allow users to address an extremely wide range of cost performance points, with higher performance and lower cost than existing designs based on CISC microprocessors.

Glueless System Interfaces

The Am29240 microcontroller series also minimizes system cost by providing a glueless attachment to external ROMs, DRAMs, and other peripheral components. Processor outputs have edge-rate control that allows them to drive a wide range of load capacitances with low noise and ringing. This eliminates the cost of external logic and buffering.

Bus- and Software-Compatibility

Compatibility within a processor family is critical for achieving a rational, easy upgrade path. The Am29240 processors are all members of a bus-compatible series of RISC microcontrollers. All members of this family, the Am29205, Am29200, Am29240, Am29245, and Am29243 microcontrollers, allow improvements in price, performance, and system capabilities without requiring that users redesign their system hardware or software. Bus compatibility ensures a convenient upgrade path for future systems.

The Am29240 microcontroller series is available in a 196-pin plastic quad flat-pack (PQFP) package. The Am29240 microcontroller series is signal-compatible with the Am29205 and the Am29200 microcontrollers.

Moreover, the Am29240 microcontroller series is binary compatible with existing RISC microcontrollers and other members of the 29K Family (the Am29000, Am29005, Am29030, Am29035, and Am29050 microprocessors, as well as the Am29205 and Am29200 microcontrollers). The Am29240 microcontroller series provides a migration path to low-cost, high-performance, highly integrated systems from other 29K Family members, without requiring expensive rewrites of application software.

Complete Development and Support Environment

A complete development and support environment is vital for reducing a product's time-to-market. Advanced Micro Devices has created a standard development environment for the 29K Family of processors. In addition, the Fusion29K third-party support organization provides the most comprehensive customer/partner program in the embedded processor market.

Advanced Micro Devices offers a complete set of hardware and software tools for design, integration, debugging, and benchmarking. These tools, which are available now for the 29K Family, include the following:

- High C® 29K optimizing C compiler with assembler, linker, ANSI library functions, and 29K architectural simulator
- XRAY29K™ source-level debugger
- MiniMON29K™ debug monitor
- A complete family of demonstration and development boards

In addition, Advanced Micro Devices has developed a standard host interface (HIF) specification for operating system services, the Universal Debug Interface (UDI) for seamless connection of debuggers to ICEs and target hardware, and extensions for the UNIX common object file format (COFF).

This support is augmented by an engineering hotline, an on-line bulletin board, and field application engineers.

PERFORMANCE OVERVIEW

The Am29240 microcontroller series offers a significant margin of performance over CISC microprocessors in existing embedded designs, since the majority of processor features were defined for the maximum achievable performance at very low cost. This section describes the features of the Am29240 microcontroller series from the point of view of system performance.

Instruction Timing

The Am29240 microcontroller series uses an arithmetic/logic unit, a field shift unit, and a prioritizer to execute most instructions. Each of these is organized to operate on 32-bit operands and provide a 32-bit result. All operations are performed in a single cycle.

The performance degradation of load and store operations is minimized in the Am29240 microcontroller series by overlapping them with instruction execution, by taking advantage of pipelining, by an on-chip data cache, and by organizing the flow of external data into the processor so that the impact of external accesses is minimized.

Pipelining

Instruction operations are overlapped with instruction fetch, instruction decode and operand fetch, instruction execution, and result write-back to the Register File. Pipeline forwarding logic detects pipeline dependencies and routes data as required, avoiding delays that might arise from these dependencies.

Pipeline interlocks are implemented by processor hardware. Except for a few special cases, it is not necessary to rearrange programs to avoid pipeline dependencies, although this is sometimes desirable for performance.

On-Chip Instruction and Data Caches

On chip instruction and data caches satisfy most processor fetches without wait states, even when the processor operates at twice the system frequency. The caches are pipelined for best performance. The reload policies minimize the amount of time spent waiting for reload, while optimizing the benefit of locality of reference.

Burst-Mode and Page-Mode Memories

The Am29240 microcontroller series directly supports burst-mode memories. The burst-mode memory supplies instructions at the maximum bandwidth, without the complexity of an external cache or the performance degradation due to cache misses.

The processor can also use the page-mode capability of common DRAMs to improve the access time in cases where page-mode accesses can be used. This is particularly useful in very low-cost systems with 16-bit-wide DRAMs, where the DRAM must be accessed twice for each 32-bit operand.

Instruction Set Overview

All 29K Family members employ a three-address instruction set architecture. The compiler or assembly-language programmer is given complete freedom to allocate register usage. There are 192 general-purpose registers, allowing the retention of intermediate calculations and avoiding needless data destruction. Instruction operands may be contained in any of the general-purpose registers, and the results may be stored into any of the general-purpose registers.

The Am29240 microcontroller series instruction set contains 117 instructions that are divided into nine classes. These classes are integer arithmetic, compare, logical, shift, data movement, constant, floating point, branch, and miscellaneous. The floating-point instructions are not executed directly, but are emulated by trap handlers.

All directly implemented instructions are capable of executing in one processor cycle, with the exception of interrupt returns, loads, and stores.

Data Formats

The Am29240 microcontroller series defines a word as 32 bits of data, a half-word as 16 bits, and a byte as 8 bits. The hardware provides direct support for word-integer (signed and unsigned), word-logical, word-boolean, half-word integer (signed and unsigned), and character data (signed and unsigned).

Word-boolean data is based on the value contained in the most significant bit of the word. The values TRUE and FALSE are represented by the most significant bit values 1 and 0, respectively.

Other data formats, such as character strings, are supported by instruction sequences. Floating-point formats (single and double precision) are defined for the processor; however, there is no direct hardware support for these formats in the Am29240 microcontroller series.

Protection

The Am29240 microcontroller series offers two mutually exclusive modes of execution, the user and supervisor modes, that restrict or permit accesses to certain processor registers and external storage locations.

The register file may be configured to restrict accesses to supervisor-mode programs on a bank-by-bank basis.

Memory Management Unit

The Am29240 microcontroller series provides a memory-management unit (MMU) for translating virtual addresses into physical addresses. The page size for translation ranges from 1 Kbyte to 16 Mbyte in powers of four. The Am29245 and Am29240 microcontrollers each have a single, 16-entry TLB. The Am29243 microcontroller has dual 16-entry TLBs, each capable of mapping pages of different size.

Interrupts and Traps

When an Am29240 microcontroller series takes an interrupt or trap, it does not automatically save its current state information in memory. This lightweight interrupt and trap facility greatly improves the performance of temporary interruptions such as simple operating-system calls that require no saving of state information.

In cases where the processor state must be saved, the saving and restoring of state information is under the control of software. The methods and data structures used to handle interrupts—and the amount of state saved—may be tailored to the needs of a particular system.

Interrupts and traps are dispatched through a 256-entry vector table that directs the processor to a routine that handles a given interrupt or trap. The vector table may be relocated in memory by the modification of a processor register. There may be multiple vector tables in the system, though only one is active at any given time.

The vector table is a table of pointers to the interrupt and trap handlers, and requires only 1 Kbyte of memory. The processor performs a vector fetch every time an interrupt or trap is taken. The vector fetch requires at least three cycles, in addition to the number of cycles required for the basic memory access.

DEBUGGING AND TESTING

The Am29240 microcontroller series provides debugging and testing features at both the software and hardware levels.

Software debugging is facilitated by the instruction trace facility and instruction breakpoints. Instruction tracing is accomplished by forcing the processor to trap after each instruction has been executed. Instruction breakpoints are implemented by the HALT instruction or by a software trap.

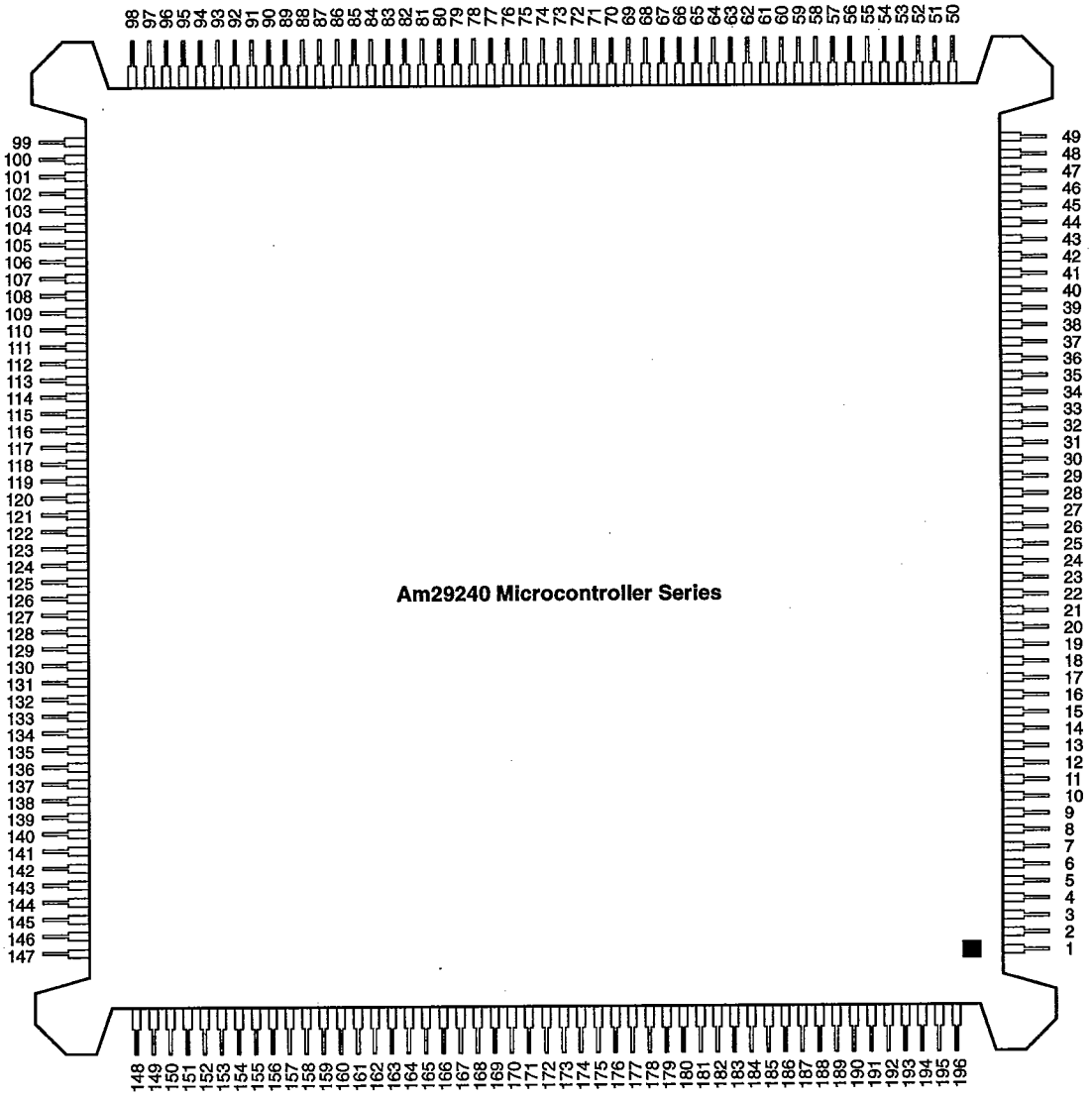
The processor provides several additional features to assist system debugging and testing:

- The Test/Development Interface is composed of a group of pins that indicate the state of the processor and control the operation of the processor.
- A Traceable Cache feature permits a hardware-development system to track accesses to the on-chip caches, permitting a high level of visibility into processor operation.
- An IEEE Std. 1149.1–1990 (JTAG) compliant Standard Test Access Port and Boundary-Scan Architecture. The Test Access Port provides a scan interface for testing processor and system hardware in a production environment, and contains extensions that allow a hardware-development system to control and observe the processor without interposing hardware between the processor and system.

CONNECTION DIAGRAM

Top Side View

196-Pin PQFP (Plastic Quad Flat Pack) Package



Notes: *Pin 1 marked for orientation.*

PQFP PIN DESIGNATION – Sorted by Pin NUMBER

PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME
1	V_{CC}	50	V_{CC}	99	V_{CC}	148	V_{CC}
2	MEMCLK	51	Reserved	100	Reserved	149	Reserved
3	MEMDRV	52	Reserved	101	Reserved	150	PIO12
4	INCLK	53	TXDB[3]	102	A23	151	PIO11
5	ID31	54	RXDB[3]	103	A22	152	PIO10
6	ID30	55	$\overline{DTRA}$	104	A21	153	PIO9
7	ID29	56	RXDA	105	A20	154	PIO8
8	ID28	57	UCLK	106	A19	155	PIO7
9	ID27	58	$\overline{DSRA}$	107	A18	156	PIO6
10	ID26	59	TXDA	108	A17	157	PIO5
11	ID25	60	$\overline{ROMCS3}$	109	A16	158	PIO4
12	ID24	61	$\overline{ROMCS2}$	110	V_{SS}	159	V_{SS}
13	V_{SS}	62	$\overline{ROMCS1}$	111	V_{CC}	160	V_{CC}
14	V_{CC}	63	$\overline{ROMCS0}$	112	A15	161	PIO3
15	ID23	64	V_{CC}	113	A14	162	PIO2
16	ID22	65	V_{SS}	114	A13	163	PIO1
17	ID21	66	$\overline{BURST}$	115	A12	164	PIO0
18	ID20	67	$\overline{RSWE}$	116	A11	165	TDO
19	ID19	68	$\overline{ROMOE}$	117	A10	166	STAT2
20	ID18	69	$\overline{RAS3}$	118	A9	167	STAT1
21	ID17	70	$\overline{RAS2}$	119	A8	168	STAT0
22	ID16	71	$\overline{RAS1}$	120	V_{SS}	169	VDAT[2]
23	V_{SS}	72	$\overline{RAS0}$	121	V_{CC}	170	PSYNC[2]
24	V_{CC}	73	$\overline{CAS3}$	122	A7	171	V_{SS}
25	ID15	74	$\overline{CAS2}$	123	A6	172	V_{CC}
26	ID14	75	V_{CC}	124	A5	173	$\overline{GREQ}$
27	ID13	76	V_{SS}	125	A4	174	DREQB
28	ID12	77	$\overline{CAS1}$	126	A3	175	DREQA
29	ID11	78	$\overline{CAS0}$	127	A2	176	TDMA
30	ID10	79	$\overline{TR/OE}$	128	A1	177	$\overline{TRAP0}$
31	ID9	80	$\overline{WE}$	129	A0	178	$\overline{TRAP1}$
32	ID8	81	$\overline{GACK}$	130	V_{SS}	179	$\overline{INTR0}$
33	V_{SS}	82	$\overline{PIACS5}$	131	V_{CC}	180	$\overline{INTR1}$
34	V_{CC}	83	$\overline{PIACS4}$	132	BOOTW	181	$\overline{INTR2}$
35	ID7	84	$\overline{PIACS3}$	133	$\overline{WAIT}$	182	$\overline{INTR3}$
36	ID6	85	$\overline{PIACS2}$	134	PAUTOFD	183	V_{SS}
37	ID5	86	V_{CC}	135	PSTROBE	184	V_{CC}
38	ID4	87	V_{SS}	136	$\overline{PWE}$	185	$\overline{WARN}$
39	ID3	88	$\overline{PIACS1}$	137	$\overline{POE}$	186	VCLK[2]
40	ID2	89	$\overline{PIACS0}$	138	PACK	187	LSYNC[2]
41	ID1	90	$\overline{PIAWE}$	139	$\overline{PBUSY}$	188	TMS
42	ID0	91	$\overline{PIAOE}$	140	V_{SS}	189	$\overline{TRST}$
43	V_{SS}	92	$R/\overline{W}$	141	V_{CC}	190	TCK
44	V_{CC}	93	$\overline{DACKB}$	142	PIO15	191	TDI
45	IDP3 [1,3]	94	$\overline{DACKA}$	143	PIO14	192	$\overline{RESET}$
46	IDP2 [1,3]	95	$\overline{DACKD}$[3]	144	PIO13	193	CNTL1
47	IDP1 [1,3]	96	$\overline{DACKC}$[3]	145	DREQD[3]	194	CNTL0
48	IDP0 [1,3]	97	Reserved	146	DREQC[3]	195	$\overline{TRIST}$
49	V_{SS}	98	V_{SS}	147	V_{SS}	196	V_{SS}

Notes: All values are typical and preliminary.

1. *Defined as a no-connect on the Am29240 microcontroller.*
2. *Defined as a no-connect on the Am29243 microcontroller.*
3. *Defined as a no-connect on the Am29245 microcontroller.*

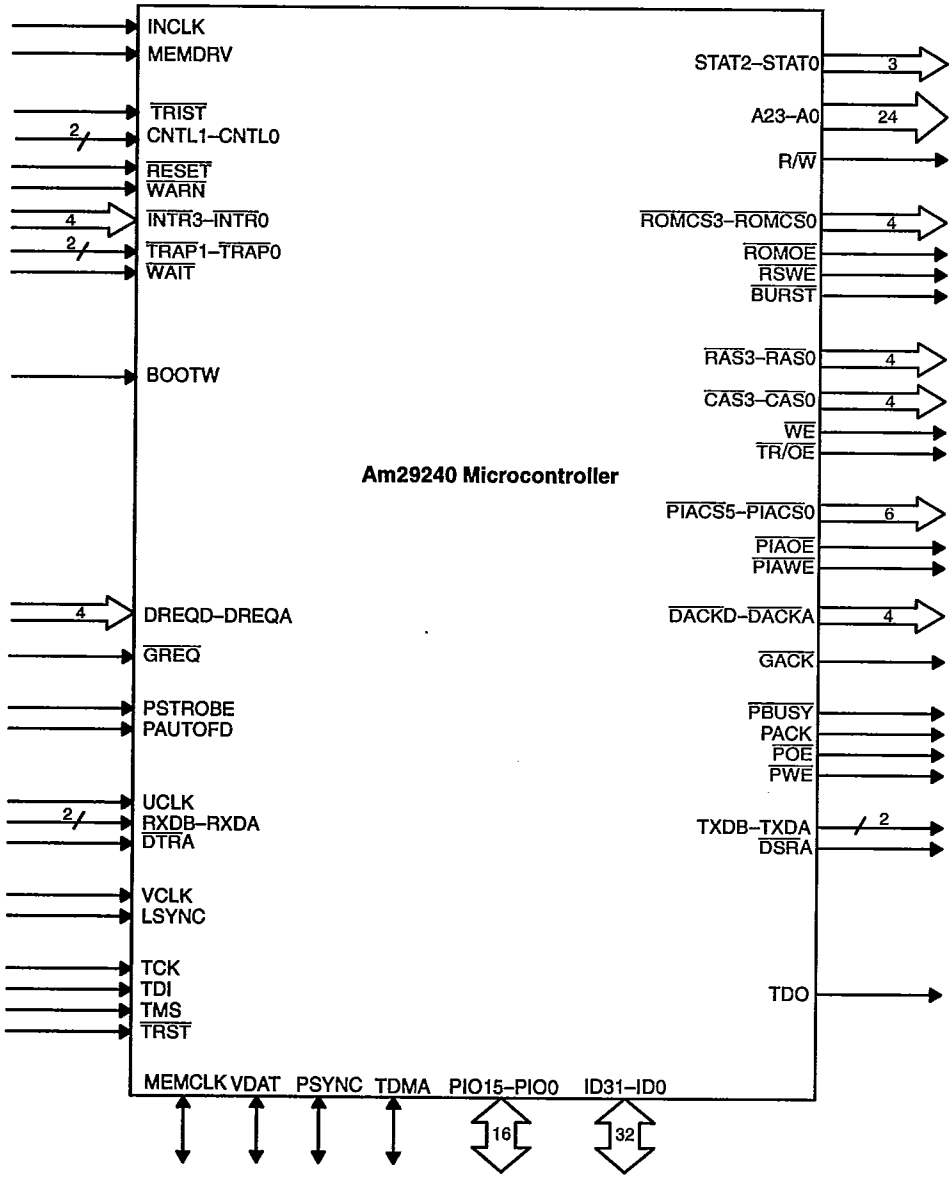
PQFP PIN DESIGNATION – Sorted by Pin NAME

PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.
A0	129	ID5	37	$\overline{\text{PIAWE}}$	90	$\overline{\text{TR/OE}}$	79
A1	128	ID6	36	PIO0	164	$\overline{\text{TRAP0}}$	177
A2	127	ID7	35	PIO1	163	$\overline{\text{TRAP1}}$	178
A3	126	ID8	32	PIO2	162	$\overline{\text{TRIST}}$	195
A4	125	ID9	31	PIO3	161	$\overline{\text{TRST}}$	189
A5	124	ID10	30	PIO4	158	TXDA	59
A6	123	ID11	29	PIO5	157	TXDB[3]	53
A7	122	ID12	28	PIO6	156	UCLK	57
A8	119	ID13	27	PIO7	155	V_{CC}	1
A9	118	ID14	26	PIO8	154	V_{CC}	14
A10	117	ID15	25	PIO9	153	V_{CC}	24
A11	116	ID16	22	PIO10	152	V_{CC}	34
A12	115	ID17	21	PIO11	151	V_{CC}	44
A13	114	ID18	20	PIO12	150	V_{CC}	50
A14	113	ID19	19	PIO13	144	V_{CC}	64
A15	112	ID20	18	PIO14	143	V_{CC}	75
A16	109	ID21	17	PIO15	142	V_{CC}	86
A17	108	ID22	16	$\overline{\text{POE}}$	137	V_{CC}	99
A18	107	ID23	15	PSTROBE	135	V_{CC}	111
A19	106	ID24	12	PSYNC[2]	170	V_{CC}	121
A20	105	ID25	11	$\overline{\text{PWE}}$	136	V_{CC}	131
A21	104	ID26	10	$\overline{\text{RAS0}}$	72	V_{CC}	141
A22	103	ID27	9	$\overline{\text{RAS1}}$	71	V_{CC}	148
A23	102	ID28	8	$\overline{\text{RAS2}}$	70	V_{CC}	160
BOOTW	132	ID29	7	$\overline{\text{RAS3}}$	69	V_{CC}	172
$\overline{\text{BURST}}$	66	ID30	6	Reserved	51	V_{CC}	184
$\overline{\text{CAS0}}$	78	ID31	5	Reserved	52	VCLK[2]	186
$\overline{\text{CAS1}}$	77	IDP0[1,3]	48	Reserved	97	VDAT[2]	169
$\overline{\text{CAS2}}$	74	IDP1[1,3]	47	Reserved	100	V_{SS}	13
$\overline{\text{CAS3}}$	73	IDP2[1,3]	46	Reserved	101	V_{SS}	23
CNTL0	194	IDP3[1,3]	45	Reserved	149	V_{SS}	33
CNTL1	193	INCLK	4	$\overline{\text{RESET}}$	192	V_{SS}	43
$\overline{\text{DACKA}}$	94	$\overline{\text{INTR0}}$	179	$\overline{\text{ROMCS0}}$	63	V_{SS}	49
$\overline{\text{DACKB}}$	93	$\overline{\text{INTR1}}$	180	$\overline{\text{ROMCS1}}$	62	V_{SS}	65
$\overline{\text{DACKC}}$[3]	96	$\overline{\text{INTR2}}$	181	$\overline{\text{ROMCS2}}$	61	V_{SS}	76
$\overline{\text{DACKD}}$[3]	95	$\overline{\text{INTR3}}$	182	$\overline{\text{ROMCS3}}$	60	V_{SS}	87
DREQA	175	LSYNC[2]	187	$\overline{\text{ROMOE}}$	68	V_{SS}	98
DREQB	174	MEMCLK	2	$\overline{\text{RSWE}}$	67	V_{SS}	110
DREQC[3]	146	MEMDRV	3	RXDA	56	V_{SS}	120
DREQD[3]	145	PACK	138	RXDB[3]	54	V_{SS}	130
$\overline{\text{DSRA}}$	58	PAUTOFD	134	R/$\overline{\text{W}}$	92	V_{SS}	140
$\overline{\text{DTRA}}$	55	$\overline{\text{PBUSY}}$	139	STAT0	168	V_{SS}	147
$\overline{\text{GACK}}$	81	$\overline{\text{PIACS0}}$	89	STAT1	167	V_{SS}	159
$\overline{\text{GREQ}}$	173	$\overline{\text{PIACS1}}$	88	STAT2	166	V_{SS}	171
ID0	42	$\overline{\text{PIACS2}}$	85	TCK	190	V_{SS}	183
ID1	41	$\overline{\text{PIACS3}}$	84	TDO	165	V_{SS}	196
ID2	40	$\overline{\text{PIACS4}}$	83	TDI	191	$\overline{\text{WAIT}}$	133
ID3	39	$\overline{\text{PIACS5}}$	82	TDMA	176	$\overline{\text{WARN}}$	185
ID4	38	$\overline{\text{PIAOE}}$	91	TMS	188	$\overline{\text{WE}}$	80

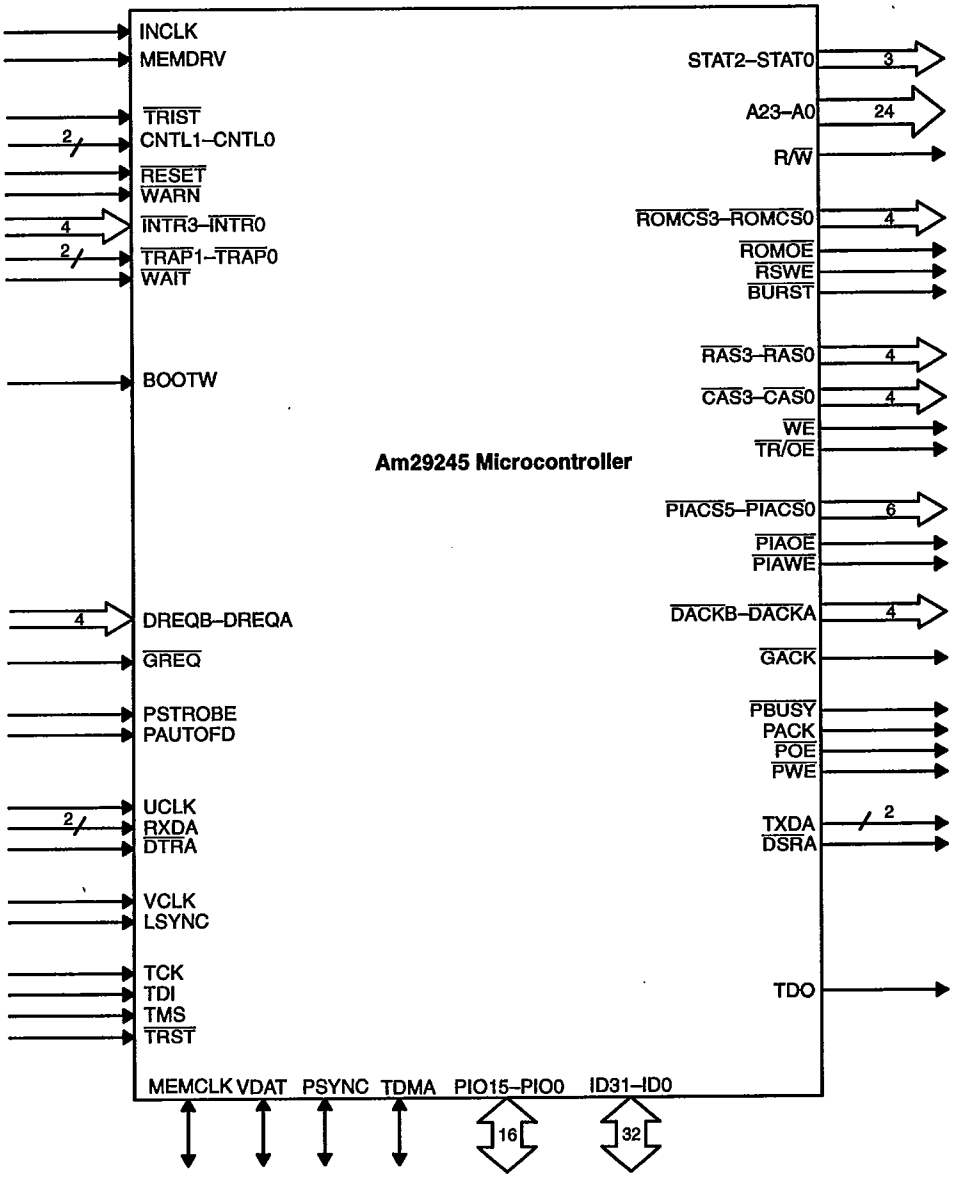
Notes: All values are typical and preliminary.

1. *Defined as a no-connect on the Am29240 microcontroller.*
2. *Defined as a no-connect on the Am29243 microcontroller.*
3. *Defined as a no-connect on the Am29245 microcontroller.*

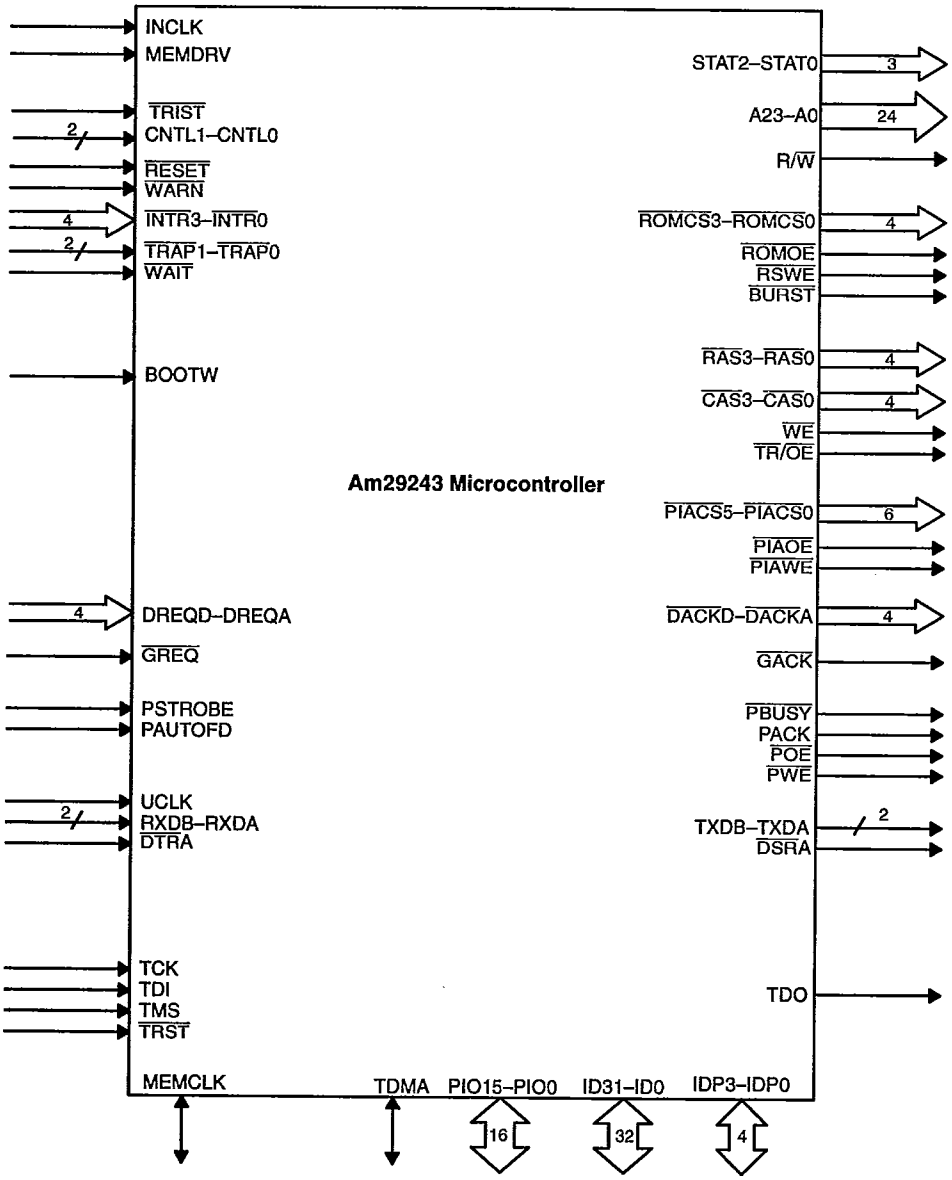
Am29240 MICROCONTROLLER LOGIC SYMBOL



Am29245 MICROCONTROLLER LOGIC SYMBOL



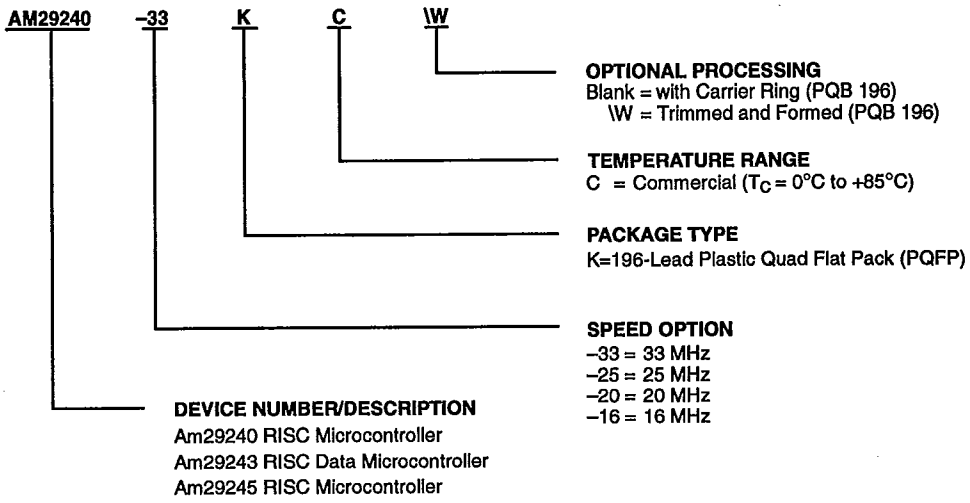
Am29243 MICROCONTROLLER LOGIC SYMBOL



ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. Valid order numbers are formed by a combination of the elements below.



Valid Combinations	
AM29240–20 AM29240–25 AM29240–33	KC, KC\W
AM29243–20 AM29243–25 AM29243–33	KC, KC\W
AM29245–16	KC, KC\W

Valid Combinations

Valid Combinations lists configurations planned to be supported in volume. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD standard military grade products.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... –65°C to +125°C
Voltage on any Pin
with Respect to GND ..... –0.5 V to V_{CC} +0.5 V

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Case Temperature (T_C) ..... 0°C to +85°C
Supply Voltage (V_{CC}) ..... +4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges

Symbol	Parameter Description	Test Conditions	Advance Information		Unit
			Min	Max	
V_{IL}	Input Low Voltage		–0.5	0.8	V
V_{IH}	Input High Voltage		2.4	V_{CC} + 0.5	V
$V_{ILINCLK}$	INCLK Input Low Voltage		–0.5	0.8	V
$V_{IHINCLK}$	INCLK Input High Voltage		2.0	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage for All Outputs except MEMCLK	I_{OL} = 3.2 mA		0.45	V
V_{OH}	Output High Voltage for All Outputs except MEMCLK	I_{OH} = –400 µA	2.4		V
I_{LI}	Input Leakage Current (Note 1)	0.45 V ≤ V_{IN} ≤ V_{CC} –0.45 V		±10 or +10/–200	µA
I_{LO}	Output Leakage Current	0.45 V ≤ V_{OUT} ≤ V_{CC} –0.45 V		±10	µA
I_{CCOP}	Operating Power-Supply Current with respect to MEMCLK	V_{CC} = 5.25 V, Outputs Floating; Holding $\overline{\text{RESET}}$ active at 25 MHz		14	mA/MHz
V_{OLC}	MEMCLK Output Low Voltage	I_{OLC} = 20 mA		0.6	V
V_{OHC}	MEMCLK Output High Voltage	I_{OHC} = –20 mA	V_{CC} –0.6		V
I_{OSGND}	MEMCLK GND Short Circuit Current	V_{CC} = 5.0 V	100		mA
I_{OSVCC}	MEMCLK V_{CC} Short Circuit Current	V_{CC} = 5.0 V	100		mA

Notes: *The Low input leakage current for the inputs* $\overline{\text{CNTL1}}$–$\overline{\text{CNTL0}}$, $\overline{\text{INTR3}}$–$\overline{\text{INTR0}}$, $\overline{\text{TRAP1}}$–$\overline{\text{TRAP0}}$, DREQD–DREQA, TCK, TDI, $\overline{\text{TRST}}$, TMS, $\overline{\text{RESET}}$, $\overline{\text{WARN}}$, $\overline{\text{MEMDRV}}$, $\overline{\text{WAIT}}$, *and* $\overline{\text{TRIST}}$ *is –200 µA. These pins have internal pull-up resistors.*

CAPACITANCE

Symbol	Parameter Description	Test Conditions	Advance Information		Unit
			Min	Max	
C_{IN}	Input Capacitance	fC = 10 MHz		15	pF
C_{INCLK}	INCLK Input Capacitance			15	pF
C_{MEMCLK}	MEMCLK Capacitance			20	pF
C_{OUT}	Output Capacitance			20	pF
$C_{I/O}$	I/O Pin Capacitance			20	pF

Notes: *Limits guaranteed by characterization.*

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges

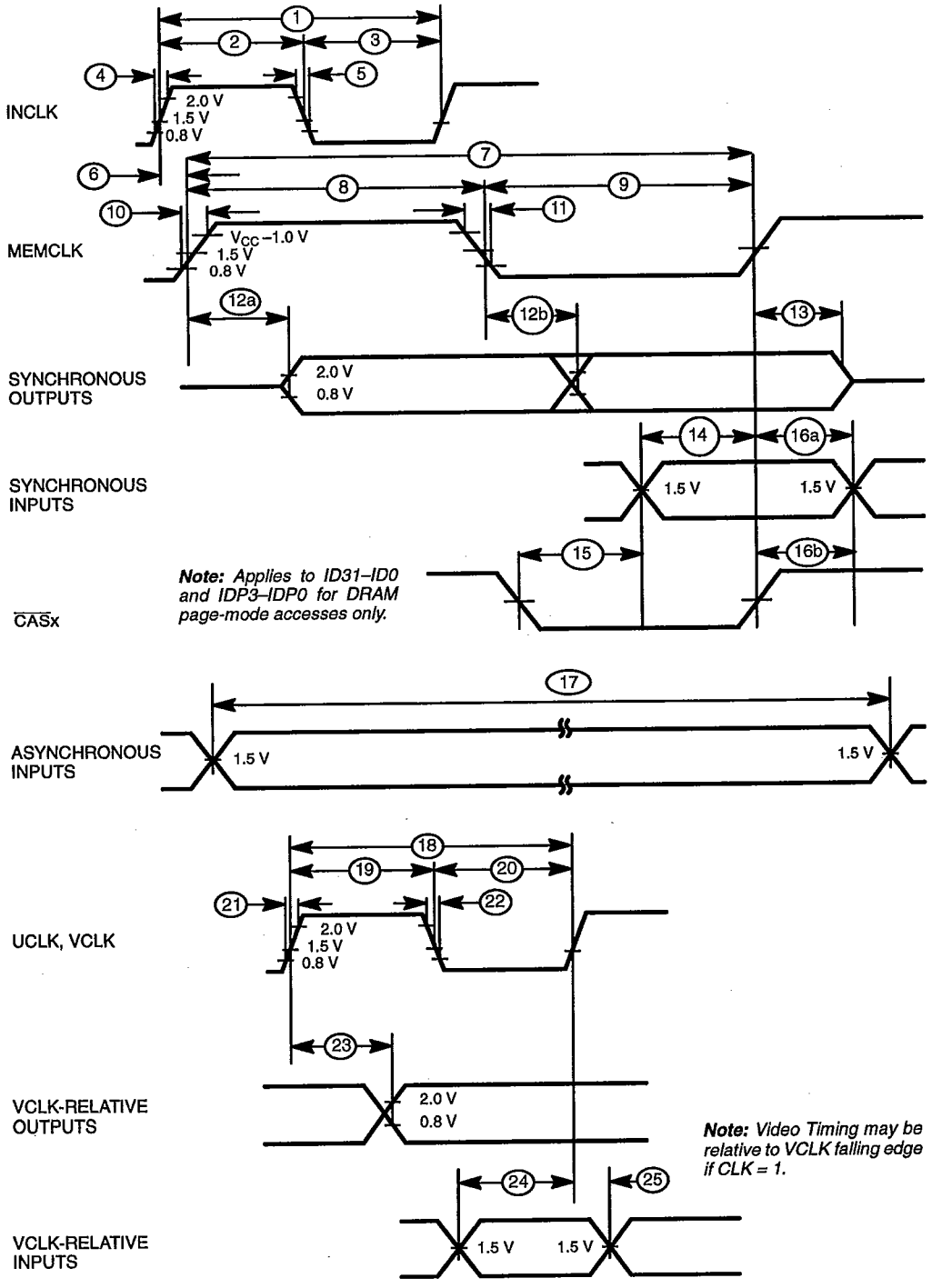
Symbol	Parameter Description	Test Conditions (Note[1])	Advance Information 25 MHz		Unit
			Min	Max	
1	INCLK Period (=0.5T)	Note[2]	20	∞	ns
2	INCLK High Time	Note[2]	6	∞	ns
3	INCLK Low Time	Note[2]	6	∞	ns
4	INCLK Rise Time	Note[2]	0	3	ns
5	INCLK Fall Time	Note[2]	0	3	ns
6	MEMCLK Delay from INCLK	MEMCLK Output[3]	0	5	ns
	MEMCLK Delay (MD) from INCLK	MEMCLK Input	5	10	ns
7	MEMCLK Period (T)	MEMCLK Input	40	∞	ns
8	MEMCLK High Time	MEMCLK Output[3]	0.5T –3	∞	ns
		MEMCLK Input	11	∞	ns
9	MEMCLK Low Time	MEMCLK Output[3]	0.5T –3	∞	ns
		MEMCLK Input	11	∞	ns
10	MEMCLK Rise Time	Note[3]	0	4	ns
11	MEMCLK Fall Time	Note[3]	0	4	ns
12a	Synchronous Output Valid Delay Rise Time from MEMCLK				
	PIO15–PIO0, STAT2–STAT0, and $\overline{\text{PIACS5}}$–$\overline{\text{PIACS0}}$	MEMCLK Output[1A]	1	11	ns
		MEMCLK Input[1A]	1	13+ (MD–5)	ns
	$\overline{\text{RAS3}}$–$\overline{\text{RAS0}}$	MEMCLK Ouput[1B]	1	17	ns
		MEMCLK Input[1B]	1	17+ (MD–5)	ns
	All others	MEMCLK Output[1C]	1	10	ns
		MEMCLK Input[1C]	1	12+ (MD–5)	ns
12b	Synchronous Output Valid Delay Fall Time from MEMCLK				
	PIO15–PIO0, STAT2–STAT0, and $\overline{\text{PIACS5}}$–$\overline{\text{PIACS0}}$	MEMCLK Output[1A]	1	10	ns
		MEMCLK Input[1A]	1	12+ (MD–5)	ns
	$\overline{\text{RAS3}}$–$\overline{\text{RAS0}}$	MEMCLK Output[1B]	1	16	ns
		MEMCLK Input[1B]	1	16+ (MD–5)	ns
	All others	MEMCLK Output[1C]	1	9	ns
		MEMCLK Input[1C]	1	11+ (MD–5)	ns
13	Synchronous Output Disable Delay from MEMCLK Rise	MEMCLK Output	1	10	ns
		MEMCLK Input	1	12+ (MD–5)	ns
14	Synchronous Input Setup Time to MEMCLK		7		ns
15	Available $\overline{\text{CAS}}$ Access Time ($T_{\overline{\text{CAS}}}$–$T_{\text{Setup}}$)	Parity Disabled[4]	0.4T		ns
		Parity Enabled[4]	0.4T –4		ns

Symbol	Parameter Description	Test Conditions (Note[1])	Advance Information 25 MHz		Unit
			Min	Max	
16a	Synchronous Input Hold Time to MEMCLK		0		ns
16b	Synchronous Input Hold Time to $\overline{CAS3}$–$\overline{CAS0}$	Note[4]	3		ns
17	Asynchronous Input Pulse Width				ns
	LSYNC and PSYNC		Note[5]		
	All others		4T		ns
18	UCLK Period	Note[2]	20		ns
	VCLK Period	Note[2]	15		ns
19	UCLK High Time	Note[2]	6		ns
	VCLK High Time	Note[2]	4		ns
20	UCLK Low Time	Note[2]	6		ns
	VCLK Low Time	Note[2]	4		ns
21	UCLK Rise time	Note[2]	0	3	ns
	VCLK Rise time	Note[2]	0	3	ns
22	UCLK Fall Time	Note[2]	0	3	ns
	VCLK Fall Time	Note[2]	0	3	ns
23	Synchronous Output Valid Delay from VCLK Rise and Fall	Note[6]	0	14	ns
24	Input Setup Time to VCLK Rise and Fall	Notes[6,7]	9		ns
25	Input Hold Time to VCLK Rise and Fall	Notes[6,7]	0		ns

Notes:

1. *All outputs driving 80 pF, measured at V_{OL} = 1.5 V and V_{OH} = 1.5 V. For higher capacitance:*
   - *A. Add 1-ns output delay per 15 pF loading up to 150-pF total.*
   - *B. Add 1-ns output delay per 25 pF loading up to 300-pF total. In order to meet the setup time (t_{ASR}) from A23–A0 to $\overline{RAS3}$–$\overline{RAS0}$ for DRAM, the capacitance loading of A23–A0 must not exceed the capacitance loading of $\overline{RAS3}$–$\overline{RAS0}$ by more than 150 pF.*
   - *C. Add 1-ns output delay per 25 pF loading up to 300-pF total.*
2. *INCLK, VCLK, and UCLK can be driven with TTL inputs. UCLK must be tied High if it is unused.*
3. *MEMCLK can drive an external load of 100 pF.*
4. *Applies to ID31–ID0 and IDP3–IDP0 for DRAM page-mode accesses only.*
5. *LSYNC and PSYNC minimum width is two bit-times. A bit-time is one period of the internal video clock, which is determined by the CLKDIV field in the Video Control Register and VCLK.*
6. *Active VCLK edge depends on the CLKI bit in the Video Control Register.*
7. *LSYNC and PSYNC can be treated as synchronous signals by meeting the setup and hold times, though the synchronization delay still applies.*

SWITCHING WAVEFORMS

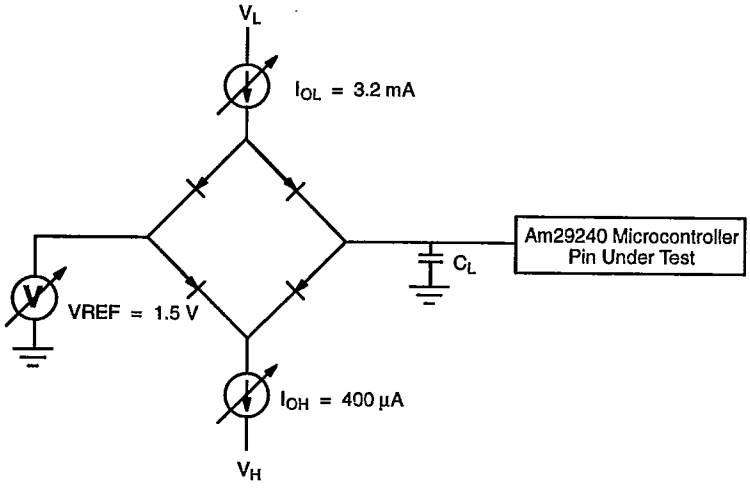


Note: *Applies to ID31–ID0 and IDP3–IDP0 for DRAM page-mode accesses only.*

Note: *Video Timing may be relative to VCLK falling edge if CLK = 1.*

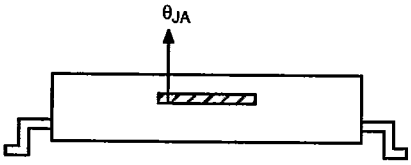
Note: *During AC testing, all inputs are driven at V_{IL} = 0.45 V, V_{IH} = 2.4 V.*

SWITCHING TEST CIRCUIT



THERMAL CHARACTERISTICS

PQFP Package



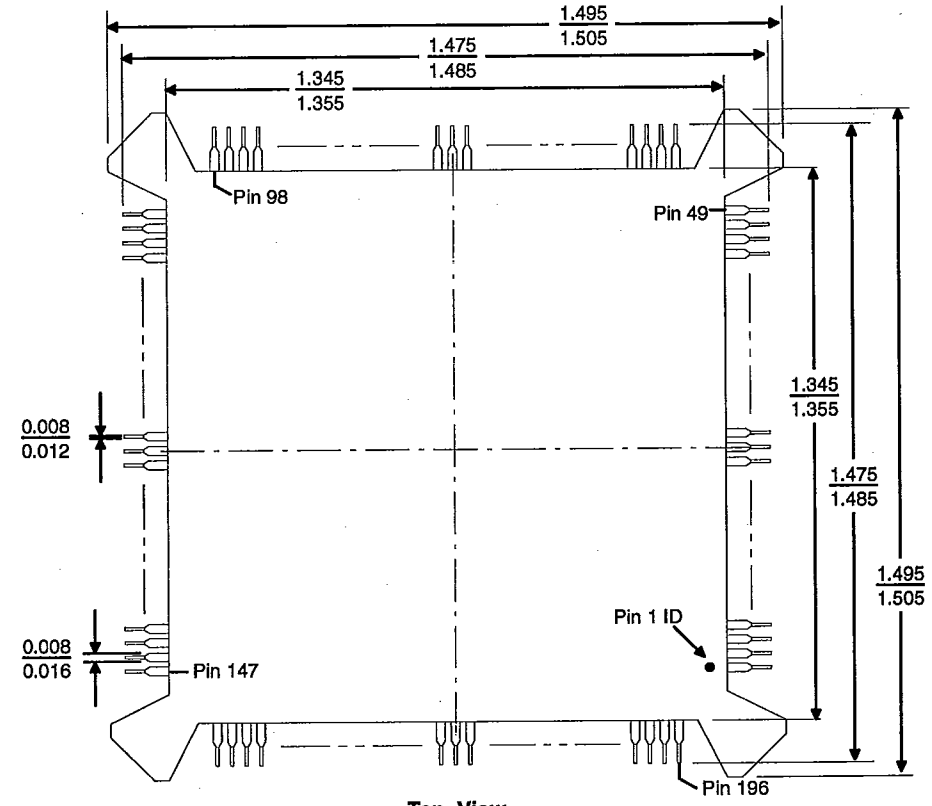
Thermal Resistance – °C/Watt

Parameter	°C/Watt
θ_{JA} Junction-to-Ambient	30
θ_{JC} Junction-to-Case	8
θ_{CA} Case-to-Ambient	22

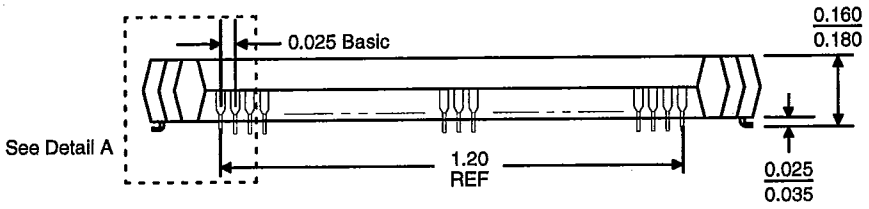
PHYSICAL DIMENSIONS

PQB 196

Plastic Quad Flat Pack; Trimmed and Formed (Measured in inches)



Top View



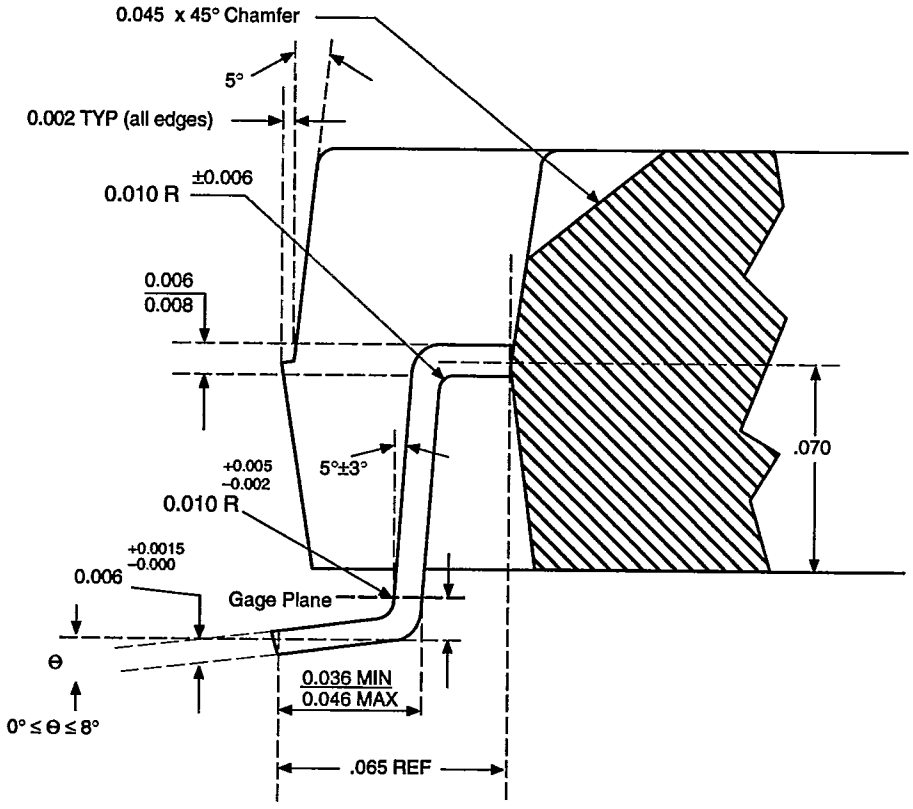
Side View

20012A
CL85
04/9/93 MB

Notes: *For reference only. BSC is an ANSI standard for Basic Space Centering.*

PHYSICAL DIMENSIONS (continued)

PQB 196—Plastic Quad Flat Pack; Trimmed and Formed (continued)



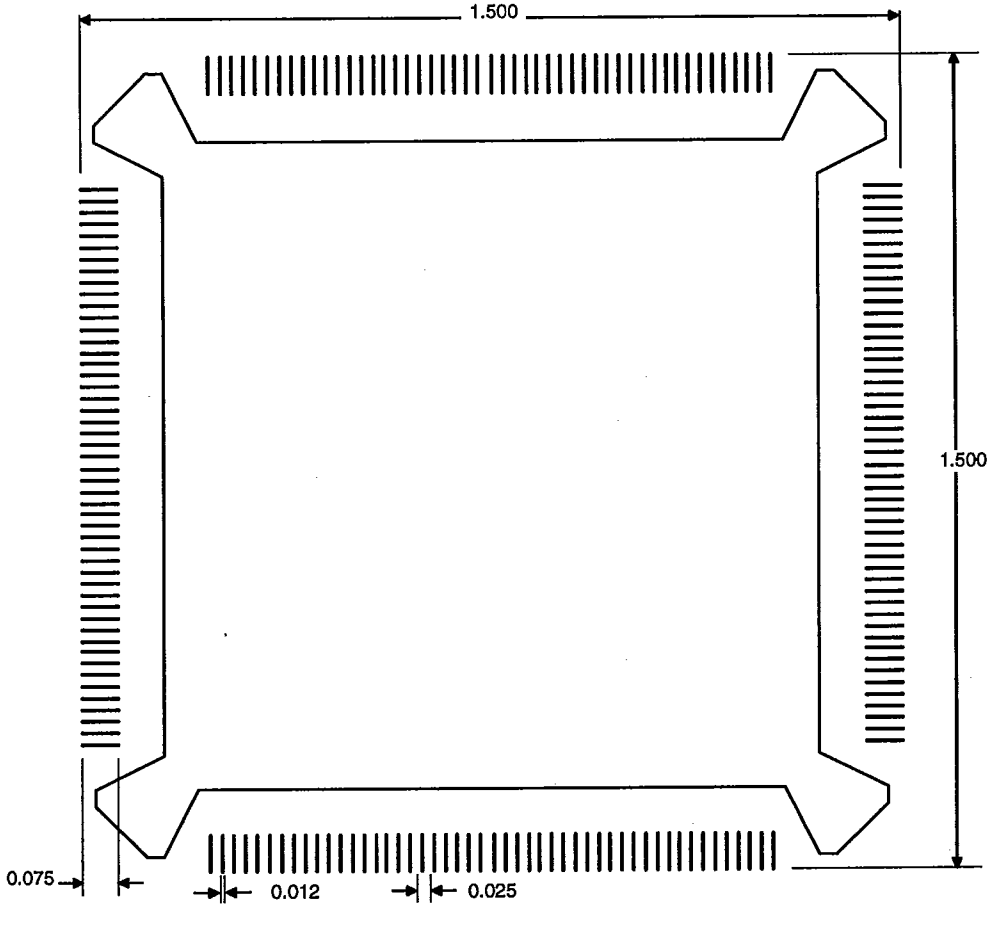
Detail A

Notes:

1. All dimensions are in inches.
2. Dimensions do not include mold protrusion.
3. Coplanarity of all leads will be within 0.004 inches measured from the seating plan. Coplanarity is measured per specification 06–500.
4. Deviation from lead-tip true position shall be within ±0.003 inches.
5. Half span (center of package to lead-tip) shall be within ±0.0085 inches.

PHYSICAL DIMENSIONS (continued)

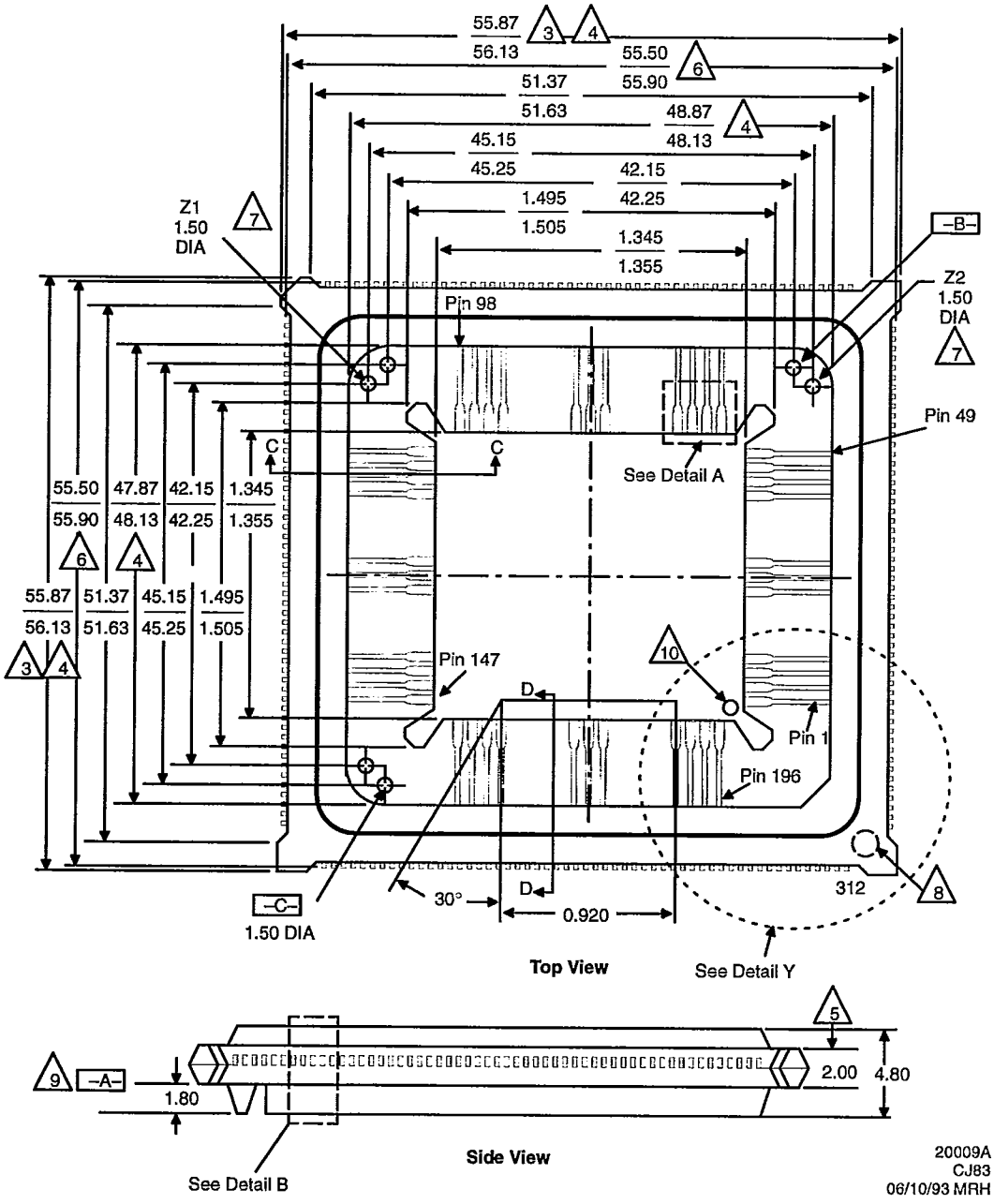
Solder Land Recommendations—196-Lead PQFP



PHYSICAL DIMENSIONS (continued)

PQB 196

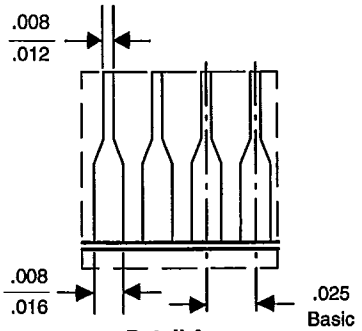
Plastic Quad Flat Pack; Molded Carrier Ring (outer ring measured in millimeters)



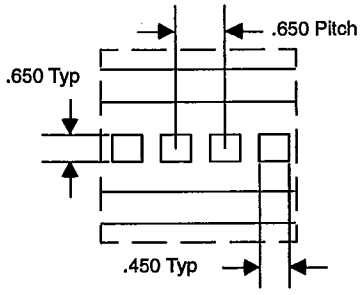
Notes: *For reference only.*

PHYSICAL DIMENSIONS (continued)

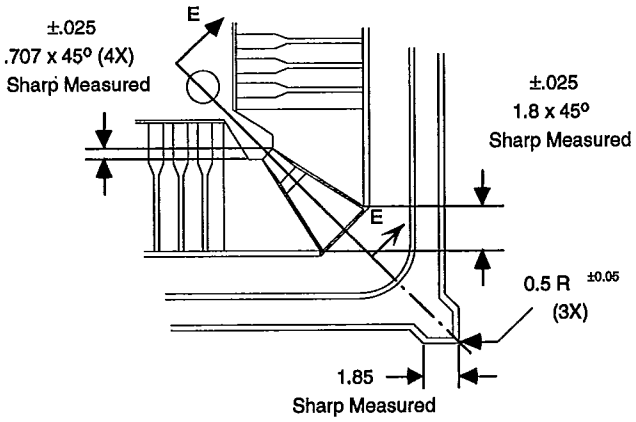
PQB 196—Plastic Quad Flat Pack with Molded Carrier Ring (continued)



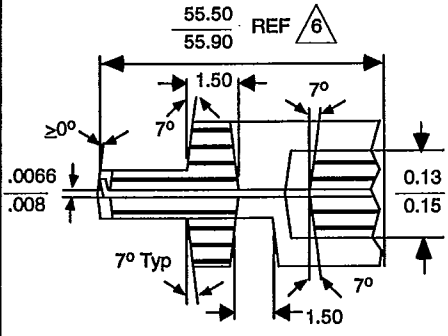
Detail A



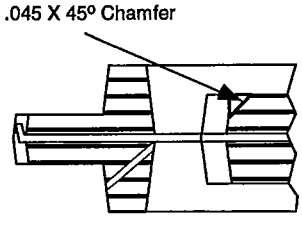
Detail B



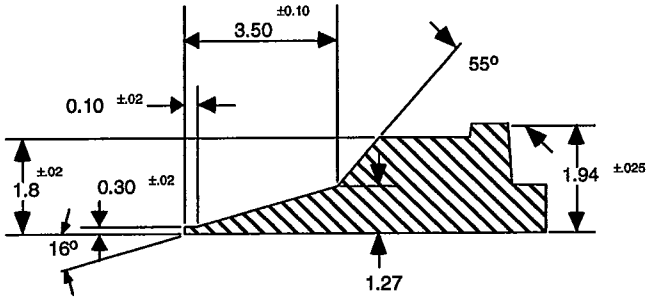
Detail Y



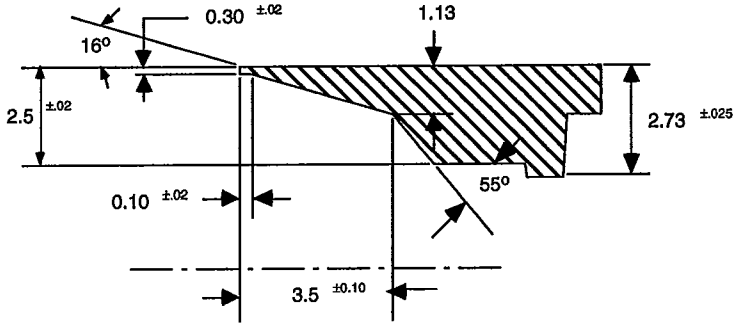
Section C–C



Section D–D



Top Gate



Bottom Gate

Section E–E

PHYSICAL DIMENSIONS (continued)

PQB 196—Plastic Quad Flat Pack with Molded Carrier Ring (continued)

Notes:

1. All dimensions and tolerances conform to ANSI Y14.5M–1982.
2. Controlling dimensions: package is measured in inches and ring is measured in millimeters.
3. These dimensions do not include mold protrusion. Allowable mold protrusion is 0.2 mm per side.
4. These dimensions include mold mismatch and are measured at the parting line.
5. Dimensions are centered about centerline of lead material.
6. These dimensions are from the outside edge to the outside edge of the test points.
7. There are six locating holes in the ring. –B– and –C– datum holes are used for trim form and excise of the molded package only. Holes Z1 and Z2 are used for electrical testing only.
8. This area is reserved for vacuum pickup on each of the four corners of the ring and must be flat within 0.025 mm. No ejector pins in this area.
9. Datum –A– surface for seating in socket applications.
10. Pin one orientation with respect to carrier ring as indicated.