# Am2952-52A/Am2953-53A

Eight-Bit Bidirectional I/O Ports with Handshake



## DISTINCTIVE CHARACTERISTICS

- **Eight-Bit, Bidirectional I/O Port** – Two eight-bit, back-to-back registers store data moving in both directions between two bidirectional busses.
- **Separate Clock, Clock Enable and Three-State Output Enable for Each Register.**
- **24mA Output Current Sink Capability.**
- **Inverting and Non-Inverting Versions** – The Am2952 provides non-inverting data outputs. The Am2953 provides inverting data outputs.
- **24-pin Slim Package**
- **Fast** – The Am2952A and Am2953A will be 25–30% faster than the Am2952 and Am2953.

## GENERAL DESCRIPTION

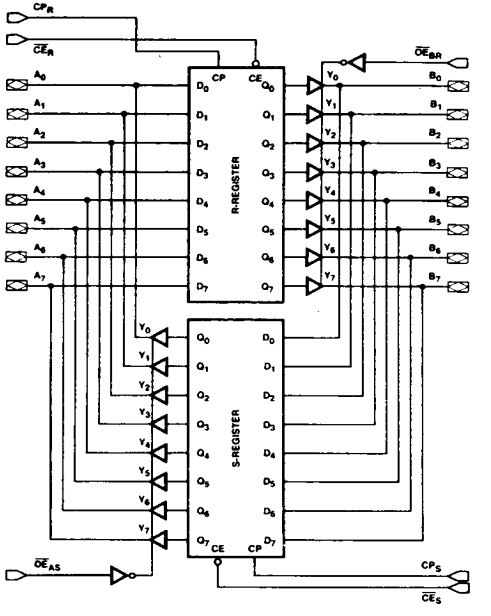
The Am2952 and Am2953, members of Advanced Micro Devices' Am2900 Family, are designed for use as parallel data I/O ports. Two eight-bit, back-to-back registers store data moving in both directions between two bidirectional, 3-state busses. On chip flag flip-flops, set automatically when a register is loaded, provide the handshaking signals required for demand-response data transfer.

Considerable flexibility is designed into the Am2952/Am2953. Separate Clock, Clock Enable and Three-State Output Enable signals are provided for each register, and edge-sensitive clear inputs are provided for each flag flip-flop. A number of these circuits can be used for wider I/O ports. Both inverting and non-inverting versions are available.

24mA output current sink capability, sufficient for most three-state busses, is provided by the Am2952/Am2953.

The Am2952A and Am2953A feature AMD's ion-implanted micro-oxide (IMOX™) processing. They are plug-in replacements for the Am2952 and Am2953 respectively but will be approximately 30% faster.

## BLOCK DIAGRAM




Note: The Am2953 provides inverting data output

IMOX is a trademark of Advanced Micro Devices, Inc.

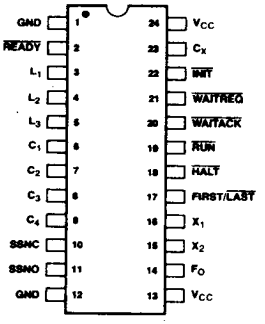
01402B



Refer to Page 13-1 for Essential Information on Military Devices

## CONNECTION DIAGRAM
### Top View

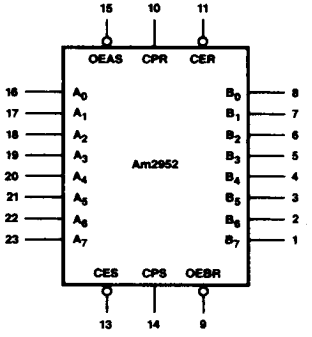
**Am2952**
**D-24-SLIM**




CD004820

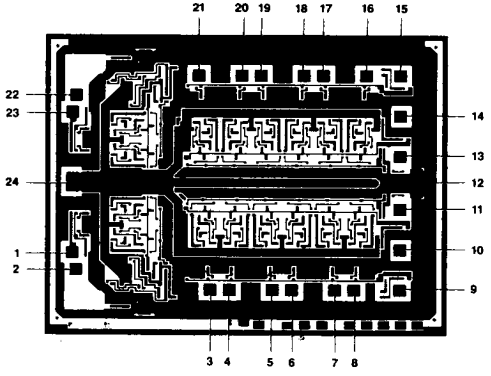
Note: Pin 1 is marked for orientation
$B_i$ is inverted on Am2953

## LOGIC SYMBOL
**Am2952**




LS001140

## METALLIZATION AND PAD LAYOUT




**DIE SIZE 0.107" x 0.138"**

## ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

**Am2952/52A**
**Am2953/53A** D C B

- B — Screening Option
  - Blank – Standard processing
  - B – Burn-in
- C — Temperature (See Operating Range)
  - C – Commercial (0°C to +70°C)
  - M – Military (–55°C to +125°C)
- D — Package
  - D– 24-pin SLIMDIP
  - X– Dice
- Am2952/52A, Am2953/53A — Device type
  - 8-Bit Bidirectional I/O Ports

| Valid Combinations | |
|---|---|
| Am2952/52A | DC, DCB, DMB |
| Am2953/53A | XC, XM |

**Valid Combinations**

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

## PIN DESCRIPTION

| Pin No. | Name | I/O | Description |
|---|---|---|---|
| | A0-7 | I/O | Eight bidirectional lines carrying the R Register inputs or S Register outputs. |
| | B0-7 | I/O | Eight bidirectional lines carrying the S Register inputs or R Register outputs. |
| 10 | CPR | I | The clock for the R Register. When $\overline{CER}$ is LOW, data is entered into the R Register on the LOW-to-HIGH transition of the CPR signal. |
| 11 | $\overline{CER}$ | I | The Clock Enable for the R Register. When $\overline{CER}$ is LOW, data is entered into the R Register on the LOW-to-HIGH transition of the CPR signal. When $\overline{CER}$ is HIGH, the R Register holds its contents, regardless of CPR signal transitions. |
| 9 | $\overline{OEBR}$ | I | The Output Enable for the R Register. When $\overline{OEBR}$ is LOW, the R Register three-state outputs are enabled onto the B0-7 lines. When $\overline{OEBR}$ is HIGH, the R Register outputs are in the high-impedance state. |
| 14 | CPS | I | The clock for the S Register. When $\overline{CES}$ is LOW, data is entered into the S Register on the LOW-to-HIGH transition of the CPS signal. |
| 13 | $\overline{CES}$ | I | The clock enable for the S Register. When $\overline{CES}$ is LOW, data is entered into the S Register on the LOW-to-HIGH transition of the CPS signal. When $\overline{CES}$ is HIGH, the S Register holds its contents, regardless of CPS signal transitions. |
| 15 | $\overline{OEAS}$ | I | The output enable for the S Register. When $\overline{OEAS}$ is LOW, the S Register three-state outputs are enabled onto the A0-7 lines. When $\overline{OEAS}$ is HIGH, the S Register outputs are in the high-impedance state. |

### REGISTER FUNCTION TABLE (Applies to R or S Register)

| Inputs | | | Internal Q | Function |
|---|---|---|---|---|
| D | CP | $\overline{CE}$ | | |
| X | X | H | NC | Hold Data |
| L | ↑ | L | L | Load Data |
| H | ↑ | L | H | |

### OUTPUT CONTROL

| $\overline{OE}$ | Internal Q | Y-Outputs | | Function |
|---|---|---|---|---|
| | | Am2950 | Am2951 | |
| H | X | Z | Z | Disable Outputs |
| L | L | L | H | Enable Outputs |
| L | H | H | L | |

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Ambient Temperature Under Bias ..... −55°C to +125°C
Supply Voltage to Ground Potential
Continuous ..... −0.5V to +7.0V
DC Voltage Applied to Outputs For
High Output State ..... −0.5V to +$V_{CC}$ max
DC Input Voltage ..... −0.5V to +5.5V
DC Output Current, Into Outputs ..... 30mA
DC Input Current ..... −30mA to +5.0mA

*Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.*

## OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

*Operating ranges define those limits over which the functionality of the device is guaranteed.*

## DC CHARACTERISTICS over operating range unless otherwise specified

| Parameters | Description | Test Conditions (Note 1) | | | Min | Typ (Note 2) | Max | Units |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = MIN, $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $A_{0-7}$, $B_{0-7}$ | MIL, $I_{OH}$ = −2mA | 2.4 | 3.4 | | Volts |
| | | | | COM'L, $I_{OL}$ = −6.5mA | 2.4 | 3.4 | | |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = MIN, $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $A_{0-7}$ $B_{0-7}$ | MIL, $I_{OL}$ = 16mA | | | 0.5 | Volts |
| | | | | COM'L, $I_{OL}$ = 24mA | | | 0.5 | |
| $V_{IH}$ | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs | | | 2.0 | | | Volts |
| $V_{IL}$ | Input LOW Level | Guaranteed input logical LOW voltage for all inputs | | | | | 0.8 | Volts |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = MIN, $I_{IN}$ = −18mA | | | | | −1.5 | Volts |
| $I_{IL}$ | Input LOW Current | $V_{CC}$ = MAX, $V_{IN}$ = 0.5V | | $A_{0-7}$, $B_{0-7}$ | | | −250 | μA |
| | | | | Others | | | −360 | μA |
| $I_{IH}$ | Input HIGH Current | $V_{CC}$ = MAX, $V_{IN}$ = 2.7V | | $A_{0-7}$, $B_{0-7}$ | | | 70 | μA |
| | | | | Others | | | 20 | |
| $I_I$ | Input HIGH Current | $V_{CC}$ = MAX, $V_{IN}$ = 5.5V | | | | | 1.0 | mA |
| $I_O$ | Output Off-state Leakage Current | $V_{CC}$ = MAX | $A_{0-7}$, $B_{0-7}$ | $V_O$ = 2.4V | | | 70 | μA |
| | | | | $V_O$ = 0.4V | | | −250 | |
| $I_{SC}$ | Output Short Circuit Current (Note 3) | $V_{CC}$ = MAX | | | −30 | | −85 | mA |
| $I_{CC}$ | Power Supply Current (Notes 4, 5) | $V_{CC}$ = MAX | COM'L | $T_A$ = 0 to +70°C | | | 275 | mA |
| | | | | $T_A$ = +70°C | | | 228 | |
| | | | MIL | $T_C$ = −55 to +125°C | | | 309 | |
| | | | | $T_C$ = +125°C | | | 202 | |

Notes: 1. For conditions shown as MIN or MAX, use the appropriate value specified under Operating Ranges for the applicable device type.
2. Typical limits are at $V_{CC}$ = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. $I_{CC}$ is measured with all inputs at 4.5V and all outputs open.
5. Worst case $I_{CC}$ is at minimum temperature.

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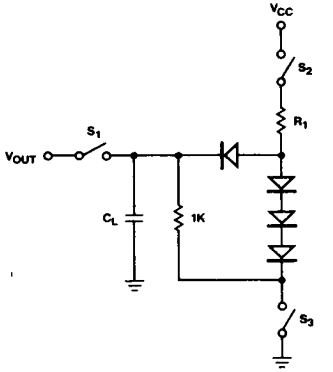
Refer to Page 13-1 for Essential Information on Military Devices

## SWITCHING TEST CIRCUIT

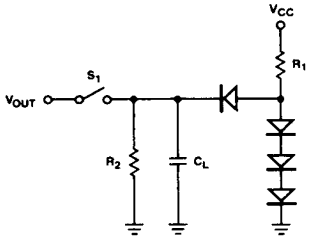
### A. THREE-STATE OUTPUTS




TC001100

$$R_1 = \frac{5.0 - V_{BE} - V_{OL}}{\frac{I_{OL} + V_{OL}}{1K}}$$

### B. NORMAL OUTPUTS




TC001081

$$R_2 = \frac{2.4V}{I_{OH}}$$

$$R_1 = \frac{5.0 - V_{BE} - V_{OL}}{\frac{I_{OL} + V_{OL}}{R_2}}$$

Notes: 1. $C_L$ = 50pF includes scope probe, wiring and stray capacitances without device in test fixture.
2. $S_1$, $S_2$, $S_3$ are closed during function tests and all AC tests except output enable tests.
3. $S_1$ and $S_3$ are closed while $S_2$ is open for $t_{PZH}$ test.
$S_1$ and $S_2$ are closed while $S_3$ is open for $t_{PZL}$ test.
4. $C_L$ = 5.0pF for output disable tests.

### TEST OUTPUT LOADS FOR Am2952/2953

| Pin # (DIP) | Pin Label | Test Circuit | $R_1$ | $R_2$ |
|---|---|---|---|---|
| 16–23 | $A_{0-7}$ | A | 220 | 1K |
| 1–8 | $B_{0-7}$ | A | 220 | 1K |

For additional information on testing, see section "Guidelines on Testing Am2900 Family Devices."

## Notes on Testing

Incoming test procedures on this device should be carefully planned, taking into account the high complexity and power levels of the part. The following notes may be useful:

1. Insure the part is adequately decoupled at the test head. Large changes in $V_{CC}$ current when the device switches may cause erroneous function failures due to $V_{CC}$ changes.
2. Do not leave inputs floating during any tests, as they may start to oscillate at high frequency.
3. Do not attempt to perform threshold tests at high speed. Following an input transition, ground current may change by as much as 400mA in 5–8ns. Inductance in the ground cable may allow the ground pin at the device to rise by 100s of millivolts momentarily.
4. Use extreme care in defining input levels for AC tests. Many inputs may be changed at once, so there will be significant noise at the device pins and they may not actually reach $V_{IL}$ or $V_{IH}$ until the noise has settled. AMD recommends using $V_{IL} \leq 0V$ and $V_{IH} \geq 3.0V$ for AC tests.
5. To simplify failure analysis, programs should be designed to perform DC, Function, and AC tests as three distinct groups of tests.
6. To assist in testing, AMD offers complete documentation on our test procedures and, in most cases, can provide Fairchild Sentry programs, under license.

## Am2952A/Am2953A SWITCHING CHARACTERISTICS

The tables below define the Am2952/Am2953A switching characteristics. Tables A are set-up and hold times relative to a clock LOW-to-HIGH transition. Tables B are propagational delays. Tables C are pulse-width requirements. Tables D are enable/disable times. All measurements are made at 1.5V with input levels at 0V or 3V. All values are in ns with $R_L$ on $A_i$ and $B_i = 220\Omega$ and $R_L$ on FS and FR = 300Ω. $C_L$ = 50pF except output disable times which are specified at $C_L$ = 5pF.

### GUARANTEED CHARACTERISTICS OVER COMMERCIAL OPERATING RANGE

($T_A$ = 0 to +70°C, $V_{CC}$ = 4.75 to 5.25V, $C_L$ = 50pF)

**A. Set-up and Hold Times**

| Input | With Respect To | $t_s$ | $t_h$ |
|---|---|---|---|
| $A_{0-7}$ ⌐ | CPR | | |
| $B_{0-7}$ ⌐ | CPS | | |
| $\overline{CES}$ ⌐ | CPS | | |
| $\overline{CER}$ ⌐ | CPR | | |

**B. Propagation Delays**

| Input | $A_{0-7}$ | $B_{0-7}$ |
|---|---|---|
| CPS ⌐ | | |
| CPR ⌐ | | |

**C. Pulse-Width Requirements**

| Input | Min LOW Pulse Width | Min HIGH Pulse Width |
|---|---|---|
| CPS | | |
| CPR | | |

**D. Enable/Disable Times**

| From | To | Disable | Enable |
|---|---|---|---|
| $\overline{OE}AS$ | $A_{0-7}$ | | |
| $\overline{OE}BR$ | $B_{0-7}$ | | |

### GUARANTEED CHARACTERISTICS OVER COMMERCIAL OPERATING RANGE

($T_C$ = −55 to +125°C, $V_{CC}$ = 4.5 to 5.5V, $C_L$ = 50pF)

**A. Set-up and Hold Times.**

| Input | With Respect To | $t_s$ | $t_h$ |
|---|---|---|---|
| $A_{0-7}$ ⌐ | CPR | | |
| $B_{0-7}$ ⌐ | CPS | | |
| $\overline{CES}$ ⌐ | CPS | | |
| $\overline{CER}$ ⌐ | CPR | | |

**B. Propagation Delays**

| Input | $A_{0-7}$ | $B_{0-7}$ |
|---|---|---|
| CPS ⌐ | | |
| CPR ⌐ | | |

**C. Pulse-Width Requirements**

| Input | Min LOW Pulse Width | Min HIGH Pulse Width |
|---|---|---|
| CPS | | |
| CPR | | |

**D. Enable/Disable Times**

| From | To | Disable | Enable |
|---|---|---|---|
| $\overline{OE}AS$ | $A_{0-7}$ | | |
| $\overline{OE}BR$ | $B_{0-7}$ | | |

## Am2952/Am2953 SWITCHING CHARACTERISTICS

The tables below define the Am2952/Am2953 switching characteristics. Tables A are set-up and hold times relative to a clock LOW-to-HIGH transition. Tables B are propagational delays. Tables C are pulse-width requirements. Tables D are enable/disable times. All measurements are made at 1.5V with input levels at 0V or 3V. All values are in ns with $R_L$ on $A_i$ and $B_i$ = 220Ω and $R_L$ on FS and FR = 300Ω. $C_L$ = 50pF except output disable times which are specified at $C_L$ = 5pF.

### GUARANTEED CHARACTERISTICS OVER COMMERCIAL OPERATING RANGE

($T_A$ = 0 to +70°C, $V_{CC}$ = 4.75 to 5.25V, $C_L$ = 50pF)

**A. Set-up and Hold Times**

| Input | With Respect To | $t_s$ | $t_h$ |
|---|---|---|---|
| $A_{0-7}$ ⌐ | CPR | 7 | 5 |
| $B_{0-7}$ ⌐ | CPS | 7 | 5 |
| $\overline{CES}$ ⌐ | CPS | *19/15 | 4 |
| $\overline{CER}$ ⌐ | CPR | *19/15 | 4 |

**B. Propagation Delays**

| Input | $A_{0-7}$ | $B_{0-7}$ |
|---|---|---|
| CPS ⌐ | *30/26 | – |
| CPR ⌐ | – | *30/26 |

**C. Pulse-Width Requirements**

| Input | Min LOW Pulse Width | Min HIGH Pulse Width |
|---|---|---|
| CPS | 20 | 20 |
| CPR | 20 | 20 |

**D. Enable/Disable Times**

| From | To | Disable | Enable |
|---|---|---|---|
| $\overline{OE}AS$ | $A_{0-7}$ | 22 | 27 |
| $\overline{OE}BR$ | $B_{0-7}$ | 22 | 27 |

*Where two numbers appear, the first is the Am2952 spec, the second is the Am2953 spec.

### GUARANTEED CHARACTERISTICS OVER MILITARY OPERATING RANGE

($T_C$ = −55 to +125°C, $V_{CC}$ = 4.5 to 5.5V, $C_L$ = 50pF)

**A. Set-up and Hold Times**

| Input | With Respect To | $t_s$ | $t_h$ |
|---|---|---|---|
| $A_{0-7}$ ⌐ | CPR | 11 | 8 |
| $B_{0-7}$ ⌐ | CPS | 11 | 8 |
| $\overline{CES}$ ⌐ | CPS | *20/15 | 4 |
| $\overline{CER}$ ⌐ | CPR | *20/15 | 4 |

**B. Propagation Delays**

| Input | $A_{0-7}$ | $B_{0-7}$ |
|---|---|---|
| CPS ⌐ | *35/28 | – |
| CPR ⌐ | – | *35/28 |

**C. Pulse-Width Requirements**

| Input | Min LOW Pulse Width | Min HIGH Pulse Width |
|---|---|---|
| CPS | 20 | 20 |
| CPR | 20 | 20 |

**D. Enable/Disable Times**

| From | To | Disable | Enable |
|---|---|---|---|
| $\overline{OE}AS$ | $A_{0-7}$ | 24 | 28 |
| $\overline{OE}BR$ | $B_{0-7}$ | 24 | 28 |

*Where two numbers appear, the first is the Am2952 spec, the second is the Am2953 spec.

# Am2954/Am2955

Octal Registers with Three-State Outputs

## DISTINCTIVE CHARACTERISTICS

- Eight-bit, high-speed parallel registers
- Am2954 has non-inverting inputs; Am2955 has inverting inputs
- Positive, edge-triggered, D-type flip-flops
- Buffered common clock and buffered common three-state control
- $V_{OL}$ = 0.5V (max) at $I_{OL}$ = 32mA
- High-speed — Clock to output 11 ns typical

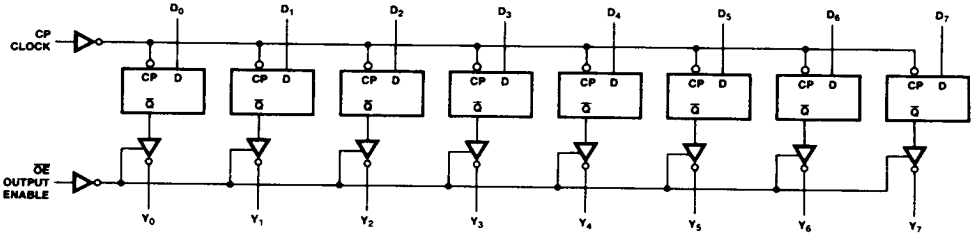
## GENERAL DESCRIPTION

The Am2954 and Am2955 are 8-bit registers built using high-speed Schottky technology. The registers consist of eight D-type flip-flops with a buffered common clock and a buffered 3-state output control. When the output enable ($\overline{OE}$) input is LOW, the eight outputs are enabled. When the $\overline{OE}$ input is HIGH, the outputs are in the 3-state condition.

Input data meeting the set-up and hold time requirements of the D inputs is transferred to the Y outputs on the LOW-to-HIGH transition of the clock input.

The devices are packaged in a space-saving (0.3-inch row spacing) 20-pin package.

## BLOCK DIAGRAM




BD002440

Inputs $D_0$ through $D_7$ are inverted on the Am2955.

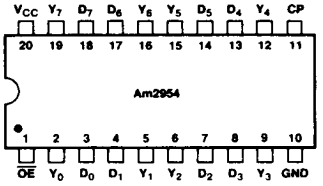
## RELATED PRODUCTS

| Part No. | Description |
|---|---|
| Am29821-26 | 8, 9, 10-Bit Registers |
| Am2918 | Quad D-Register |
| Am2920 | Quad D-Type Flip-Flop |

03603B

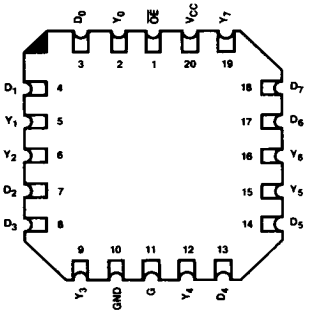
## CONNECTION DIAGRAM
Top View

**D-20, P-20, F-20***




CD004780

**L-20-1**

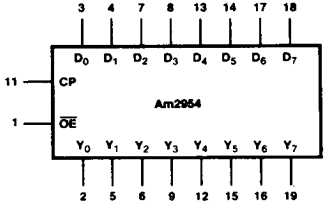



CD004580

Note: Pin 1 is marked for orientation

*F-20 pin configuration identical to D-20, P-20.

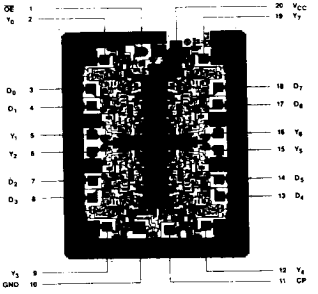
## LOGIC SYMBOL




LS000970

**Note: Inputs $D_0$ through $D_7$ are inverted on the Am2955**

## METALLIZATION AND PAD LAYOUT
**Am2954**



**DIE SIZE 0.085" x 0.110"**

## ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

**Am2954/2955** **D** **C** **B**

- Screening Option
  - Blank – Standard processing
  - B – Burn-in
- Temperature (See Operating Range)
  - C – Commercial (0°C to +70°C)
  - M – Military (–55°C to +125°C)
- Package
  - D – 20-pin CERDIP
  - F – 20-pin flatpak
  - L – 20-pin leadless chip carrier
  - P – 20-pin plastic DIP
  - X – Dice
- Device type
  - Octal Registers

| Valid Combinations | |
|---|---|
| Am2954<br>Am2955 | PC<br>DC, DCB, DM, DMB<br>FM, FMB<br>LC, LCB, LM, LMB<br>XC, XM |

**Valid Combinations**

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

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Refer to Page 13-1 for Essential Information on Military Devices

## PIN DESCRIPTION

| Pin No. | Name | I/O | Description |
|---|---|---|---|
| | $D_I/\overline{D_I}$ | I | The D flip-flop data inputs (Am2954, non-inverting/Am2955, inverting). |
| 11 | CP | I | Clock Pulse for the register. Enters data on the LOW-to-HIGH transition. |
| | $Y_I$ | O | The register three-state outputs. |
| 1 | $\overline{OE}$ | I | Output Control. An active-LOW three-state control used to enable the outputs. A HIGH level input forces the outputs to the high impedance (off) state. |

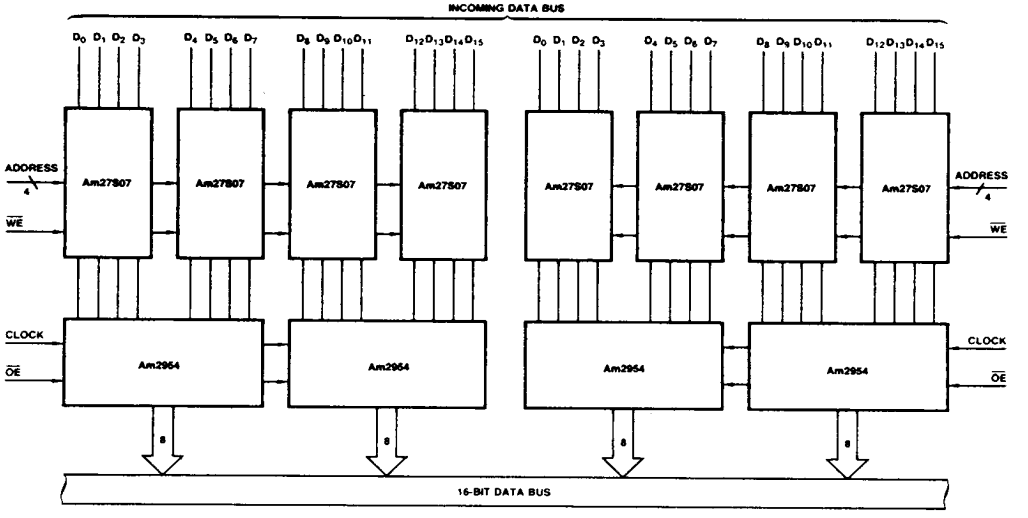
## FUNCTION TABLE

| Function | Inputs | | | | Internal | Outputs |
|---|---|---|---|---|---|---|
| | $\overline{OE}$ | Clock | Am2954 $D_I$ | Am2955 $D_I$ | $Q_I$ | $Y_I$ |
| $H_i$-Z | H | L | X | X | NC | Z |
| | H | H | X | X | NC | Z |
| LOAD REGISTER | L | ↑ | L | H | L | L |
| | L | ↑ | H | L | H | H |
| | H | ↑ | L | H | L | Z |
| | H | ↑ | H | L | H | Z |

H = HIGH
L = LOW
X = Don't Care

NC = No Change
Z = High Impedance
↑ = LOW-to-HIGH transition

## APPLICATION




AF001870

Dual 16-word by 16-bit non-inverting high-speed data buffer.

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Ambient Temperature Under Bias ..... −55°C to +125°C
Supply Voltage to Ground Potential
(Pin 16 to Pin 8) Continuous ..... −0.5V to +7.0V
DC Voltage Applied to Outputs For
High Output State ..... −0.5V to +$V_{CC}$ max
DC Input Voltage ..... −0.5V to +5.5V
DC Output Current, Into Outputs ..... 30mA
DC Input Current ..... −30 to +5.0mA

*Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.*

## OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

*Operating ranges define those limits over which the functionality of the device is guaranteed.*

## DC CHARACTERISTICS over operating range unless otherwise specified

| Parameters | Description | Test Conditions (Note 1) | | Min | Typ (Note 2) | Max | Units |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = MIN, $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | MIL., $I_{OH}$ = −2.0mA | 2.4 | 3.4 | | Volts |
| | | | COM'L, $I_{OH}$ = −6.5mA | 2.4 | 3.1 | | |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = MIN, $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $I_{OL}$ = 20mA | | | .45 | Volts |
| | | | $I_{OL}$ = 32mA | | | .5 | |
| $V_{IN}$ | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs | | 2.0 | | | Volts |
| $V_{IL}$ | Input LOW Level | Guaranteed input logical LOW voltage for all inputs | | | | 0.8 | Volts |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = MIN, $I_{IN}$ = −18mA | | | | −1.2 | Volts |
| $I_{IL}$ | Input LOW Current | $V_{CC}$ = MAX, $V_{IN}$ = 0.5V | | | | −250 | μA |
| $I_{IN}$ | Input HIGH Current | $V_{CC}$ = MAX, $V_{IN}$ = 2.7V | | | | 50 | μA |
| $I_I$ | Input HIGH Current | $V_{CC}$ = MAX, $V_{IN}$ = 5.5V | | | | 1.0 | mA |
| $I_{OZ}$ | Off-State (High-Impedance) Output Current | $V_{CC}$ = MAX | $V_O$ = 0.5V | | | −50 | μA |
| | | | $V_O$ = 2.4V | | | 50 | |
| $I_{SC}$ | Output Short Circuit Current (Note 3) | $V_{CC}$ = MAX | | −40 | | −100 | mA |
| $I_{CC}$ | Power Supply Current (Note 4) | $V_{CC}$ = MAX | | | 90 | 140 | mA |

Notes: 1. For conditions shown as MIN or MAX use the appropriate value specified under Operating Ranges for the applicable device type.
2. Typical limits are at $V_{CC}$ = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. Am2954 measured at CLK = LOW-to-HIGH, $\overline{OE}$ = HIGH and all data inputs are LOW.
Am2955 measured at CLK = LOW-to-HIGH, $\overline{OE}$ = HIGH, and all data inputs are $\overline{OE}$ = HIGH, and all data inputs are LOW.

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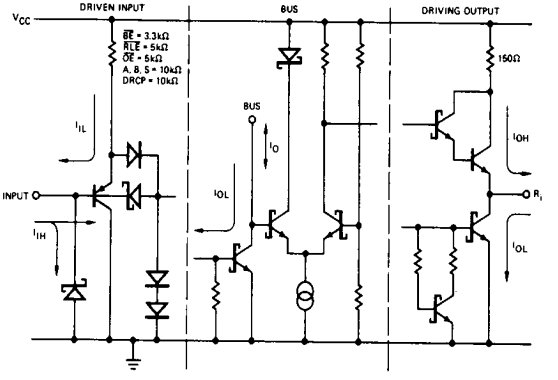
Refer to Page 13-1 for Essential Information on Military Devices

## SWITCHING CHARACTERISTICS ($T_A$ = +25°C, $V_{CC}$ = 5.0V)

| Parameters | Description | | Test Conditions | Am2954 / Am2955 Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Clock to Output, $Y_i$ | | $C_L$ = 15pF, $R_L$ = 280Ω | | 8 | 15 | ns |
| $t_{PHL}$ | | | | | 11 | 17 | ns |
| $t_{ZH}$ | $\overline{OE}$ to $Y_i$ | | | | 8 | 15 | ns |
| $t_{ZL}$ | | | | | 11 | 18 | ns |
| $t_{HZ}$ | $\overline{OE}$ to $Y_i$ | | $C_L$=5pF, $R_L$ = 280Ω | | 5 | 9 | ns |
| $t_{LZ}$ | | | | | 7 | 12 | ns |
| $t_{PW}$ | Clock Pulse Width | HIGH | $C_L$ = 15pF, $R_L$ = 280Ω | 6 | | | ns |
| | | LOW | | 7.3 | | | ns |
| $t_S$ | Data to Clock | | | 5 | | | ns |
| $t_H$ | | | | 2 | | | ns |
| $f_{max}$ | Maximum Clock Frequency (Note 1) | | | 75 | 100 | | MHz |

Note: 1. Per industry convention, $f_{max}$ is the worst case value of the maximum device operating frequency with no constraints on $t_r$, $t_f$, pulse width or duty cycle.

## INPUT/OUTPUT CURRENT INTERFACE CONDITIONS

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Note: Actual current flow direction shown.