Am2961/Am2962

4-Bit Error Correction Multiple Bus Buffers

DISTINCTIVE CHARACTERISTICS

- Provides complete data path interface between the Am2960 Error Detection and Correction Unit, the system data bus and dynamic RAM memory
- Three-state 24mA output to data bus
- Three-state data output to memory
- Inverting data bus for Am2961 and noninverting for Am2962
- Data bus latches allow operation with multiplexed buses
- Space saving 24-pin 0.3" package

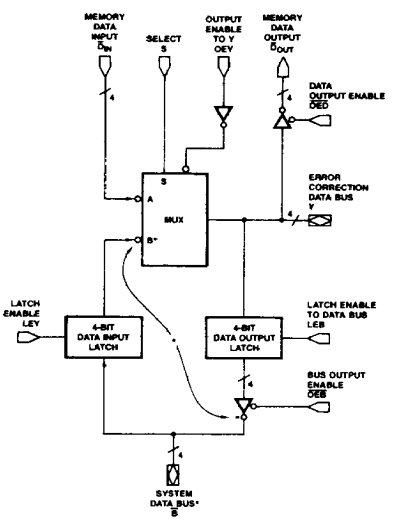
GENERAL DESCRIPTION

The Am2961 and Am2962 are high-performance, low-power Schottky multiple bus buffers that provide the complete data path interface between the Am2960 Error Detection and Correction Unit, dynamic RAM memory and the system data bus. The Am2961 provides an inverting data path between the data bus (B_i) and the Am2960 error correction data input (Y_i) and the Am2962 provides a noninverting configuration (B_i to Y_i). Both devices provide inverting data paths between the Am2960 and memory data bus, thereby optimizing internal data path speeds.

The Am2961 and Am2962 are 4-bit devices. Four devices are used to interface each 16-bit Am2960 Error Detection and Correction Unit with dynamic memory. The system can easily be expanded to 32 or more bits for wider memory applications. The 4-bit configuration allows enabling the appropriate devices two-at-a-time for intermixed word or byte, read and write in 16-bit systems with error correction.

Data latches between the error correction data bus and the system data bus facilitate byte writing in memory systems wider than 8-bits. They also provide a data holding capability during single-step system operation.

BLOCK DIAGRAM



BD001170

*Am2962 is the same function but noninverting to the system data bus, B.

ADVANCED INFORMATION

- 25 – 30% speed improvement plug-in replacements for Am2961/ Am2962.

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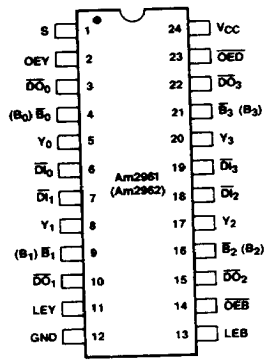
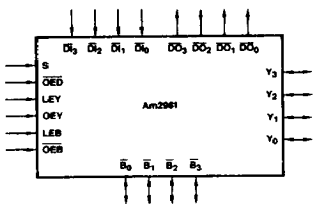
CONNECTION DIAGRAM
Top View
D-24-SLIM



CD001430

LOGIC SYMBOL



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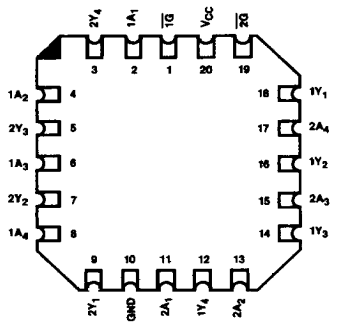
CONNECTION DIAGRAM
Leadless Chip Carrier
L-28-1



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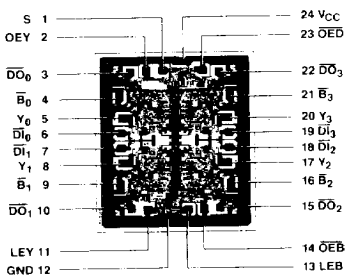
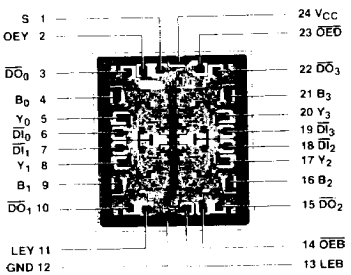
Note: Pin 1 is marked for orientation. B-Bus is noninverting for Am2962.

METALLIZATION AND PAD LAYOUT

Am2961



Am2962



DIE SIZES .102" x .087"

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

Am2961
Am2962

D — Package
D– 24-pin CERDIP (D-24-SLIM)
L – 28-pin leadless chip carrier (L-28-1)

C — Temperature (See Operating Range)
C – Commercial (0°C to +70°C)
M – Military (–55°C to +125°C)

B — Screening Option
Blank – Standard processing
B – Burn-in

Device type
4-Bit Error Correction Multiple Bus Buffers

Valid Combinations	
Am2961 Am2962	DC, DCB, DM, DMB LC, LCB, LM, LMB XC, XM

Valid Combinations

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

PIN DESCRIPTION

Pin No.	Name	I/O	Description
4,9, 16,21	B_0, B_1, B_2, B_3	I/O	The four bidirectional system data bus inputs/outputs. The B-to-Y path is inverting for the Am2961 ($\overline{B}_i$) and noninverting for the Am2962 (B_i).
14	$\overline{OEB}$	I	The three-state Output Enable for the system data bus output drivers. When $\overline{OEB}$ is LOW, data from the Data Output Latch is output to the system data bus. When $\overline{OEB}$ is HIGH, the bus drivers are in the high-impedance state and the Data Input Latch can receive input data from the system data bus.
13	LEB	I	Latch Enable for the Data Output Latch. When LEB is HIGH, the latch is transparent and Y–Bus data is output to the B-Bus. When LEB goes LOW, Y-Bus data meeting the latch set-up and hold time requirements is latched for output to the B-Bus.
5, 8, 17, 20	Y_0, Y_1, Y_2, Y_3	I/O	The four bidirectional EDC data inputs/outputs for connection to the EDC data I/O port.
11	LEY	I	The Latch Enable control for the Data Input Latch for the data input from the system data bus (B). When LEY is HIGH the latch is transparent and B input data is available at the MUX input for selection to the Y outputs. When LEY goes LOW, B input data meeting the latch set-up and hold time requirements is latched for subsequent selection to the Y outputs.
2	OEY	I	Output Enable for the Y (EDC) Bus outputs. When OEY is HIGH, data selected by the input data multiplexer is output to the Y-bus. When OEY is LOW, the MUX output is in the high-impedance state and the Y-Bus can receive input data from the EDC Unit.
1	S	I	The Select input for the input data multiplexer. A LOW input selects data from the memory data input, $\overline{DI}$, for output to the EDC bus (Y). A HIGH input selects data from the system data bus Data Input Latch (B or $\overline{B}$).
3, 10, 15, 22	$\overline{DO}_0$, $\overline{DO}_1$, $\overline{DO}_2$, $\overline{DO}_3$	O	The Data Outputs to the memory data inputs. The $\overline{DO}$ outputs are inverted with respect to the EDC Bus (Y). These outputs are "RAM Driver" outputs with a collector resistor in the lower output driver to protect against undershoot on the HIGH-to-LOW transition.
23	$\overline{OED}$	I	Output Enable for the $\overline{DO}$ outputs. An active LOW input causes the $\overline{DO}$ outputs to output inverted data from the EDC (Y) Bus and a HIGH input puts the $\overline{DO}$ outputs in the high-impedance state.
6, 7, 18, 19	$\overline{DI}_0$, $\overline{DI}_1$, $\overline{DI}_2$, $\overline{DI}_3$	I	The Data Inputs from memory. $\overline{DI}$ inputs are selected by the data input MUX for output to the EDC (Y) Bus (controlled by S and OEY) and/or output to the system data bus (B) (controlled by LEB and $\overline{OEB}$).

FUNCTION TABLES

Y-BUS OUTPUT

LEY	$\overline{DI}_i$	$\overline{B}_i$* Am2961	B_i* Am2962	S	OEY	Y
X	X	X	X	X	L	Z
X	L	X	X	L	H	H
X	H	X	X	L	H	L
H	X	L	H	H	H	H
H	X	H	L	H	H	L
L	X	X	X	H	H	NC

*$\overline{OEB}$ = HIGH for B data input

B-BUS OUTPUT

Y* Input	LEB	$\overline{OEB}$	$\overline{B}$ Am2961	B Am2962
X	X	H	Z	Z
L	H	L	H	L
H	H	L	L	H
X	L	L	NC	NC

*OEY = LOW for B data input

$\overline{DO}$ PORT OUTPUT

Y	$\overline{OED}$	$\overline{DO}$
X	H	Z
L	L	H
H	L	L

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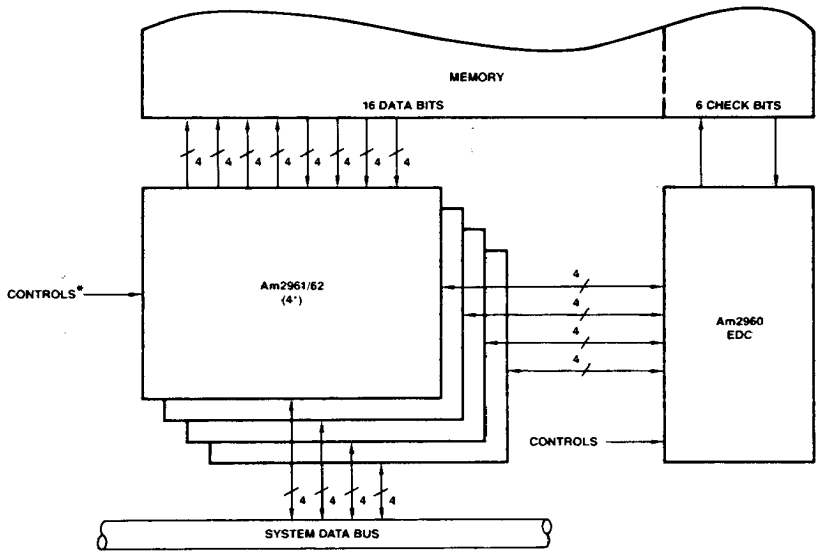
APPLICATION



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*Since the EDC Data Bus Buffers are four-bit wide devices, controls can be paired to device inputs to provide byte level controls (for any data width).

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Ambient Temperature Under Bias
Power Applied ..... −55°C to +125°C
Supply Voltage to Ground Potential
Continous ..... −0.5V to +7.0V
DC Voltage Applied to Outputs For
High Output State ..... −0.5V to V_{CC} Max
DC Input Voltage 5.5V
DC Output Current, Into Outputs 30mA
DC Input Current ..... −30mA to +5.0mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS OVER OPERATING RANGE – Y BUS

Parameters	Descriptions	Test Conditions (Note 1)		Min	Typ (Note 2)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OH} = −3.0mA	2.4	3.4		Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 8mA		0.3	0.45	Volts
			I_{OL} = 16mA		0.35	0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs	MIL			0.7	Volts
			COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA				−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.4V	OEY = LOW			−2.0	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V	OEY = LOW			100	μA
I_I	Input HIGH Current	V_{CC} = MAX, V_{IN} = 5.5V	OEY = LOW			1.0	mA
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX		−30		−130	mA

DC CHARACTERISTICS OVER OPERATING RANGE – B BUS

Parameters	Descriptions	Test Conditions (Note 1)		Min	Typ (Note 2)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OH} = −3.0mA	2.4			Volts
			I_{OH} = −15mA	2.0			
V_{OL}	Output LOW Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 12mA		0.3	0.45	Volts
			I_{OL} = 24mA		0.35	0.50	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs	MIL			0.7	Volts
			COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA				−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.4V	$\overline{OEB}$ = HIGH			−1.0	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V	$\overline{OEB}$ = HIGH			100	μA
I_I	Input HIGH Current	V_{CC} = MAX, V_{IN} = 5.5V	$\overline{OEB}$ = HIGH			1.0	mA
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX		−50		−150	mA

Notes: 1. For conditions as MIN or MAX, use the appropriate value specified under Operating Range for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

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Refer to Page 13-1 for Essential Information on Military Devices

DC CHARACTERISTICS OVER OPERATING RANGE – DO OUTPUTS

Parameters	Descriptions	Test Conditions (Note 1)		Min	Typ (Note 2)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	MIL I_{OH} = –50μA	2.5			Volts
			COM'L I_{OH} = –100μA	2.7			Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 1mA			0.4	Volts
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX		–50		–150	mA
I_O	Off-State Out Current	V_{CC} = MAX	V_O = 0.4V			–100	μA
			V_O = 2.4V			+100	

DC CHARACTERISTICS OVER OPERATING RANGE – DI INPUTS AND CONTROLS

Parameters	Descriptions	Test Conditions (Note 1)		Min	Typ (Note 2)	Max	Units
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs	MIL			0.7	Volts
			COM'L			0.8	
V_C	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = –18mA				–1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.4V	DI Inputs			–1.0	mA
			Controls			–1.6	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V				50	μA
I_I	Input HIGH Current	V_{CC} = MAX, V_{IN} = 5.5V				1.0	mA

DC CHARACTERISTICS OVER OPERATING RANGE – POWER SUPPLY

Parameters	Descriptions	Test Conditions (Note 1)	Min	Typ (Note 2)	Max	Units
I_{CC}	Power Supply Current	V_{CC} = MAX		110	155	mA

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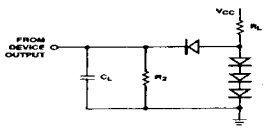
SWITCHING TEST CIRCUIT



TC000400

Figure 1.

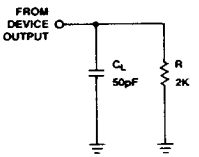


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Figure 2.

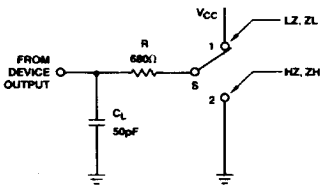

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Figure 3.

SWITCHING CHARACTERISTICS over operating range unless otherwise specified*

Am2961

Parameters	Description	Test Conditions	COMMERCIAL Min	COMMERCIAL Max	MILITARY Min	MILITARY Max	Units
t_{PLH}	Propagation Delay $\overline{B}$ to Y (Latch Transparent, OEY = LEY = HIGH)	Figure 1 C_L = 5pF R_L = 390Ω R_2 = 1kΩ		25		28	ns
t_{PHL}				25		28	ns
t_{PLH}	Propagation Delay $\overline{DI}$ to Y (OEY = HIGH, S = LOW)			15		18	ns
t_{PHL}				15		18	ns
t_{PLH}	Propagation Delay S to Y (OEY = HIGH)			25		28	ns
t_{PHL}				25		28	ns
t_{PLH}	Propagation Delay LEY to Y (OEY = S = HIGH)			25		30	ns
t_{PHL}				35		40	ns
t_{PZH}	Y Bus Output Enable Time OEY to Y			18		21	ns
t_{PZL}				18		21	ns
t_{PHZ}	Y Bus Output Disable Time OEY to Y			18		21	ns
t_{PLZ}				18		21	ns
t_{PLH}	Propagation Delay LEB to $\overline{B}$ ($\overline{OEB}$ = LOW)	Figure 1 C_L = 50pF R_L = 270Ω R_2 = 1kΩ		25		30	ns
t_{PHL}				35		40	ns
t_{PLH}	Propagation Delay Y to $\overline{B}$ (Latch Transparent, LEB = HIGH, $\overline{OEB}$ = LOW, OEY = LOW)			18		21	ns
t_{PHL}				20		23	ns
t_{PLH}	Propagation Delay Y to $\overline{B}$ (Latch Transparent, LEB = HIGH, $\overline{OEB}$ = LOW, OEY = LOW)	Figure 1 C_L = 300pF R_L = 270Ω R_2 = 1kΩ		26		30	ns
t_{PHL}				31		35	ns
t_{PZH}	$\overline{B}$ Bus Output Enable Time $\overline{OEB}$ to $\overline{B}$	Figure 1 C_L = 50pF R_L = 270Ω R_2 = 1kΩ		18		21	ns
t_{PZL}				18		21	ns
t_{PLZ}	$\overline{B}$ Bus Output Disable Time $\overline{OEB}$ to $\overline{B}$			18		21	ns
t_{PHZ}				18		21	ns
t_{PLH}	Propagation Delay Y to $\overline{DO}$ ($\overline{OED}$ = OEY = LOW)	Figure 2 C_L = 50PF R = 2kΩ		15		18	ns
t_{PHL}				20		23	ns
t_{PZH}	$\overline{DO}$ Output Enable Time $\overline{OED}$ to $\overline{DO}$	S = 2 Figure 3 C_L = 50pF R = 680Ω		28		30	ns
t_{PZL}		S = 1		28		30	ns
t_{PHZ}	$\overline{DO}$ Output Disable Time $\overline{OED}$ to $\overline{DO}$	S = 2		16		18	ns
t_{PLZ}		S = 1		24		28	ns
t_S	$\overline{B}$ to LEY Set-up Time ($\overline{OEB}$ = HIGH)	Figure 1 C_L = 50pF R_L = 390Ω R_2 = 1kΩ	6		6		ns
t_H	$\overline{B}$ to LEY Hold Time ($\overline{OEB}$ = HIGH)		9		10		ns
t_S	Y to LEB Set-up Time (OEY = LOW)	Figure 1 C_L = 50pF R_L = 270Ω R_2 = 1kΩ	6		6		ns
t_H	Y to LEB Hold Time (OEY = LOW)		9		10		ns

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

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Refer to Page 13-1 for Essential Information on Military Devices

SWITCHING CHARACTERISTICS over operating range unless otherwise specified*

Am2962

Parameters	Description	Test Conditions	COMMERCIAL Min	COMMERCIAL Max	MILITARY Min	MILITARY Max	Units
t_{PLH}	Propagation Delay B to Y (Latch Transparent, $\overline{OEY}$ = LEY = HIGH)	Figure 1, C_L = 5pF, R_L = 390Ω, R_2 = 1kΩ		27		28	ns
t_{PHL}				27		28	ns
t_{PLH}	Propagation Delay $\overline{Di}$ to Y ($\overline{OEY}$ = HIGH, S = LOW)			15		18	ns
t_{PHL}				15		18	ns
t_{PLH}	Propagation Delay S to Y ($\overline{OEY}$ = HIGH)			25		28	ns
t_{PHL}				25		30	ns
t_{PLH}	Propagation Delay LEY to Y ($\overline{OEY}$ = S = HIGH)			25		30	ns
t_{PHL}				35		40	ns
t_{PZH}	Y Bus Output Enable Time $\overline{OEY}$ to Y			18		21	ns
t_{PZL}				18		21	ns
t_{PHZ}	Y Bus Output Disable Time $\overline{OEY}$ to Y			18		21	ns
t_{PLZ}				18		21	ns
t_{PLH}	Propagation Delay LEB to B ($\overline{OEB}$ = LOW)	Figure 1, C_L = 50pF, R_L = 270Ω, R_2 = 1kΩ		25		30	ns
t_{PHL}				35		40	ns
t_{PLH}	Propagation Delay Y to B (Latch Transparent, LEB = HIGH, $\overline{OEB}$ = LOW, $\overline{OEY}$ = LOW)			20		23	ns
t_{PHL}				21		24	ns
t_{PLH}	Propagation Delay Y to B (Latch Transparent, LEB = HIGH, $\overline{OEB}$ = LOW, $\overline{OEY}$ = LOW)	Figure 1, C_L = 300p F, R_L = 270Ω, R_2 = 1kΩ		28		32	ns
t_{PHL}				32		36	ns
t_{PZH}	B Bus Output Enable Time $\overline{OEB}$ to B	Figure 1, C_L = 50pF, R_L = 270Ω, R_2 = 1kΩ		18		21	ns
t_{PZL}				18		21	ns
t_{PLZ}	B Bus Output Disable Time $\overline{OEB}$ to B			18		21	ns
t_{PHZ}				18		21	ns
t_{PLH}	Propagation Delay Y to $\overline{DO}$ ($\overline{OED}$ = $\overline{OEY}$ = LOW)	Figure 2, C_L = 50pF, R = 2KΩ		15		18	ns
t_{PHL}				20		23	ns
t_{PZH}	$\overline{DO}$ Output Enable Time $\overline{OED}$ to $\overline{DO}$	S = 2		28		30	ns
t_{PZL}		S = 1		28		30	ns
t_{PHZ}	$\overline{DO}$ Output Disable Time $\overline{OED}$ to $\overline{DO}$	S = 2		16		18	ns
t_{PLZ}		S = 1		24		28	ns
		Figure 3, C_L = 50pF, R = 680Ω					
t_S	B to LEY Set-up Time ($\overline{OEB}$ = HIGH)	Figure 1, C_L = 50pF, R_L = 390Ω, R_2 = 1kΩ	8		8		ns
t_H	B to LEY Hold Time ($\overline{OEB}$ = HIGH)		8		9		ns
t_S	Y to LEB Set-up Time ($\overline{OEY}$ = LOW)	Figure 1, C_L = 50pF, R_L = 270Ω, R_2 = 1kΩ	8		8		ns
t_H	Y to LEB Hold Time ($\overline{OEY}$ = LOW)		8		9		ns

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

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Refer to Page 13-1 for Essential Information on Military Devices