



Am2968A

256K Dynamic Memory Controller/Driver

Advanced
Micro
Devices

DISTINCTIVE CHARACTERISTICS

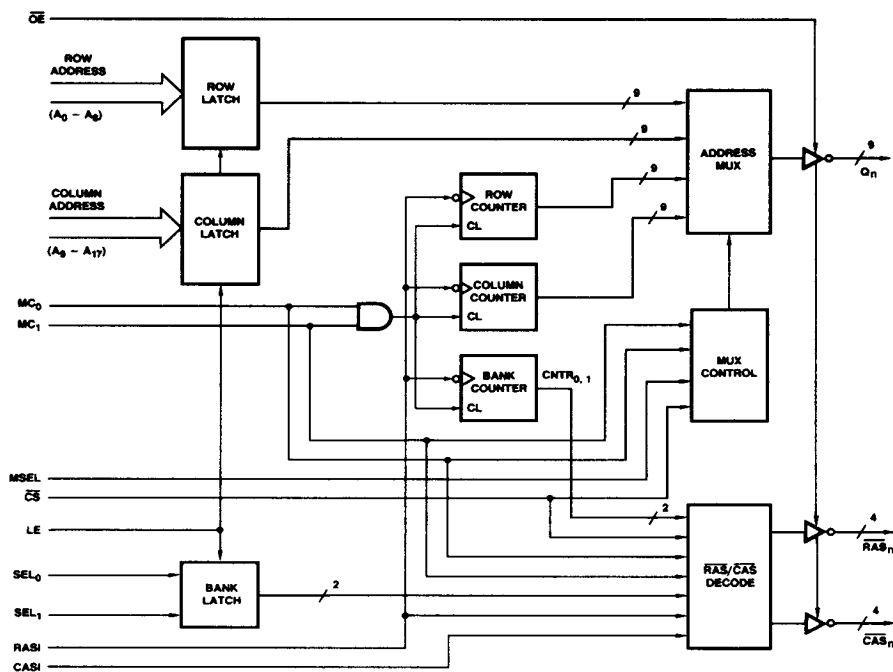
- Provides control for 16K, 64K, and 256K dynamic RAMs
- Outputs directly drive up to 88 DRAMs, with a guaranteed worst-case limit on the undershoot
- Highest-order two address bits select one of four banks of RAMs
- Separate output enable for multi-channel access to memory on surface-mount packages
- Supports scrubbing operations and other specialty access modes
- Upgrade path to Am29368 1M DRAM Controller

GENERAL DESCRIPTION

The Am2968A Dynamic Memory Controller/Driver (DMC) is intended to be used with today's high performance memory systems. The DMC acts as the address controller between any processor and dynamic memory array, using its two 9-bit address latches to hold the Row and Column addresses for any DRAM up to 256K. These latches, and the two Row/Column refresh address counters, feed into a 9-bit, 4-input MUX for output to the dynamic RAM address lines. A 2-bit bank select latch for the two high-order address bits is provided to select one each of the four $\overline{RAS}_n$ and $\overline{CAS}_n$ outputs.

The Am2968A has two basic modes of operation, read/write and refresh. In refresh mode, the two counters cycle through the refresh addresses. If memory scrubbing is not being implemented, only the Row Counter is used, generating up to 512 addresses to refresh a 512-cycle-refresh 256K DRAM. When memory scrubbing is being performed, both the Row and Column counters are used to perform read-modify-write cycles. In this mode all $\overline{RAS}_n$ outputs will be active while only one $\overline{CAS}_n$ is active at a time.

BLOCK DIAGRAM

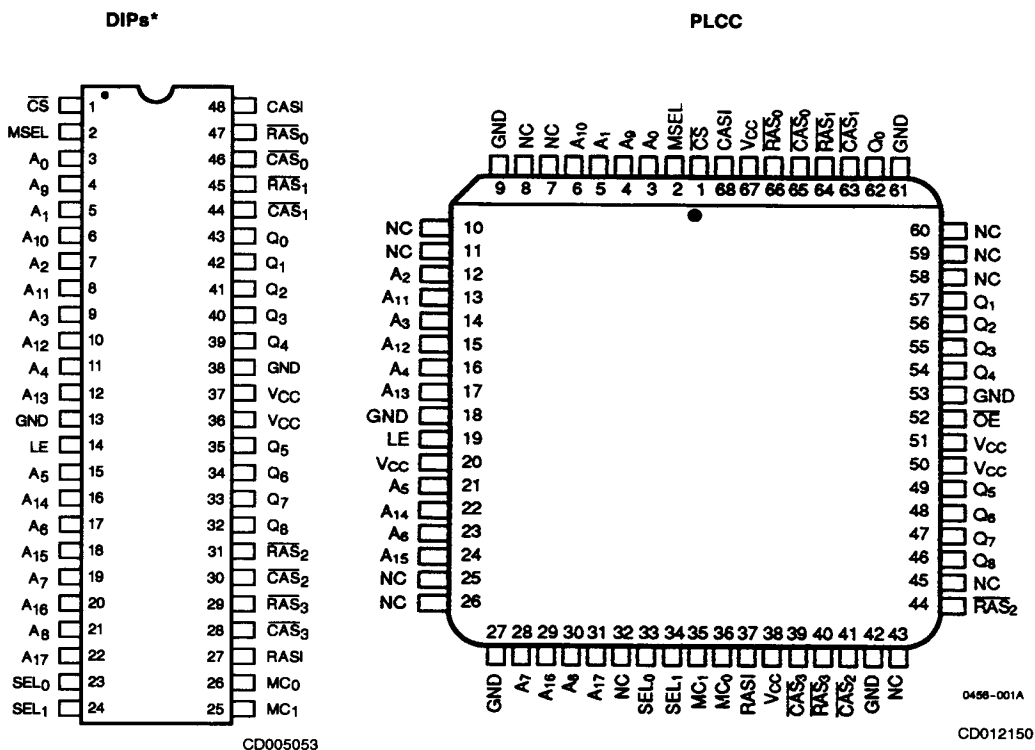


BD001903

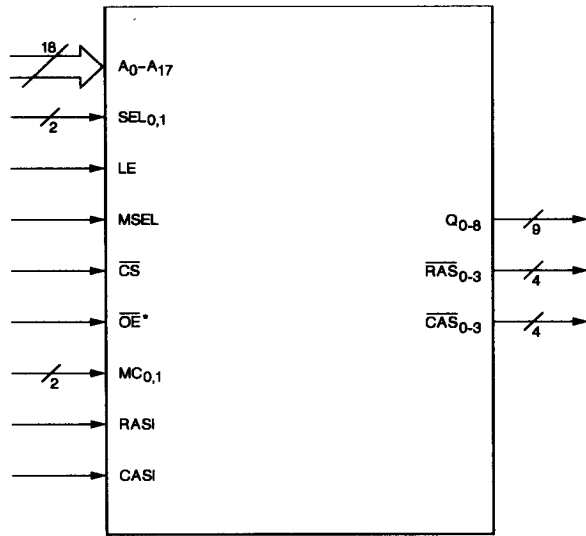
RELATED AMD PRODUCTS

Part No.	Description
Am29C668	4M Configurable Dynamic Memory Controller/Driver
Am29C660D	12ns 32-Bit Cascadable EDC
Am29C983A	9-Bit x 4-Port Multiple Bus Exchange, High Speed
Am29C985	9-Bit x 4-Port Multiple Bus Exchange w/Parity
Am29C60A	16-Bit Cascadable EDC, High Speed
Am29368	1M Dynamic Memory Controller/Driver
Am2971A	100MHz Enhanced Programmable Event Generator
Am2976	11-Bit DRAM Driver
Am2965/6	8-Bit DRAM Driver (Inverting, Non-inverting)
Am29C827A	10-Bit Buffer
Am29C828A	10-Bit Buffer (Inverting)

CONNECTIONS DIAGRAMS Top View



LOGIC DIAGRAM



LS002841

Die Size: 0.205" x 0.256"

Gate Count: 300

Parameter	CERDIP	PDIP	PLCC	Units
θ_{JA}	37	55	31	35
θ_{JC}	10	N/A	6	N/A

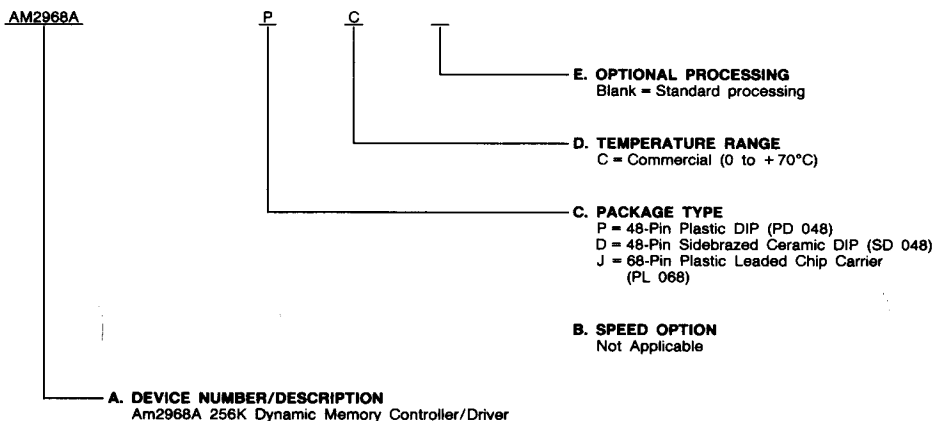
* Available only on surface mount packages.

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

- A. Device Number**
- B. Speed Option** (if applicable)
- C. Package Type**
- D. Temperature Range**
- E. Optional Processing**



Valid Combinations

Valid Combinations	
AM2968A	PC, DC, JC

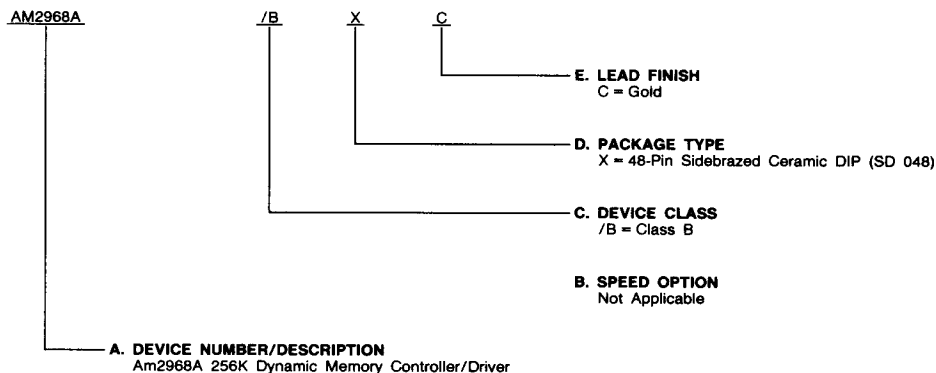
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

ORDERING INFORMATION (Cont'd.)

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. CPL (Controlled Products List) products are processed in accordance with MIL-STD-883C, but are inherently non-compliant because of package, solderability, or surface treatment exceptions to those specifications. The order number (Valid Combination) for APL products is formed by a combination of:

- A. Device Number**
- B. Speed Option** (if applicable)
- C. Device Class**
- D. Package Type**
- E. Lead Finish**



Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

Valid Combinations	
AM2968A	/BXC

Group A Tests

Group A tests consist of 1, 2, 3, 9, 10, 11

PIN DESCRIPTION

A₀ – A₁₇ Address Inputs (Inputs 18)

A₀ – A₈ are latched in as the nine-bit Row Address for the RAM. These inputs drive Q₀ – Q₈ when the Am2968A is in the Read/Write mode and MSEL is LOW. A₉ – A₁₇ are latched in as the Column Address, and will drive Q₀ – Q₈ when MSEL is HIGH and the DMC is in the Read/Write mode. The addresses are latched with the Latch Enable (LE) signal.

CAS₀ – 3 Column Address Strobe (Outputs 4, Active LOW)

During normal Read/Write cycles the two select bits (SEL₀, SEL₁) determine which CAS_n output will go active following CAS_i going HIGH. When memory scrubbing is performed, only the CAS_n signal selected by CNTR₀ and CNTR₁ will be active (see CAS Output Function Table). For non-scrubbing cycles, all four CAS_n outputs remain HIGH.

CASI Column Address Strobe (Input, Active HIGH)

This input going active will cause the selected CAS_n output to be forced LOW.

CS Chip Select (Input, Active LOW)

This active-LOW input is used to select the DMC. When CS is active, the Am2968A operates normally in all four modes. When CS goes HIGH, the device will not enter the Read/Write mode. This allows more than one Am2968A DMC to control the same memory, thus providing an easy method for expanding the memory size.

LE Latch Enable (Input, Active HIGH)

This active-HIGH input causes the Row, Column, and Bank Select latches to become transparent, allowing the latches to accept new input data. A LOW input on LE latches the input data, assuming it meets the setup and hold time requirements.

MC₀ – 1 Mode Control (Inputs 2)

These inputs are used to specify which of the four operating modes the DMC should be using. The description of the four operating modes is given in Table 1.

MSEL Multiplexer Select (Input)

This input determines whether the Row or Column Address will be sent to the memory address inputs. When MSEL is HIGH the Column Address is selected, while the Row Address is selected when MSEL is LOW. The address may come from either the address latch or refresh address counter depending on MC_{0,1}.

OE Output Enable (Input, Active LOW, Three-State)

This active-LOW input enables/disables the output signals. When OE is HIGH, the outputs of the DMC enter the high-impedance state. OE is only available on the surface-mount packages.

Q₀ – 8 Address Outputs (Outputs 9)

These address outputs will feed the DRAM address inputs, and provide drive for memory systems up to 500 picofarads in capacitance.

RAS₀ – 3 Row Address Strobe (Outputs 4, Active LOW)

Each one of the Row Address Strobe outputs provides a RAS_n signal to one of the four banks of dynamic memory. Each will go LOW only when selected by SEL₀ and SEL₁ and only after RASI goes HIGH. All four go LOW in response to RASI in either of the Refresh modes.

RASI Row Address Strobe (Input Active High)

During normal memory cycles, the decoded RAS_n output (RAS₀, RAS₁, RAS₂, or RAS₃) is forced LOW after receipt of RASI. In either Refresh mode, all four RAS_n outputs will go LOW following RASI going HIGH.

SEL₀ – 1 Bank Select (Inputs 2)

These two inputs are normally the two higher-order address bits, and are used in the Read/Write mode to select which bank of memory will be receiving the RAS_n and CAS_n signals after RASI and CAS_i go HIGH.

FUNCTIONAL DESCRIPTION

Architecture

The Am2968A provides all the required data and refresh addresses needed by the dynamic RAM memory. In normal

operation, the Row and Column addresses are multiplexed to the dynamic RAM by using MSEL, with the corresponding RAS_n and CAS_n signals activated to strobe the addresses into the RAM. High capacitance drivers on the outputs allow the DMC to drive four banks of 16-bit words, including a 6-bit checkword, for a total of 88 DRAMs.

Table 1. MODE CONTROL FUNCTION

MC ₁	MC ₀	Operating Mode
0	0	Refresh without Scrubbing. Refresh cycles are performed with only the Row Counter being used to generate addresses. In this mode, all four RAS _n outputs are active while the four CAS _n signals are kept HIGH.
0	1	Refresh with Scrubbing/Initialize. During this mode, refresh cycles are done with both the Row and Column counters generating the addresses. MSEL is used to select between the Row and Column counter. All four RAS _n go active in response to RASI, while only one CAS _n output goes LOW in response to CAS _i . The Bank Counter keeps track of which CAS _n output will go active. This mode is also used on system power-up so that the memory can be written with a known data pattern.
1	0	Read/Write. This mode is used to perform Read/Write cycles. Both the Row and Column addresses are latched and multiplexed to the address output lines using MSEL. SEL ₀ and SEL ₁ are decoded to determine which RAS _n and CAS _n will be active.
1	1	Clear Refresh Counter. This mode will clear the three refresh counters (Row, Column, and Bank) on the HIGH-to-LOW transition of RASI, putting them at the start of the refresh sequence. In this mode, all four RAS _n are driven LOW upon receipt of RASI so that DRAM wake-up cycles may be performed.

Table 2. ADDRESS OUTPUT FUNCTION

CS	MC ₁	MC ₀	MSEL	Mode	MUX Output
0	0	0	X	Refresh without Scrubbing	Row Counter Address
	0	1	1	Refresh with Scrubbing	Column Counter Address
			0		Row Counter Address
	1	0	1	Read/Write	Column Address Latch
			0		Row Address Latch
	1	1	X	Clear Refresh Counter	Zero
1	0	0	X	Refresh without Scrubbing	Row Counter Address
	0	1	1	Refresh with Scrubbing	Column Counter Address
			0		Row Counter Address
	1	0	X	Read/Write	Zero
	1	1	X	Clear Refresh Counter	Zero

Table 3. RAS OUTPUT FUNCTION

RAS _i	CS	MC ₁	MC ₀	SEL ₁	SEL ₀	Mode	RAS ₀	RAS ₁	RAS ₂	RAS ₃
0	X	X	X	X	X	X	1	1	1	1
1	0	0	0	X	X	Refresh without Scrubbing	0	0	0	0
				0	1	Refresh with Scrubbing	0	0	0	0
				0	0	Read/Write	0	1	1	1
				0	1		1	0	1	1
		1	0	1	0		1	1	0	1
				1	1		1	1	1	0
				X	X	Clear Refresh Counter	0	0	0	0
		0	0	X	X	Refresh without Scrubbing	0	0	0	0
	1	0	1			Refresh with Scrubbing	0	0	0	0
		1	0			Read/Write	1	1	1	1
		1	1			Clear Refresh Counter	0	0	0	0

Table 4. CAS OUTPUT FUNCTION

Inputs						Internal		Outputs			
CAS _i	CS	MC ₁	MC ₀	SEL ₁	SEL ₀	CNTR ₁	CNTR ₀	CAS ₀	CAS ₁	CAS ₂	CAS ₃
1	0	0	0	X	X	X	X	1	1	1	1
				X	X	0	0	0	1	1	1
						0	1	1	0	1	1
						1	0	1	1	0	1
						1	1	1	1	1	0
		1	0	0	0	X	X	0	1	1	1
				0	1			1	0	1	1
				1	0			1	1	0	1
				1	1			1	1	1	0
		1	1	X	X	X	X	1	1	1	1
	1	0	0	X	X	X	X	1	1	1	1
				X	X	0	0	0	1	1	1
						0	1	1	0	1	1
						1	0	1	1	0	1
						1	1	1	1	1	0
		1	0	X	X	X	X	1	1	1	1
								1	1	1	1
								1	1	1	1
								1	1	1	1
0	X	X	X	X	X	X	X	1	1	1	1

Input Latches

For those systems where addresses and data are multiplexed onto a single bus, the DMC has latches to hold the address information. The twenty input latches (Row, Column, and Bank Select) are transparent when Latch Enable (LE) is HIGH and will latch the input data meeting setup and hold time requirements when LE goes LOW. For systems where the processor has separate address and data buses, LE may be permanently enabled HIGH.

Refresh Counters

The two 9-bit refresh counters make it possible to support 128, 256, and 512 line refresh. External control over which type of refresh is to be performed allows the user maximum flexibility when choosing the refreshing scheme. Transparent (hidden), burst, synchronous or asynchronous refresh modes are all possible.

The refresh counters are advanced at the HIGH-to-LOW transition of RAS_I. This assures a stable counter output for the next refresh cycle.

Refresh with Error Correction

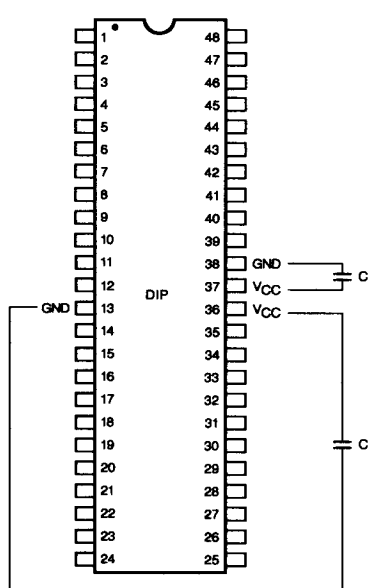
The Am2968A makes it possible to correct single-bit errors in parallel with performing dynamic RAM refresh cycles. This "scrubbing" of memory can be done periodically as a back-

ground routine when the memory is not being used by the processor. In a memory scrubbing cycle (MC_{1,0} = 01), the Row Address is strobed into all four banks with all four RAS_n outputs going LOW.

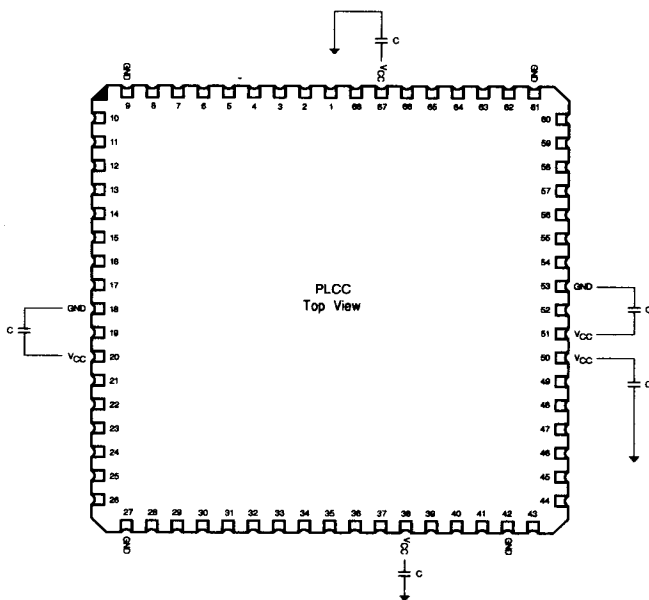
The Column Address is strobed into a single bank with the activated CAS_n output being selected by the Bank Counter. This type of cycle is used to simultaneously refresh the addressed row in all banks and read and correct (if necessary) one word in memory; thereby reducing the overhead associated with Error Detection and Correction. When doing refresh with memory scrubbing, both the Row and Column counters are multiplexed to the dynamic RAM address lines by using MSEL. Using the Refresh with Memory Scrubbing mode implies the presence of an error correcting facility such as the Am29C60A EDC unit. When doing refresh without scrubbing, all four RAS_n still go LOW but the CAS_n outputs are all driven HIGH so as not to activate the output lines of the memory.

Decoupling

Due to the high switching speeds and high drive capability of the Am2968A, it is necessary to decouple the device for proper operation. 1μF multilayer ceramic capacitors are recommended for decoupling (see Figure 1a). It is important to mount the capacitors as close as possible to the power pins (V_{CC}, GND) to minimize lead inductance and noise. A ground plane is recommended.



CD010301



CD010311

Figures 1a
Decoupling Connection Diagrams

V_{ONP}

The guaranteed maximum undershoot voltage of the Am2968A is -0.5 volts. V_{ONP} is measured with respect to

ground (Fig. 1b). Note that the ground of the capacitive load must be the same as for the V_{CC} pin(s). As loading increases, V_{ONP} will approach zero.

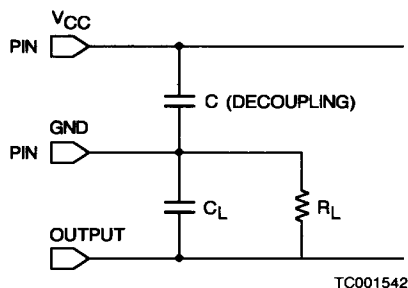
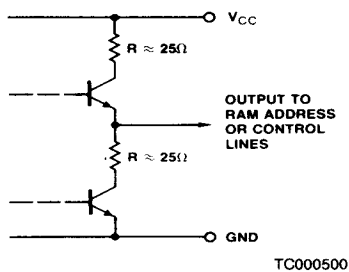


Figure 1b

The RAM Driver symmetrical output design offers significant improvement over a standard Schottky output by providing a balanced drive output impedance ($\approx 25\Omega$ both HIGH and LOW), and by pulling up to MOS V_{OH} levels. External resistors, not required with the RAM Driver, protect standard Schottky drivers from error causing undershoot but also slow the output rise by adding to the internal R.

The RAM Driver is optimized to drive LOW at maximum speed based on safe undershoot control and to drive HIGH with a symmetrical speed characteristic. This is an optimum approach because the dominant RAM loading characteristic is input capacitance.

TYPICAL OUTPUT DRIVER

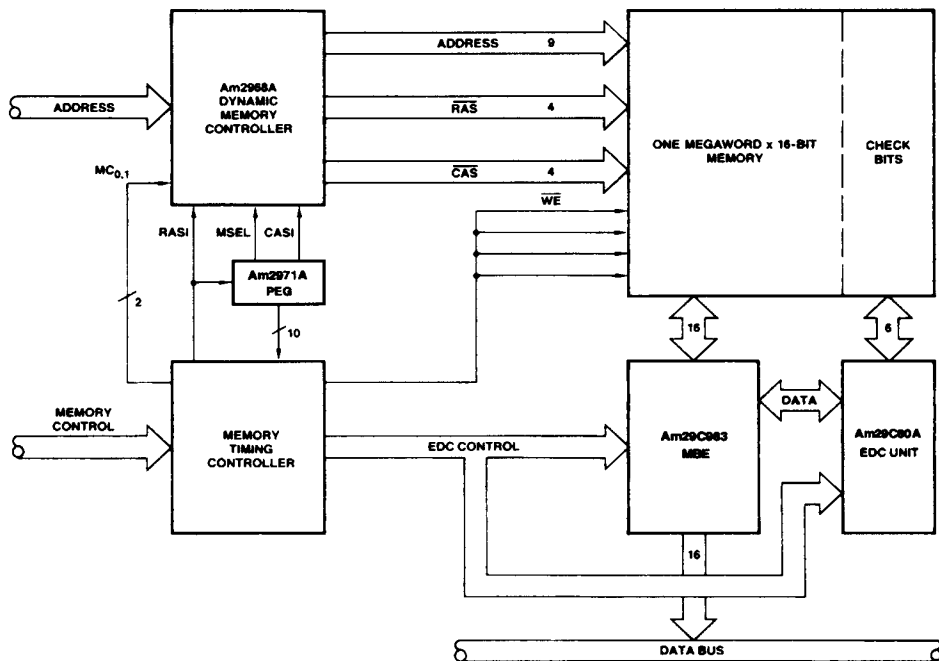


APPLICATIONS

Timing Control

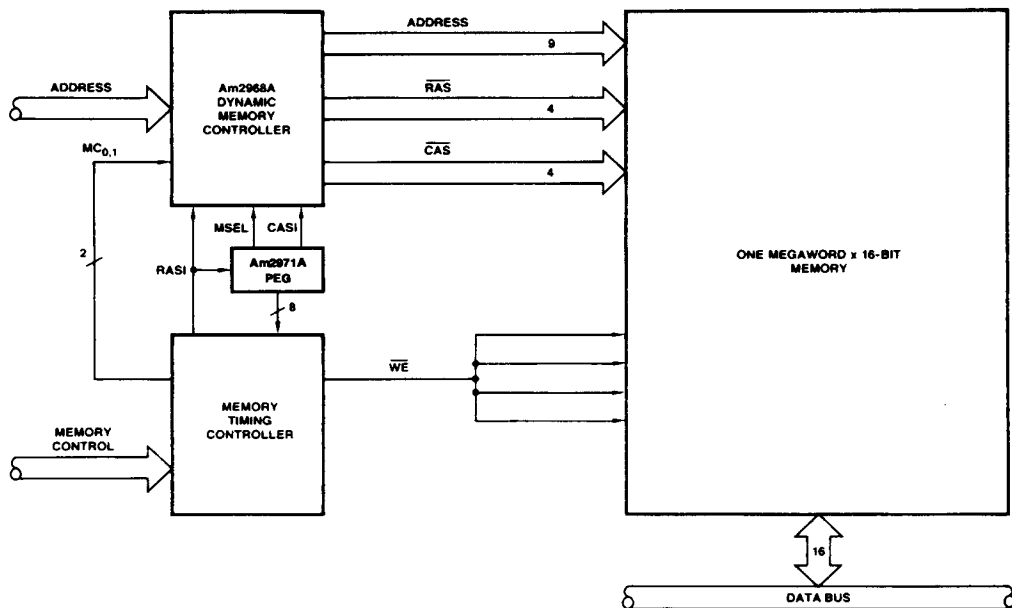
To obtain optimum performance and maximum design flexibility, the timing and control logic for the memory system has

been kept a separate function. For systems implementing Error Detection and Correction, the Am29C60A EDC unit may be used in 16-bit systems. The Am29C983 MBE serves as a data bus buffer.



AF000793

Figure 2a. One Megaword Dynamic Memory with Error Detection and Correction



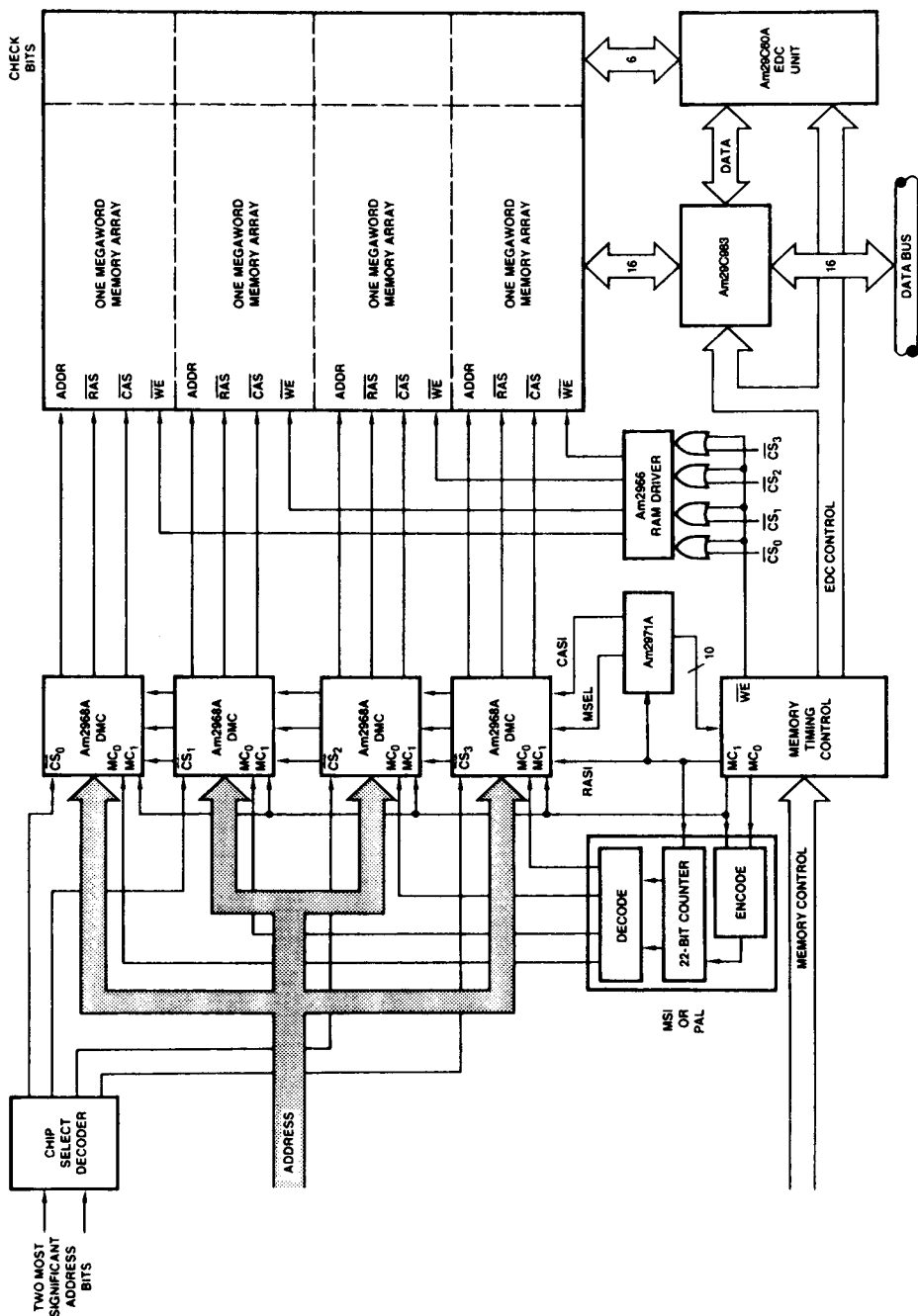
AF000803

Figure 2b. One Megaword Dynamic Memory

Memory Expansion

With a 9-bit address path, the Am2968A can control up to one megaword memory when using 256K dynamic RAMs. If a larger memory size is desired, the DMC's chip select ($\overline{CS}$)

makes it easy to double the memory size by using two Am2968As. Memory can be increased in one megaword increments by adding another DMC unit. A four-megaword memory system implementing EDC is shown in Figure 3.



BD001553

Figure 3. Four Megaword Error Correcting Memory

ABSOLUTE MAXIMUM RATINGS

Storage Temperature -65°C to +150°C
 Ambient Temperature with
 Power Applied -55°C to +125°C
 Supply Voltage to Ground Potential
 Continuous -0.5 V to +7.0 V
 DC Voltage Applied to Outputs For
 High Output State -0.5 V to +V_{CC} max
 DC Input Voltage -0.5 V to +5.5 V
 DC Input Current -30 mA to +5.0 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

T_A (Ambient) 0 to +70°C
 V_{CC} 5.0 V ±10%
 Min 4.50 V
 Max 5.50 V

Military* (M) Devices

T_C (Case) -55 to +125°C
 V_{CC} 5.0 V ±10%
 Min 4.50 V
 Max 5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

*Military Product 100% tested at T_C = 25°C, +125°C, and -55°C.

DC CHARACTERISTICS over operating ranges unless otherwise specified; Included in Group A, Subgroup 1, 2, 3 tests unless otherwise noted.

Parameters	Descriptions	Test Conditions (Note 1)		Min.	Typ.	Max.	Units
V _{OH}	Output HIGH Voltage	V _{CC} = Min., V _{IN} = V _{IH} or V _{IL} I _{OH} = -1 mA	COMM	2.7			Volts
			MIL	2.5			
V _{OL}	Output LOW Voltage	V _{CC} = Min., V _{IN} = V _{IH} or V _{IL}	I _{OL} = 1 mA			0.5	Volts
			I _{OL} = 12 mA			0.8	
V _{IH}	Input HIGH Level	Guaranteed input logical-HIGH voltage for all inputs		2.0			Volts
V _{IL}	Input LOW Level	Guaranteed input logical-LOW voltage for all inputs				0.8	Volts
V _I	Input Clamp Voltage	V _{CC} = Min., I _{IN} = -18 mA				-1.2	Volts
I _{IL}	Input LOW Current	V _{CC} = Max., V _{IN} = 0.4 V				-400	μA
I _{IH}	Input HIGH Current	V _{CC} = Max., V _{IN} = 2.4 V				20	μA
I _I	Input HIGH Current	V _{CC} = Max., V _{IN} = 5.5 V				100	μA
I _{OZH}	Off-State Current	V _O = 2.4 V				50	μA
I _{OZL}	Off-State Current	V _O = 0.4 V				-50	μA
I _{OL}	Output Sink Current	V _{OL} = 2.0 V		45			mA
I _{SC}	Output Short-Circuit Current	V _{CC} = Max. (Note 2)		-60	-95	-275	mA
I _{CC}	Power Supply Current	V _{CC} = Max.	25°C, 5 V		230		mA
			0°C to +70°C			280	
			-55°C to 125°C			295	

Notes: 1. For conditions shown as Min or Max, use the appropriate value specified under Operating Range for the applicable device type.

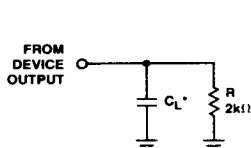
2. Not more than one output should be shorted at a time. Duration of the short-circuit test should not exceed one second.

KEY TO SWITCHING WAVEFORMS

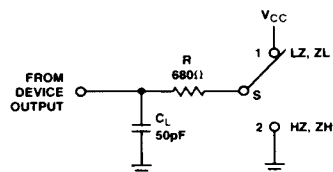
WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

KS000010

SWITCHING TEST CIRCUITS



TC000490



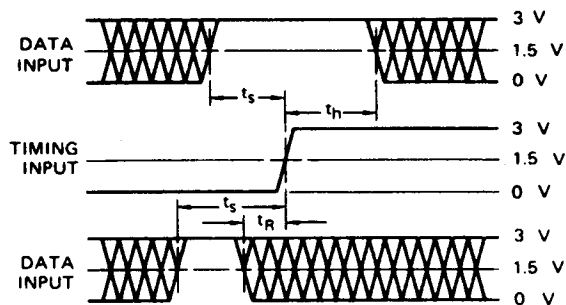
TC000510

* t_{pd} specified at $C_L = 50$ and 500 pF

A. Capacitive Load Switching

B. Three-State Enable/Disable (for PLCC only)

SWITCHING TEST WAVEFORMS

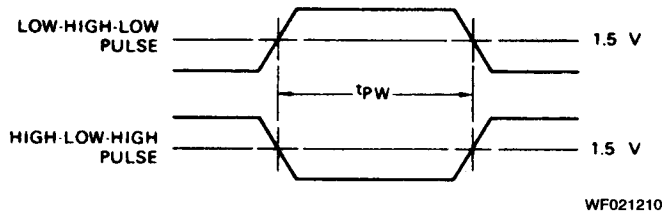


WF021190

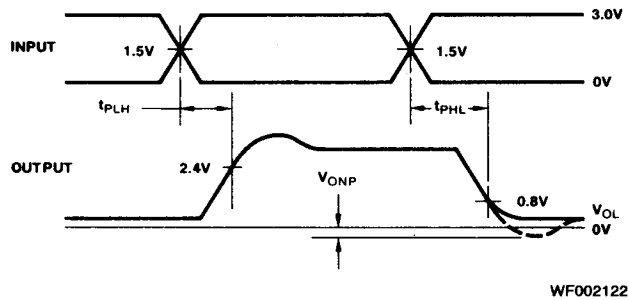
A. Setup, Hold, and Release Times

Notes: 1. Diagram shown for HIGH data only. Output transition may be opposite sense.
2. Cross-hatched are "don't care" condition.

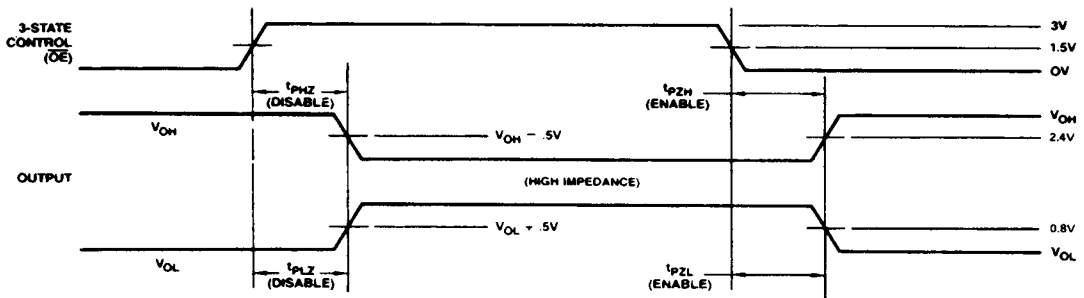
SWITCHING TEST WAVEFORM (Cont'd.)



B. Pulse Width



C. Output Drivers Levels



Note: Decoupling is needed for all AC tests

D. Three-State Control Levels (for Surface-mount packages only)

GENERAL TEST NOTES

Incoming test procedures on this device should be carefully planned, taking into account the complexity and power levels of the part. The following notes may be useful.

1. Insure the part is adequately decoupled at the test head. Large changes in V_{CC} current as the device switches may cause erroneous function failures due to V_{CC} changes.
2. Do not leave inputs floating during any tests, as they may start to oscillate at high frequency.
3. Do not attempt to perform threshold tests at high speed. Following an input transition, ground current may change by as much as 400 mA in 5-8 ns. Inductance in the ground cable may allow the ground pin at the device to rise by hundreds of millivolts momentarily.
4. Use extreme care in defining input levels for AC tests. Many inputs may be changed at once, so there will be significant noise at the device pins and they may not actually reach V_{IL} or V_{IH} until the noise has settled. AMD recommends using $V_{IL} \leq 0$ V and $V_{IH} \geq 4$ V for AC tests.
5. To simplify failure analysis, programs should be designed to perform DC, Function, and AC tests as three distinct groups of tests.
6. Automatic tester hardware and handler add additional round trip A.C. delay to test measurements. Actual propagation delay testing may incorporate a correlation factor to negate the additional delay.

SWITCHING CHARACTERISTICS over operation range for $C_L = 50$ pF; included in Group A, Subgroup 9, 10, 11 tests unless otherwise noted

Parameter Symbol		Parameter Description	Test Conditions	COMMERCIAL AND MILITARY			Units	
				Typ.	Min.	Max.		
1	t _{PD}	A _n to Q _n Delay	Fig. A and C	12	3	20	ns	
2	t _{PD}	RAS _i to $\overline{RAS}_n$		10	3	18	ns	
3	t _{PD}	CAS _i to $\overline{CAS}_n$		8	3	17	ns	
4	t _{PD}	MSEL to Q _n		12	3	20	ns	
5	t _{PD}	MC _n to Q _n		15	5	24	ns	
6	t _{PD}	LE to $\overline{RAS}_n$		15		25	ns	
7	t _{PD}	LE to $\overline{CAS}_n$		14		24	ns	
8	t _{PD}	MC _n to $\overline{RAS}_n$		14	3	21	ns	
9	t _{PD}	MC _n to $\overline{CAS}_n$		12	3	19	ns	
10	t _{PD}	LE to Q _n		15	5	25	ns	
11	t _{PWL}	RAS _i , CAS _i		10	20		ns	
12	t _{PWH}	RAS _i , CAS _i		10	20		ns	
13	t _S	A _n to LE		1	5		ns	
14	t _H	A _n to LE		1	5		ns	
15	t _{PD}	$\overline{CS}$ to Q _n		16		23	ns	
16	t _{PD}	$\overline{CS}$ to $\overline{RAS}_n$		12		20	ns	
17	t _{PD}	$\overline{CS}$ to $\overline{CAS}_n$		11		19	ns	
18	t _{PD}	SEL _n to $\overline{RAS}_n$		12		20	ns	
19	t _{PD}	SEL _n to $\overline{CAS}_n$		11		18	ns	
20	t _S	SEL _n to LE		1	5		ns	
21	t _H	SEL _n to LE		1	5		ns	
22	t _{SKEW}	Q _n to $\overline{RAS}_n$ (MC _n = 10)		10		17	ns	
23	t _{SKEW}	Q _n to $\overline{RAS}_n$ (MC _n = 00, 01)		10		17	ns	
24	t _{SKEW}	Q _n to $\overline{RAS}_n$		2		10	ns	
25	t _{SKEW}	Q _n to $\overline{CAS}_n$		12		17	ns	
26	t _H	MC ₁ to RAS _i	C _L = 50 pF		5		ns	
27	t _S	$\overline{CS}$ to RAS _i	C _L = 50 pF		5		ns	
28	t _S	SEL ₁ to RAS _i	C _L = 50 pF		5		ns	
	t _{PLZ}	Output Disable Time	Fig. D and B	S = 1	15		22	ns
	t _{PHZ}	From LOW, HIGH (Note 1)		S = 2	13		20	ns
	t _{PZL}	Output Enable Time	Fig. D and B	S = 1	13		19	ns
	t _{PZH}	From LOW, HIGH (Note 1)		S = 2	14		21	ns
†	V _{ONP}	Output Undershoot Voltage (Note 2)	Fig. A and C		0		-0.5	V

Notes:

1. Three-state ($\overline{OE}$) applies only to PLCC package.
2. Not tested in production. Guaranteed by characterization data.

† = Not included in Group A testing

SWITCHING CHARACTERISTICS over operating range for $C_L = 150$ pF; included in Group A, Subgroup 9, 10, 11 tests unless otherwise noted (Note 3)

Parameter	Description	Test Conditions	Typ.	COMMERCIAL AND MILITARY		Units
				Min.	Max.	
1	t_{PD}	A_n to Q_n Delay	16	9	24	ns
2	t_{PD}	RAS _i to $\overline{RAS}_n$	15	9	23	ns
3	t_{PD}	CAS _i to $\overline{CAS}_n$	14	9	22	ns
4	t_{PD}	MSEL to Q_n	17	9	26	ns
5	t_{PD}	MC_n to Q_n	18	10	28	ns
6	t_{PD}	LE to $\overline{RAS}_n$	20		28	ns
7	t_{PD}	LE to $\overline{CAS}_n$	19		27	ns
8	t_{PD}	MC_n to $\overline{RAS}_n$	19	9	25	ns
9	t_{PD}	MC_n to $\overline{CAS}_n$	17	9	23	ns
10	t_{PD}	LE to Q_n	20	10	27	ns
11	t_{PWL}	RAS _i , CAS _i	10	20		ns
12	t_{PWH}	RAS _i , CAS _i	10	20		ns
13	t_S	A_n to LE	1	5		ns
14	t_H	A_n to LE	1	5		ns
15	t_{PD}	$\overline{CS}$ to Q_n	19		27	ns
16	t_{PD}	$\overline{CS}$ to $\overline{RAS}_n$	14		22	ns
17	t_{PD}	$\overline{CS}$ to $\overline{CAS}_n$	14		22	ns
18	t_{PD}	SEL _n to $\overline{RAS}_n$	15		23	ns
19	t_{PD}	SEL _n to $\overline{CAS}_n$	14		22	ns
20	t_S	SEL _n to LE	1	5		ns
21	t_H	SEL _n to LE	1	5		ns
22	t_{SKEW}	Q_n to $\overline{RAS}_n$ ($MC_n = 10$)	10		15	ns
23	t_{SKEW}	Q_n to $\overline{RAS}_n$ ($MC_n = 00,01$)	10		17	ns
24	t_{SKEW}	Q_n to $\overline{RAS}_n$	2		8	ns
25	t_{SKEW}	Q_n to $\overline{CAS}_n$	15		17	ns
26	t_H	MC_1 to RAS _i		5		ns
27	t_S	$\overline{CS}$ to RAS _i		5		ns
28	t_S	SEL ₁ to RAS _i		5		ns
†	VONP	Output Undershoot Voltage	0		-0.5	V

Note: 3. Production AC testing at 150pF load is not done. Performance at 150pF load is guaranteed by characterization data and correlation to the 50pF and 500pF measurements.

† = Not included in Group A tests

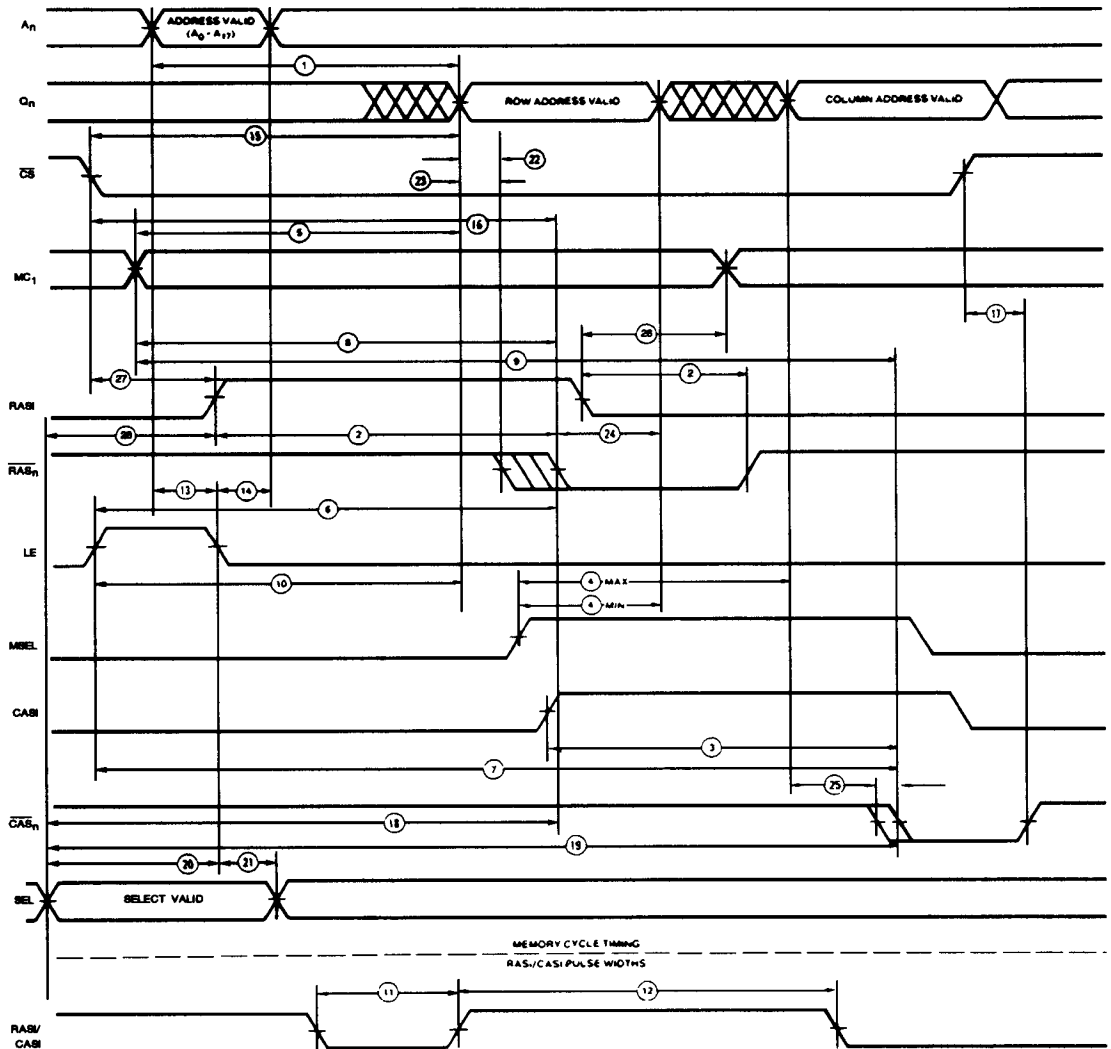
SWITCHING CHARACTERISTICS over operating range for $C_L = 500$ pF. Included in Group A, Subgroup 9, 10, 11 tests unless otherwise noted

Parameter	Description	Test Conditions	Typ.	COMMERCIAL AND MILITARY		Units
				Min.	Max.	
1	t_{PD}	A_n to Q_n Delay	29	12	40	ns
2	t_{PD}	RAS _i to $\overline{RAS}_n$	28	12	40	ns
3	t_{PD}	CAS _i to $\overline{CAS}_n$	26	12	37	ns
4	t_{PD}	MSEL to Q_n	29	12	42	ns
5	t_{PD}	MC_n to Q_n	30	12	44	ns
6	t_{PD}	LE to $\overline{RAS}_n$	32		46	ns
7	t_{PD}	LE to $\overline{CAS}_n$	31		45	ns
8	t_{PD}	MC_n to $\overline{RAS}_n$	30	12	40	ns
9	t_{PD}	MC_n to $\overline{CAS}_n$	28	12	40	ns
10	t_{PD}	LE to Q_n	32	12	46	ns
11	t_{PWL}	RAS _i , CAS _i	10	20		ns
12	t_{PWH}	RAS _i , CAS _i	10	20		ns
13	t_S	A_n to LE	1	5		ns
14	t_H	A_n to LE	1	5		ns
15	t_{PD}	$\overline{CS}$ to Q_n	30		45	ns
16	t_{PD}	$\overline{CS}$ to $\overline{RAS}_n$	27		40	ns
17	t_{PD}	$\overline{CS}$ to $\overline{CAS}_n$	26		38	ns
18	t_{PD}	$\overline{SEL}_n$ to $\overline{RAS}_n$	31		42	ns
19	t_{PD}	$\overline{SEL}_n$ to $\overline{CAS}_n$	28		41	ns
20	t_S	$\overline{SEL}_n$ to LE	1	5		ns
21	t_H	$\overline{SEL}_n$ to LE	1	5		ns
22	t_{SKEW}	Q_n to $\overline{RAS}_n$ ($MC_n = 10$)	10		18	ns
23	t_{SKEW}	Q_n to $\overline{RAS}_n$ ($MC_n = 00,01$)	10		18	ns
24	t_{SKEW}	Q_n to $\overline{RAS}_n$	2		8	ns
25	t_{SKEW}	Q_n to $\overline{CAS}_n$	15		20	ns
26	t_H	MC_1 to RAS _i		5		ns
27	t_S	$\overline{CS}$ to RAS _i		5		ns
28	t_S	$\overline{SEL}_1$ to RAS _i		5		ns
†	V _{ONP}	Output Undershoot Voltage	0		-0.5	V

Fig. A and C

† = Not included in Group A tests

SWITCHING WAVEFORMS



WF003268

Am2968A Dynamic Memory Controller Timing

MEMORY CYCLE TIMING

The relationship between DMC specifications and system timing requirements are shown in Figure 4. T_1 , T_2 and T_3 represent the minimum timing requirements at the DMC inputs to guarantee that RAM timing requirements are met and that maximum system performance is achieved.

The minimum requirement for T_1 , T_2 and T_3 are as follows:

$$T_1 \text{ Min.} = t_{ASR} + t_{22}$$

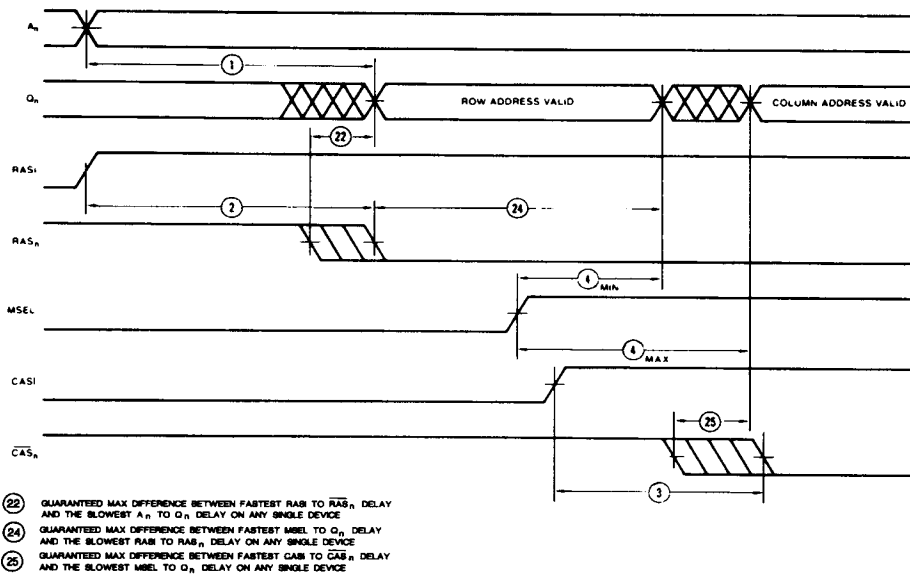
$$T_2 \text{ Min.} = t_{RAH} + t_{24}$$

$$T_3 \text{ Min.} = T_2 + t_{25} + t_{ASC}$$

See RAM data sheet for applicable values for t_{RAH} , t_{ASC} and t_{ASR} .

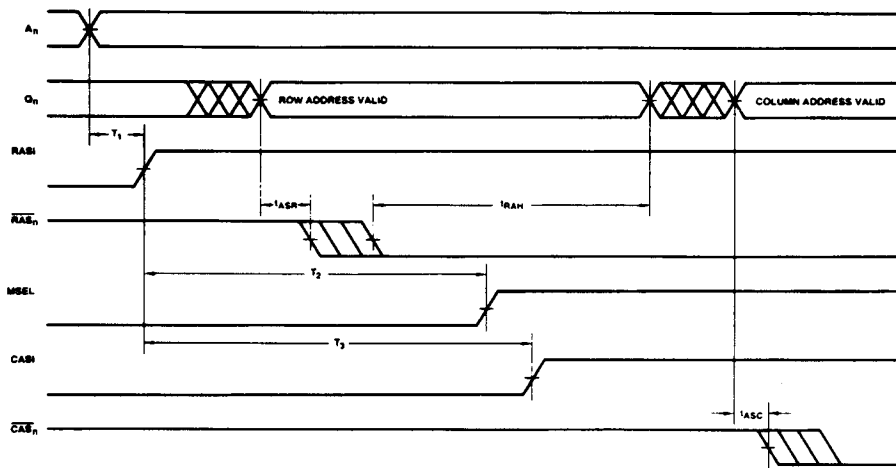
Figure 4. Memory Cycle Timing

a. Specifications Applicable to Memory Cycle Timing ($MC_n = 1, 0$)



WF003285

b. Desired System Timing



WF001962

REFRESH CYCLE TIMING

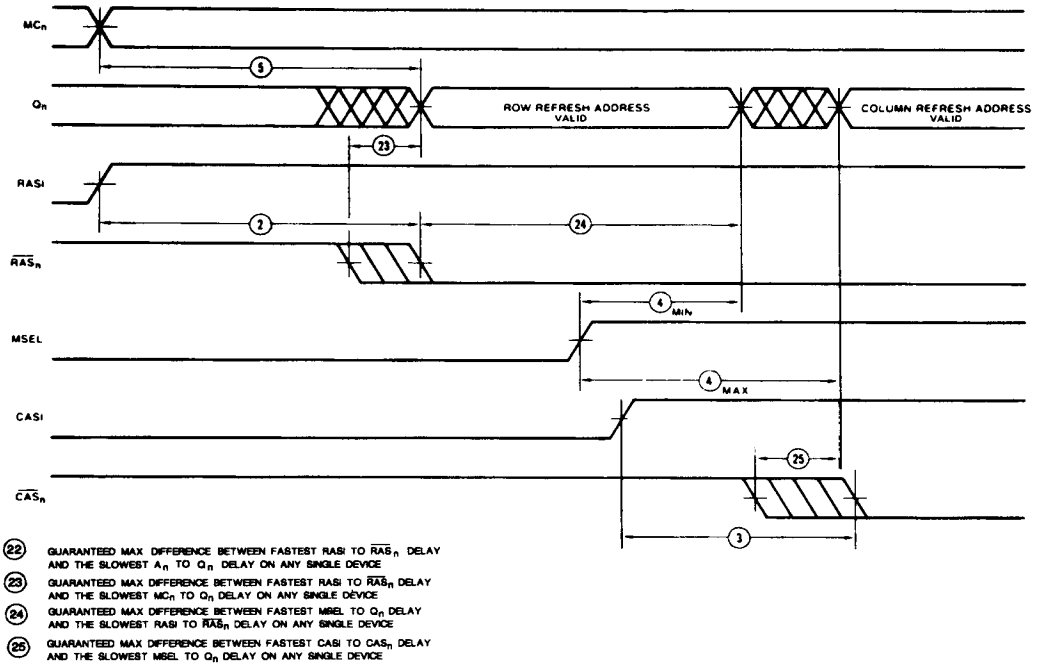
T_4 minimum is calculated as follows:

The timing relationships for refresh are shown in Figure 5.

$$T_4 \text{ Min.} = t_{ASR} + t_{23}$$

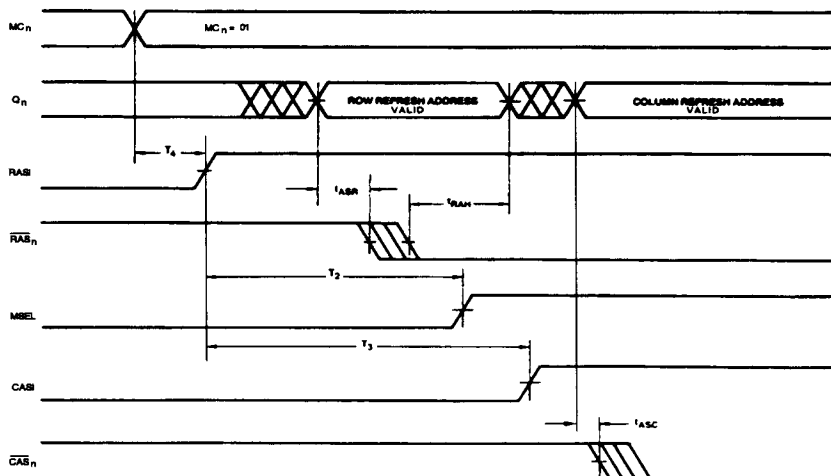
Figure 5. Refresh Cycle Timing

a. Specifications Applicable to Refresh Cycle Timing ($MC_n = 00, 01$)



WF003273

b. Desired Timing: Refresh with Scrubbing

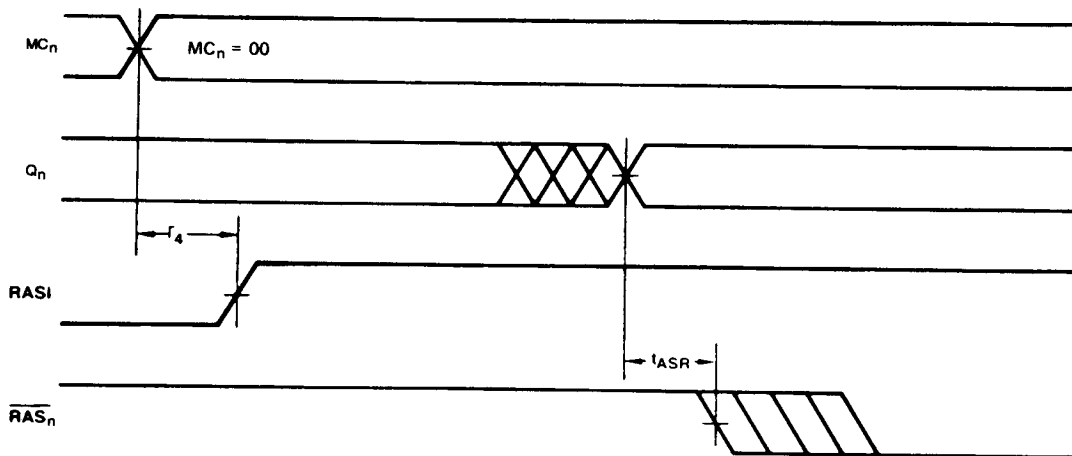


WF001983

REFRESH CYCLE TIMING

Figure 5. Refresh Cycle Timing (Cont'd.)

c. Desired Timing: Refresh without Scrubbing



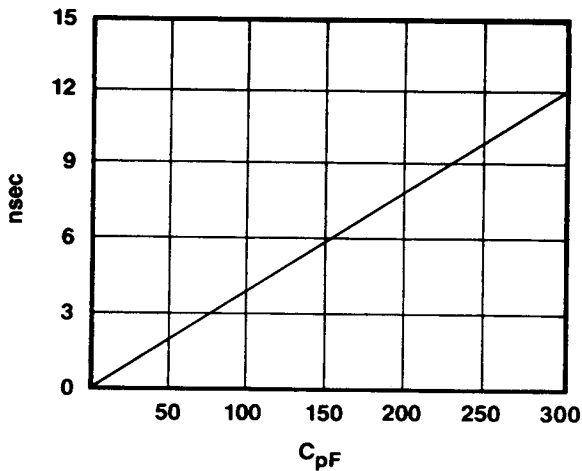
WF003253

NANOSECONDS VERSUS PICOFARADS

To help calculate how the AC performance of the DMC will vary for capacitive loads other than 50, 150, and 500pF refer to the table below.

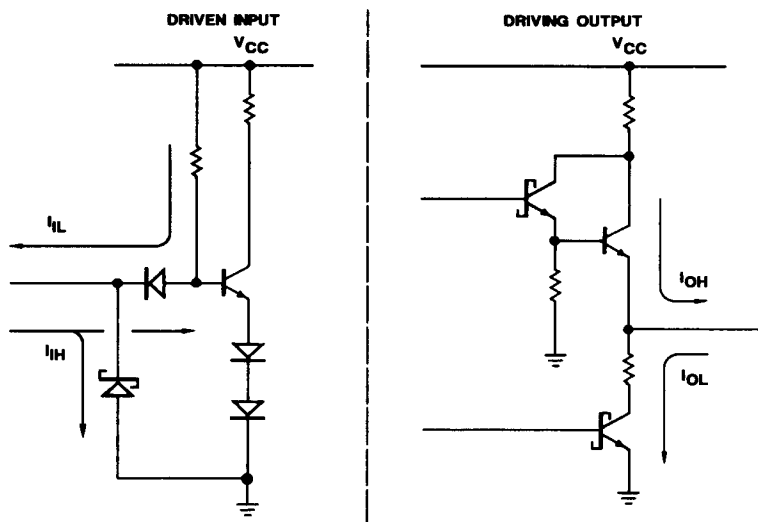
Example: For a system capacitive load of 250pF, add the delay associated with 100pF from the table to the AC specs done at 150pF.

Change in Propagation Delay
versus Loading Capacitance
(TYPICAL)



LCR00011

INPUT/OUTPUT CURRENT DIAGRAM



IC000791