Field-programmable microcontroller peripherals — PSD3XX Family

Key Features

- ❑ Single Chip Programmable Peripheral for Microcontroller-based Applications
- ❑ 19 Individually Configurable I/O pins that can be used as
  - — Microcontroller I/O port expansion
  - — Programmable Address Decoder (PAD) I/O
  - — Latched address output
  - — Open drain or CMOS
- ❑ Two Programmable Arrays (PAD A and PAD B)
  - — Total of 40 Product Terms and up to 16 Inputs and 24 Outputs
  - — Address Decoding up to 1 MB
  - — Logic replacement
- ❑ "No Glue" Microcontroller Chip-Set
  - — Built-in address latches for multiplexed address/data bus
  - — Non-multiplexed address/data bus mode
  - — ALE and Reset polarity programmable
  - — Selectable modes for read and write control bus as $\overline{RD}/\overline{WR}$ or R/$\overline{W}$/E
- ❑ 256 Kbits of UV EPROM
  - — Configurable as 32K x 8 or as 16K x 16
  - — Divides into 8 equal mappable blocks for optimized mapping
  - — Block resolution is 4K x 8 or 2K x 16
  - — 120 ns EPROM access time, including input latches and PAD address decoding.
- ❑ 16 Kbit Static RAM
  - — Configurable as 2K x 8 or as 1K x 16
  - — 120 ns SRAM access time, including input latches and PAD address decoding
- ❑ Address/Data Track Mode
  - — Enables easy Interface to Shared Resources (Mail Box SRAM) with other Microcontrollers or a Host Processor
- ❑ Built-In Security
  - — Locks the PSD3XX Configuration and PAD Decoding
- ❑ Available in a Variety of Packaging
  - — 44 Pin PLDCC and CLDCC
- ❑ Simple Menu-Driven Software: Configure the PSD3XX on an IBM PC

PSD3XX Family Feature Summary

Part	PLD Inputs/ Product Terms	Ports	EPROM Size	SRAM Size	Configuration	Memory Paging	C-Miser Bit	Security Bit
PSD301®	14/40	19	256 Kb	16 Kb	x8 or x16		X	X
PSD311	14/40	19	256 Kb	16 Kb	x8		X	X
PSD302	18/40	19	512 Kb	16 Kb	x8 or x16	X	X	X
PSD312	18/40	19	512 Kb	16 Kb	x8	X	X	X
PSD303	18/40	19	1 Mb	16 Kb	x8 or x16	X	X	X
PSD313	18/40	19	1 Mb	16 Kb	x8	X	X	X

Field-programmable microcontroller peripherals PSD3XX Family

Partial Listing of Microcontrollers Supported

- **Motorola family:**
  M6805, M68HC11, M68HC16, M68000/10/20, M60008, M683XX
- **Intel family:**
  8031/8051, 8096/8098, 80186/88, 80196/98
- **Signetics:**
  SC80C451, SC80552
- **TI:**
  SC80C451, TMS320C14
- **Zilog:**
  Z8, Z80, Z180
- **National:**
  HPC16000, HPC46400

Applications

- Computers (Notebook and Portable PCs)
  - Fixed Disk Control, Modem, Imaging, Laser Printer Control
- Telecommunications
  - Modem, Cellular Phone, Digital PBX, Digital Speech, FAX, Digital Signal Processing
- Portable Industrial Equipment
  - Measurement Meters, Data Recorders
- Medical Instrumentation
  - Hearing Aids, Monitoring Equipment, Diagnostic Tools

Introduction

The PSD3XX Series are members of the rapidly growing family of PSD devices. They are the market's first low-voltage single-chip solution for microcontroller-based applications where consistent specifications for design, fast time-to-market, small form factor, and low power consumptions are essential. When combined in an 8- or 16-bit system, virtually any microcontroller (68HC11, 8051, 80186, etc.) and the PSD3XX device work together to create a very powerful chip-set solution. This implementation eliminates mixing and matching low voltage specifications for various discrete components. It also provides all the required control and peripheral elements needed in a microcontroller-based system with no external discrete "glue" logic required.

The solution comes complete with simple system software development tools for integrating the PSD3XX with the microcontroller. Hosted on IBM PC platforms or compatibles, the easy to use software enables the designer to quickly configure the device and use it immediately.

Product Description

The PSD3XX family integrates high performance user-configurable blocks of EPROM, SRAM, and programmable logic. The major functional blocks include two programmable logic arrays, PAD A and PAD B, 256K to 1Mbit of EPROM, 16K bits of SRAM, input latches, and output ports. The PSD3XX family is ideal for applications requiring low power and very small form factors. These include hard disk control, modems, cellular telephones, instrumentation, computer peripherals, military and similar applications.

The PSD3XX family offers a unique single-chip solution for microcontrollers that need:

- I/O reconstruction (microcontrollers lose at least two I/O ports when accessing external resources).
- More EPROM and SRAM than the microcontroller's internal memory.
- Chip-select, control, or latched address lines that are otherwise implemented discretely.
- An interface to shared external resources.
- Expanded microcontroller address space.

The PSD3XX Family Architecture (Figure 1) can efficiently interface with, and enhance, any low-voltage 8- or 16-bit microcontroller system. This is the first solution that provides microcontrollers with port expansion, latched addresses, page logic, two programmable logic arrays (PAD A and PAD B), an interface to shared resources, 256K, 512K or 1M bit EPROM, and 16K bit SRAM on a single chip. The PSD3XX family does not require any glue logic for interfacing to any 8- or 16-bit microcontroller.

The 8051 microcontroller family can take full advantage of the PSD3XX's separate program and data address spaces. Users of the 68HCXX microcontroller family can change the functionality of the control signals and directly connect the R/$\overline{W}$ and E, or the R/$\overline{W}$ and DS signals. (Users of 16-bit microcontrollers, including the 80186, 8096, 80196 and 16XXX, can use the PSD301/302/303 in a 16-bit configuration). Address and data buses can be configured as separate or multiplexed, whichever is required by the host processor.

The flexibility of the PSD3XX I/O ports permits interfacing to shared resources. The arbitration can be controlled internally by PAD A outputs. The user can assign the following functions to these ports: standard I/O pins, chip-select outputs from PAD A and PAD B, or latched address or multiplexed low-order address/data byte. This enables users to design add-on systems such as disk drives, modems, etc., that easily interface to the host bus (e.g., IBM PC, SCSI).

The page register extends the accessible address space of certain microcontrollers from 64 K to 1 M. There are 16 pages that can serve as base address inputs to the PAD, thereby enlarging the address space of 16 address line microcontrollers by a factor of 16.

Figure 1. PSD3XX Family Architecture

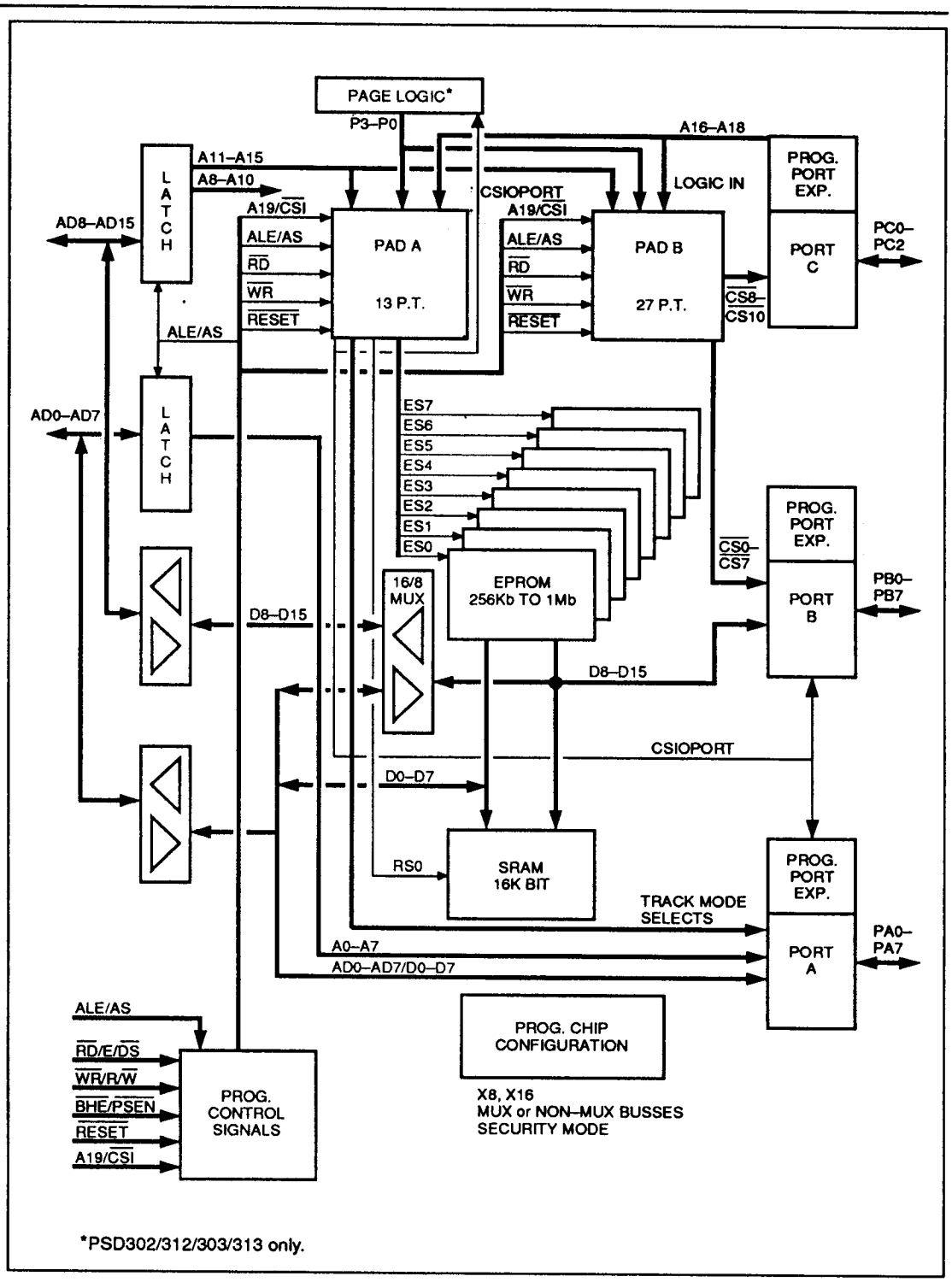


Table 1. PSD3XX Pin Descriptions

Name	Type	Description
$\overline{BHE}/\overline{PSEN}$ (PSD30X Devices)	I	When the data bus width is 8 bits (CDATA = 0), this pin is $\overline{PSEN}$. In this mode, $\overline{PSEN}$ is the active low EPROM read pulse. The SRAM and I/O ports read signal is generated according to the description of the $\overline{WR}/V_{PP}$ or R/$\overline{W}$ and $\overline{RD}/E/\overline{DS}$ pins. If the host processor is a member of the 8031 family, $\overline{PSEN}$ must be connected to the corresponding host pin. In other 8-bit host processors that do not have a special EPROM-only read strobe, PSEN should be tied to V_{CC}. In this case, $\overline{RD}$ or E and R/$\overline{W}$ provide the read strobe for the SRAM, I/O ports, and EPROM. When the data bus width is configured as 16 (CDATA = 1), this pin is $\overline{BHE}$. When $\overline{BHE}$ is low, data bus bits D8–D15 are read from, or written into, the PSD3XX, depending on the operation being read or write, respectively. In programming mode, this pin is pulsed between V_{PP} and 0.
or $\overline{PSEN}$ (PSD31X Devices Only)	I	The $\overline{PSEN}$ is the active low EPROM read pulse. The SRAM and I/O ports read signal is generated according to the description of the $\overline{WR}/V_{PP}$ or R/$\overline{W}$, and $\overline{RD}$/E pins. If the host processor is a member of the 8031 family, $\overline{PSEN}$ must be connected to the correspondinbg host pin. In other 8-bit host processors that do not have a special EPROM-only read strobe, $\overline{PSEN}$ should be tied to V_{CC}. In this case, $\overline{RD}$ or E and R/$\overline{W}$ provide the read strobe for the SRAM, I/O ports, and EPROM.
$\overline{WR}/V_{PP}$ or R/$\overline{W}/V_{PP}$	I	In the operating mode this pin's function is $\overline{WR}$ (CRRWR = 0) or R/$\overline{W}$ (CRRWR = 1) when configured as R/$\overline{W}$. The following tables summarize the read and write operations (CRRWR = 1): CEDS = 0 R/$\overline{W}$ | E | X | 0 | NOP 0 | 1 | write 1 | 1 | read CEDS = 1 R/$\overline{W}$ | $\overline{DS}$ | X | 1 | NOP 0 | 0 | write 1 | 0 | read When configured as $\overline{WR}$, a write operation is executed during an active low pulse. When configured as R/$\overline{W}$, with R/$\overline{W}$ = 1 and E = 1, a read operation is executed; if R/$\overline{W}$ = 0 and E = 1, a write operation is executed. In programming mode, this pin must be tied to V_{PP} voltage.
$\overline{RD}/E/\overline{DS}$ (Note 2)	I	The pin function depends on the CRRWR and CEDS configuration bits. If CRRWR = 0, $\overline{RD}$ is an active low read pulse. When CRRWR = 1, this pin and the R/$\overline{W}$ pin define the following cycle type: If CEDS = 0, E is an active high strobe. If CEDS = 1, $\overline{DS}$ is an active low strobe.
or $\overline{RD}$/E (Note 3)	I	When configured as $\overline{RD}$ (CRRWR = 0), this pin provides an active low $\overline{RD}$ strobe. When configured as E (CRRWR = 1), this pin becomes an active high pulse, which, together with R/$\overline{W}$ defines the cycle type. Then, if R/$\overline{W}$ = 1 and E = 1, a read operation is executed. If R/$\overline{W}$ = 0 and E = 1, a write operation is executed.

Legend: The I/O column abbreviations are: I = input; I/O = input/output; P = power.

NOTE: 1. All the configuration bits mentioned in Table 1 appear in parentheses and are explained in the Configuration Register section.
2. PSD302/312/303/313 only.
3. PSD301/311 only.

Table 1. PSD3XX Pin Descriptions (Cont.)

Name	Type	Description
$\overline{CSI}$/A19	I	This pin has two configurations. When it is $\overline{CSI}$ (CA19/$\overline{CSI}$ = 0) and the pin is asserted high, the device is deselected and powered down. (See Tables 12 and 13 for the chip state during power-down mode.) If the pin is asserted low, the chip is in normal operational mode. When it is configured as A19, (CA19/$\overline{CSI}$ = 1), this pin can be used as an additional input to the PAD. CADLOG3 = 1 defines the pin as an address; CADLOG3 = 0 defines it as a logic input. If it is an address, A19 can be latched with ALE (CADDHLT = 1) or be a transparent logic input (CADDHLT = 0). In this mode, there is no power-down capability.
RESET	I	The user-programmable pin can be configured to reset on high level (CRESET = 1) or on low level (CRESET = 0). It should remain active for at least 100 ns. See Tables 10a, 10b and 11 for the chip state after reset.
ALE or AS	I	In the multiplexed modes, the ALE pin functions as an Address Latch Enable or as an Address strobe and can be configured as an active high or active low signal. The ALE or AS trailing edge latches lines AD15/A15–AD0/A0 and A16–A19 in 16-bit mode (AD7/A7–AD0/A0 and A16–A19 in 8-bit mode) and $\overline{BHE}$, depending on the PSD3XX configuration. See Table 8. In the non-multiplexed modes, it can be used as a general-purpose logic input to the PAD.
PA7 PA6 PA5 PA4 PA3 PA2 PA1 PA0	I/O	PA7–PA0 is an 8-bit port that can be configured to track AD7/A7–AD0/A0 from the input (CPAF2 = 1). Otherwise (CPAF2 = 0), each bit can be configured separately as an I/O or lower-order latched address line. When configured as an I/O (CPAF1 = 0), the direction of the pin is defined by its direction bit, which resides in the direction register. If a pin is an I/O output, its data bit (which resides in the data register) comes out. When it is configured as a low-order address line (CPAF1 =1), A7–A0 can be made the corresponding output through this port (e.g., PA6 can be configured to be the A6 address line). Each port bit can be a CMOS output (CPACOD = 0) or an open drain output (CPACOD = 1). When the chip is in non-multiplexed mode (CADDRAT = 0), the port becomes the data bus lines (D0–D7). See Figure 4.
PB7 PB6 PB5 PB4 PB3 PB2 PB1 PB0	I/O	PB7–PB0 is an 8-bit port for which each bit can be configured as an I/O (CPBF = 1) or chip-select output (CPBF = 0). Each port bit can be a CMOS output (CPBCOD = 0) or an open drain output (CPBCOD = 1). When configured as an I/O, the direction of the pin is defined by its direction bit, which resides in the direction register. If a pin is an I/O output, its data (which resides in the data register) comes out. When configured as a chip-select output, $\overline{CS0}$–$\overline{CS3}$ are a function of up to four product terms of the inputs to the PAD B; $\overline{CS4}$,–$\overline{CS7}$ then are each a function of up to two product terms. On the PSD301L/302L/303L, when the chip is in non-multiplexed mode (CADDRAT = 0) and the data bus width is 16 (CDATA = 1), the port becomes the data bus (D8–D15). See Figure 6.

Table 1. PSD3XX Pin Descriptions (Cont.)

Name	Type	Description
PC0 PC1 PC2	I/O	This is a 3-bit port for which each bit is configurable as a PAD A and B input or output. When configured as an input (CPCF = 0), a bit individually becomes an address (CADLOG = 1) or a logic input (CADLOG = 0). The addresses can be latched with ALE (CADDHLT = 1) or be transparent inputs to the PADs (CADDHLT = 0). When a pin is configured as an output (CPCF = 1), it is a function of one product term of all PAD inputs. See Figure 7.
AD0/A0 AD1/A1 AD2/A2 AD3/A3 AD4/A4 AD5/A5 AD6/A6 AD7/A7	I/O	In multiplexed mode, these pins are the multiplexed low-order address/data byte. After ALE latches the addresses, these pins input or output data, depending on the settings of the $\overline{RD}$/E ($\overline{RD}$/E/$\overline{DS}$ on the PSD302/303), $\overline{WR}$/V_{PP} or R/$\overline{W}$, and $\overline{BHE}$/$\overline{PSEN}$ pins. In non-multiplexed mode, these pins are the low-order address input.
AD8/A8 AD9/A9 AD10/A10 AD11/A11 AD12/A12 AD13/A13 AD14/A14 AD15/A15	I/O	In 16-bit multiplexed mode, these pins are the multiplexed high-order address/data byte. After ALE latches the addresses, these pins input or output data, depending on the settings of the $\overline{RD}$/E or $\overline{RD}$/E/$\overline{DS}$, $\overline{WR}$/V_{PP} or R/$\overline{W}$, and $\overline{BHE}$/$\overline{PSEN}$ pins. In all other modes, these pins are the high-order address input.
GND	P	V_{SS} (ground) pin.
V_{CC}	P	Supply voltage input.

Operating Modes

The PSD3XX's four operating modes enable it to interface directly to 8- and 16-bit microcontrollers with multiplexed and non-multiplexed address/data buses. These operating modes are:

- Multiplexed 8-bit address/data bus
- Multiplexed 16-bit address/data bus (PSD30X)
- Non-multiplexed address/data, 8-bit data bus
- Non-multiplexed 16-bit address/data bus (PSD30X)

Multiplexed 8-bit Address/Data Bus

This mode is used to interface to microcontrollers with an 8-bit data bus and a 16-bit or larger address bus. The address/data bus (AD0/A0–AD7/A7) is bi-directional and permits the latching of the address when the ALE signal is active. On the same pins, the data is read from or written to the device; this depends on the state of the $\overline{RD}$/E or $\overline{RD}$/E/$\overline{DS}$ pin, $\overline{BHE}$/$\overline{PSEN}$ or $\overline{PSEN}$ pin and $\overline{WR}$/V_{PP} or R/$\overline{W}$ pins. The high-order address/data bus (AD8/A8–AD15/A15) contains the high-order address bus byte. Ports A and B can be configured as in Table 2.

Multiplexed 16-bit Address/Data Bus

This mode is used to interface to microcontrollers with a 16-bit data bus and a 16-bit or larger address bus. The low-order address/data bus (AD0/A0–AD7/A7) is bi-directional and permits the latching of the address when the ALE signal is active. On the same pins, the data is read from or written to the device; this depends on the state of the $\overline{RD}$/E/$\overline{DS}$, $\overline{BHE}$/$\overline{PSEN}$, and $\overline{WR}$/V_{PP} or R/$\overline{W}$ pins. The high-order address/data bus (AD8/A8–AD15/A15) is bi-directional and permits latching of the high-order address when the ALE signal is active on the same pins. The high-order data bus is read from or written to the device, depending on the state of the $\overline{RD}$/E/$\overline{DS}$, $\overline{BHE}$/$\overline{PSEN}$, and $\overline{WR}$/V_{PP} or R/$\overline{W}$ pins. Ports A and B can be configured as in Table 2.

Non-Multiplexed Address/Data, 8-bit Data Bus

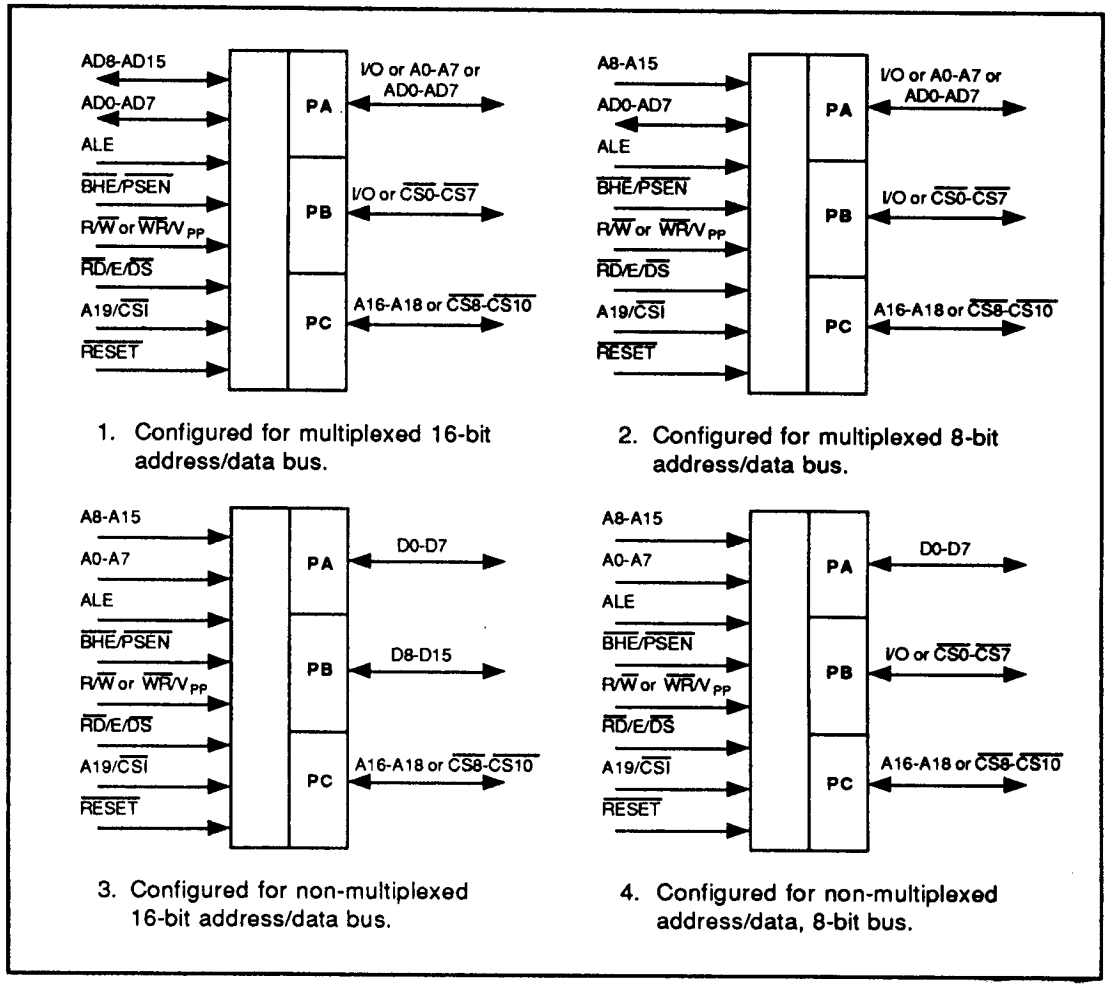
This mode is used to interface to non-multiplexed 8-bit microcontrollers with an 8-bit data bus and a 16-bit or larger address bus. The low-order address/data bus (AD0/A0–AD7/A7) is the low-order address input bus. The high-order address/data bus (AD8/A8–AD15/A15) (A8–A15 on the PSD31X) is the high-order address bus byte. Port A is the low-order data bus. Port B can be configured as shown in Table 2.

Non-Multiplexed Address/Data, 16-bit Data Bus

This mode is used to interface to non-multiplexed 16-bit microcontrollers with a 16-bit data bus and a 16-bit or larger address bus. The low-order address/data bus (AD0/A0–AD7/A7) is the low-order address input bus. The high-order address/data bus (AD8/A8–AD15/A15) is the high-order address bus byte. Port A is the low-order data bus. Port B is the high-order data bus.

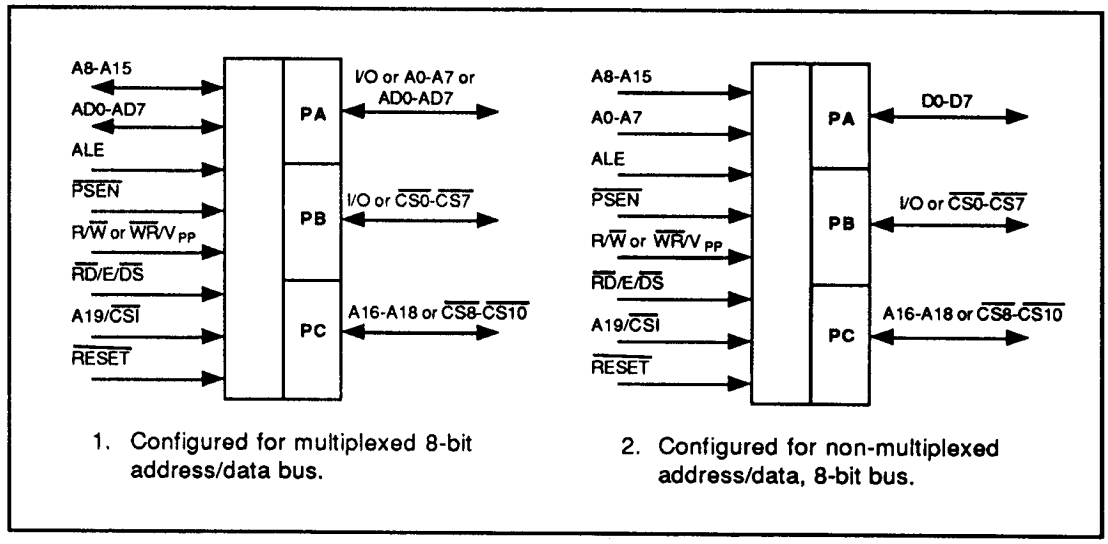
Table 2 summarizes the effect of the different operating modes on ports A, B, and the address/data pins. The configuration of Port C is independent of the four operating modes.

Figure 2a. PSD3XX Port Configurations (x8/x16)



1. Configured for multiplexed 16-bit address/data bus.
2. Configured for multiplexed 8-bit address/data bus.
3. Configured for non-multiplexed 16-bit address/data bus.
4. Configured for non-multiplexed address/data, 8-bit bus.

Figure 2b. PSD3XX Port Configurations (x8 Only)



1. Configured for multiplexed 8-bit address/data bus.
2. Configured for non-multiplexed address/data, 8-bit bus.

Legend: AD8–AD15 = Addresses A8–A15 multiplexed with data lines D8–D15.
AD0–AD7 = Addresses A0–A7 multiplexed with data lines D0–D7.

Table 2. PSD30X Bus and Port Configuration Options

	Multiplexed Address/Data	Non-Multiplexed Address/Data
8-bit Data Bus		
Port A	I/O or low-order address lines or Low-order multiplexed address/data byte	D0–D7 data bus byte
Port B	I/O or $\overline{CS0}$–$\overline{CS7}$	I/O and/or $\overline{CS0}$–$\overline{CS7}$
AD0/A0–AD7/A7	Low-order multiplexed address/data byte	Low-order address bus byte
AD8/A8–AD15/A15	High-order multiplexed address data byte	High-order address bus byte
16-bit Data Bus		
Port A	I/O or low-order address lines or Low-order multiplexed address/data byte	Low-order data bus byte
Port B	I/O or $\overline{CS0}$–$\overline{CS7}$	High-order data bus byte
AD0/A0–AD7/A7	Low-order multiplexed address/data byte	Low-order address bus byte
AD8/A8–AD15/A15	High-order multiplexed address/data byte	High-order address bus byte

Table 2a. PSD31X Bus and Port Configuration Options

	Multiplexed Address/Data	Non-Multiplexed Address/Data
8-bit Data Bus		
Port A	I/O or low-order address lines or Low-order multiplexed address/data byte	D0–D7 data bus byte
Port B	I/O or $\overline{CS0}$–$\overline{CS7}$	I/O and/or $\overline{CS0}$–$\overline{CS7}$
AD0/A0–AD7/A7	Low-order multiplexed address/data byte	Low-order address bus byte
A8–A15	High-order address bus byte	High-order address bus byte

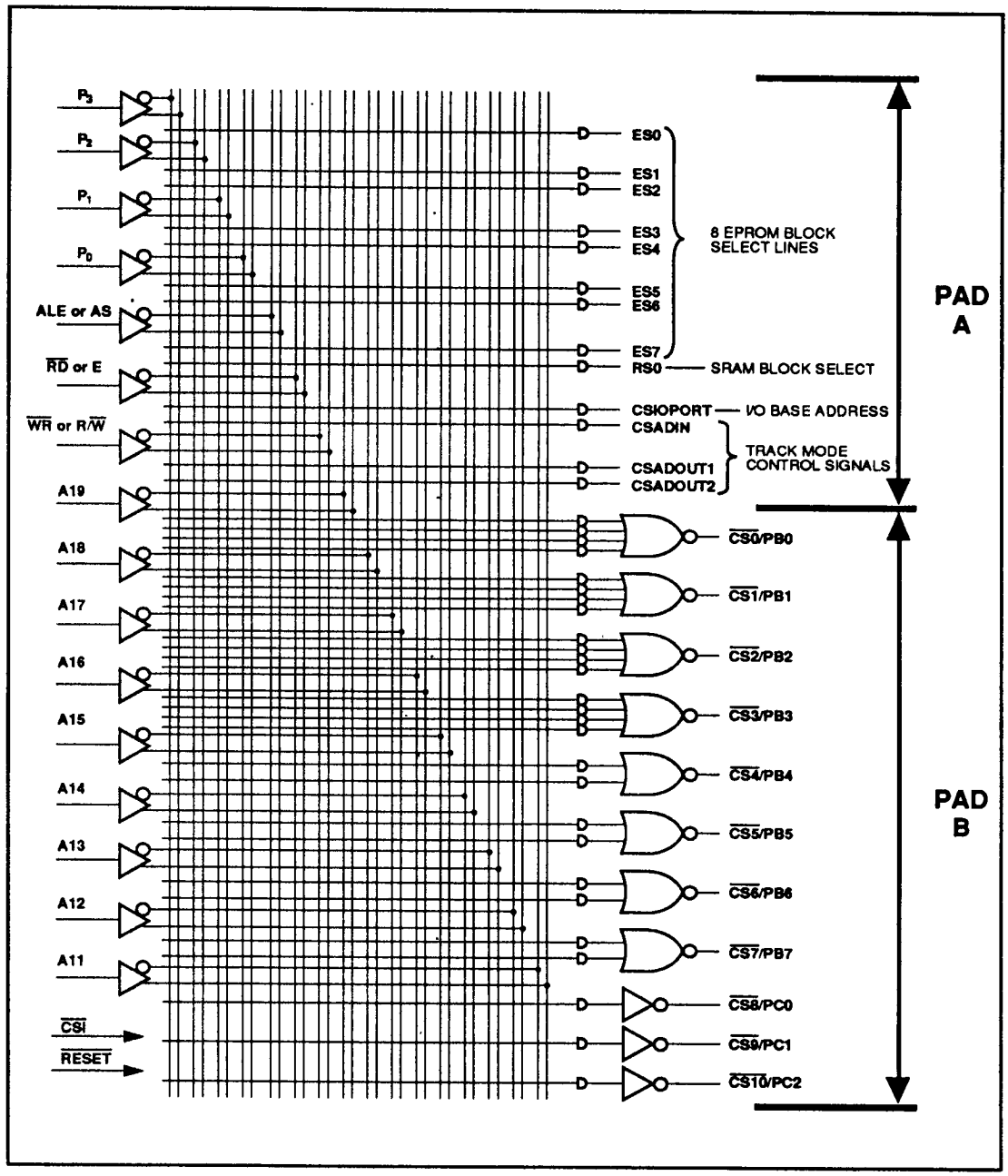
Programmable Address Decoder (PAD)

The PSD3XX consists of two programmable arrays referred to as PAD A and PAD B (Figure 3). PAD A is used to generate chip select signals derived from the input address to the internal EPROM blocks, SRAM, I/O ports, and Track Mode signals. All its I/O functions are listed in Table 3 and shown in Figure 3. PAD B outputs to Ports B and C for off-chip usage.

PAD B can also be used to extend the decoding to select external devices or as a random logic replacement. The input bus to both PAD A and PAD B is the same.

Using MAPLE software, each programmable bit in the PAD's array can have one of three logic states of 0, 1, and don't care (X). In a user's logic design, both PADs can share the same inputs using the X for input signals that are not supposed to affect other functions. The PADs use reprogrammable CMOS EPROM technology and can be programmed and erased by the user.

Figure 3. PAD Description



NOTES:
4. $\overline{CSI}$ is a power-down signal. When high, the PAD is in stand-by mode and all its outputs become non-active. See Tables 12 and 13.
5. RESET deselects all PAD output signals. See Tables 10 and 11.
6. A18, A17, and A16 are internally multiplexed with $\overline{CS10}$, $\overline{CS9}$, and $\overline{CS8}$, respectively. Either A18 or $\overline{CS10}$, A17 or $\overline{CS9}$, and A16 or $\overline{CS8}$ can be routed to the external pins of Port C. Port C can be configured as either input or output.
7. P_0–P_3 are not included on PSD3X1 devices.

Table 3. PSD3XX PAD A and PAD B Functions

	Function
PAD A and PAD B Inputs	
A19/$\overline{CSI}$	In $\overline{CSI}$ mode (when high), PAD deselects all of its outputs and enters a power-down mode (see Tables 12 and 13). In A19 mode, it is another input to the PAD.
A16–A18	These are general purpose inputs from Port C. See Figure 3, Note 4.
A11–A15	These are address inputs.
P0–P3	These are page number inputs (for the PSD302/312/303/313 only).
$\overline{RD}$ or E	. This is the read pulse or enable strobe input.
$\overline{WR}$ or R/$\overline{W}$	This is the write pulse or R/$\overline{W}$ select signal.
ALE	This is the ALE input to the chip.
RESET	This deselects all outputs from the PAD; it can not be used in product term equations. See Tables 10 and 11.
PAD A Outputs	
ES0–ES7	These are internal chip-selects to the 8 EPROM banks. Each bank can be located on any boundary that is a function of one product term of the PAD address inputs.
RS0	This is an internal chip-select to the SRAM. Its base address location is a function of one term of the PAD address inputs.
CSIOPORT	This internal chip-select selects the I/O ports. It can be placed on any boundary that is a function of one product term of the PAD inputs. See Tables 6 and 7.
CSADIN	This internal chip-select, when Port A is configured as a low-order address/data bus in the track mode (CPAF2 = 1), controls the input direction of Port A. CSADIN is gated externally to the PAD by the internal read signal. When CSADIN and a read operation are active, data presented on Port A flows out of AD0/A0–AD7/A7. This chip-select can be placed on any boundary that is a function of one product term of the PAD inputs. See Figure 5.
CSADOUT1	This internal chip-select, when Port A is configured as a low-order address/data bus in track mode (CPAF2 = 1), controls the output direction of Port A. CSADOUT1 is gated externally to the PAD by the ALE signal. When CSADOUT1 and the ALE signal are active, the address presented on AD0/A0–AD7/A7 flows out of Port A. This chip-select can be placed on any boundary that is a function of one product term of the PAD inputs. See Figure 5.
CSADOUT2	This internal chip-select, when Port A is configured as a low-order address/data bus in the track mode (CPAF2 = 1), controls the output direction of Port A. CSADOUT2 must include the write-cycle control signals as part of its product term. When CSADOUT2 is active, the data presented on AD0/A0–AD7/A7 flows out of Port A. This chip-select can be placed on any boundary that is a function of one product term of the PAD inputs. See Figure 5.
PAD B Outputs	
$\overline{CS0}$–$\overline{CS3}$	These chip-select outputs can be routed through Port B. Each of them is a function of up to four product terms of the PAD inputs.
$\overline{CS4}$–$\overline{CS7}$	These chip-select outputs can be routed through Port B. Each of them is a function of up to two product terms of the PAD inputs.
$\overline{CS8}$–$\overline{CS10}$	These chip-select outputs can be routed through Port C. See Figure 3, Note 4. Each of them is a function of one product term of the PAD inputs.

Configuration Bits

The configuration bits shown in Table 4 are non-volatile cells that let the user set the device, I/O, and control functions to the proper operational mode. Table 5 lists all configuration bits. The configuration bits are programmed and verified during the programming phase. In operational mode, they are not accessible. To simplify implementing a specific mode, use the PSD3XX MAPLE software to set the bits.

Table 4. PSD3XX Non-Volatile Configuration Bits

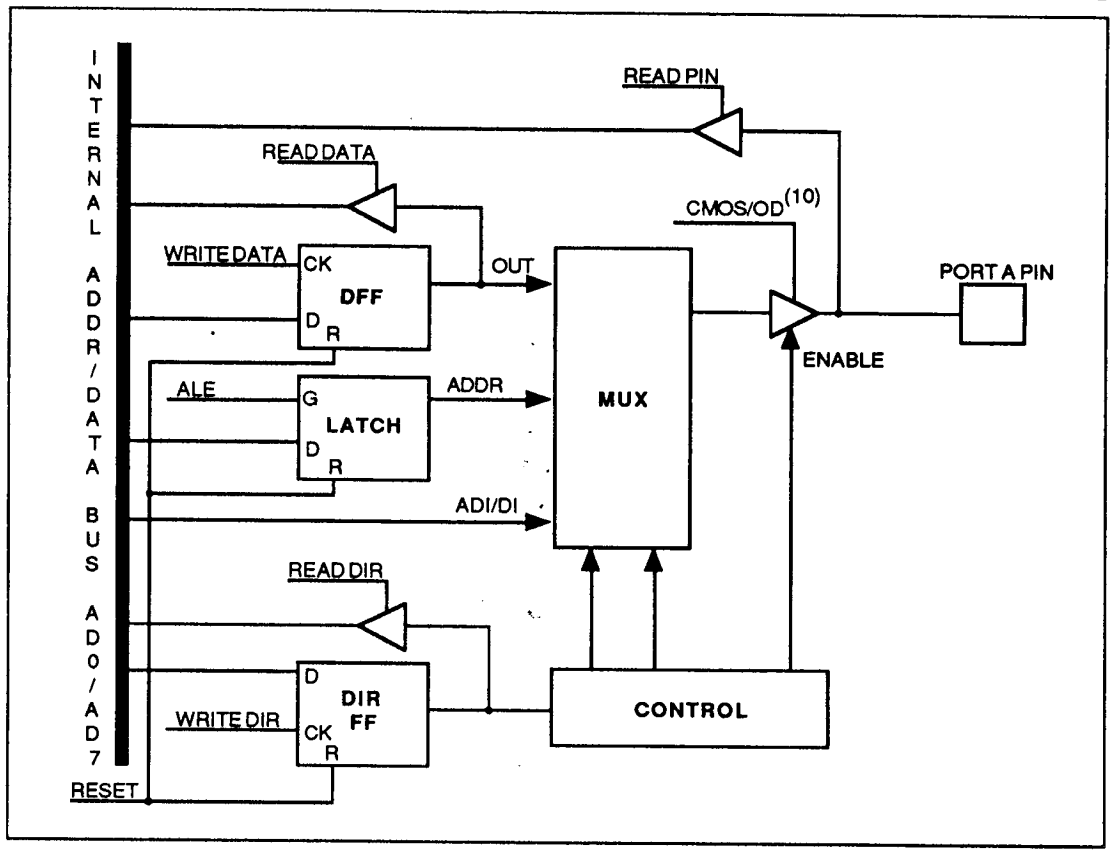
Use This Bit	To
CDATA	Set the data bus width to 8 or 16 bits (PSD30X only).
CADDRDAT	Set the address/data buses to multiplexed or non-multiplexed mode.
CEDS	Determine the polarity and functionality of read and write. (Note 9)
CA19/$\overline{CSI}$	Set A19/$\overline{CSI}$ to $\overline{CSI}$ (power-down) or A19 input.
CALE	Set the ALE polarity.
CPAF2	Set Port A either to track the low-order byte of the address/data multiplexed bus or to select the I/O or address option.
CSECURITY	Set the security on or off (a secured part can not be duplicated).
CRESET	Set the RESET polarity.
$\overline{COMB}$/SEP	Set $\overline{PSEN}$ and $\overline{RD}$ for combined or separate address spaces (see Figures 9 and 10).
CPAF1 (8 Bits)	Configure each pin of Port A in multiplexed mode to be an I/O or address out.
CPACOD (8 Bits)	Configure each pin of Port A as an open drain or active CMOS pull-up output.
CPBF (8 Bits)	Configure each pin of Port B as an I/O or a chip-select output.
CPBCOD (8 Bits)	Configure each pin of Port B as an open drain or active CMOS pull-up output.
CPCF (3 Bits)	Configure each pin of Port C as an address input or a chip-select output.
CADDHLT	Configure pins A16 – A19 to go through a latch or to have their latch transparent.
CADLOG (4 Bits)	Configure A16 – A19 individually as logic or address inputs. (Note 9)
CATD	Configure pins A16–A19 as PAD logic inputs or high-order address inputs (Note 8).
CLOT	Determine in non-multiplexed mode if address inputs are transparent or latched (Note 9).
CRRWR	Set the $\overline{RD}$/E and $\overline{WR}$/V_{PP} or R/$\overline{W}$ pins to $\overline{RD}$ and $\overline{WR}$ pulse, or to E strobe and R/$\overline{W}$ status (Note 8).
CRRWR	Configure the polarity and control methods of read and write cycles. (Note 9)
CMISER	Controls the lower-power mode.

NOTES: 8. PSD31X only. 9. PSD302/312/303/313 only.

Port Functions

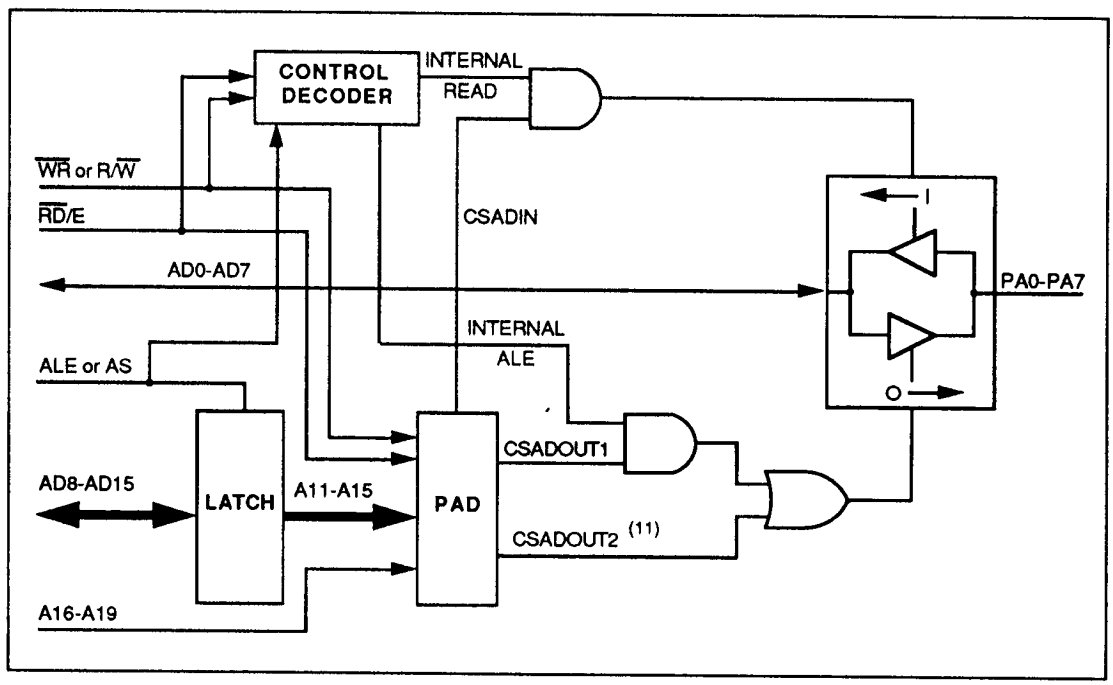
The PSD3XX has three I/O ports (Ports A, B, and C) that are configurable at the bit level. This permits great flexibility and a high degree of customization for specific applications. The following is a description of each port. Figure 4 shows the pin structure of Port A.

Figure 4. Port A Pin Structure



NOTE: 10. CMOS/OD determines whether the output is open drain or CMOS.

Figure 5. Port A Track Mode



NOTE: 11. The expression for CSADOUT2 must include the following write operation cycle signals:
For CRRWR = 0, CSADOUT2 must include $\overline{WR}$ = 0.
For CRRWR = 1, CSADOUT2 must include E = 1 and R/$\overline{W}$ = 0.

Table 5. PSD3XX Configuration Bits[12,13]

Configuration Bits	No. of Bits	Function
CDATA (Note 14)	1	8-bit or 16-bit Data Bus Width CDATA = 0 eight bits CDATA = 1 sixteen bits
CADDRDAT	1	ADDRESS/DATA Multiplexed (separate buses) CADDRDAT = 0, non-multiplexed CADDRDAT = 1, multiplexed
CA19/$\overline{CSI}$	1	A19 or $\overline{CSI}$ CA19/$\overline{CSI}$ = 0, enable power-down CA19/$\overline{CSI}$ = 1, enable A19 input to PAD
CALE	1	Active HIGH or Active LOW CALE = 0, Active high CALE = 1, Active low
CRESET	1	Active high or active low CRESET = 0, active low reset signal CRESET = 1, active high reset signal
$\overline{COMB}$/SEP	1	Combined or Separate Address Space for SRAM and EPROM 0 = Combined, 1 = Separate
CPAF1	8	Port A I/Os or A0–A7 CPAF1 = 0, Port A pin = I/O CPAF1 = 1, Port A pin = A0 – A7
CPAF2	1	Port A AD0–AD7 (address/data multiplexed bus) CPAF2 = 0, address or I/O on Port A (according to CPAF1) CPAF2 = 1, address/data multiplexed on Port A (track mode)
CATD (Note 16)	1	A16–A19 address or logic inputs CATD = 0, logic inputs CATD = 1, address inputs
CADDHLT	1	A16–A19 Transparent or Latched CADDHLT = 0, Address latch transparent CADDHLT = 1, Address latched (ALE dependent)
CSECURITY	1	SECURITY On/Off CSECURITY = 0, off CSECURITY = 1, on
CLOT (Note 15)	1	A0–A15 Address Inputs are transparent or ALE-dependent in non-multiplexed modes CLOT = 0, transparent CLOT = 1, ALE-dependent
CRRWR CEDS (Note 15)	2	Determine the polarity and control methods of read and write cycles. CEDS CRRWR 0 0 $\overline{RD}$ and $\overline{WR}$ active low pulses 0 1 R/$\overline{W}$ status and high E pulse 1 1 R/$\overline{W}$ status and low $\overline{DS}$ pulse
CRRWR (Note 16)	1	CRRWR = 0, $\overline{RD}$ and $\overline{WR}$ active low strobes CRRWR = 1, R/$\overline{W}$ status and E active high pulse
CPACOD	8	Port A CMOS or Open Drain Output CPACOD = 0, CMOS output CPACOD = 1, open-drain output

Table 5. PSD3XX Configuration Bits (Cont.)

Configuration Bits	No. of Bits	Function
CPBF	8	Port B is I/O or $\overline{CS0}$– $\overline{CS7}$ CPBF = 0, Port B pin is CS0 – $\overline{CS7}$ CPBF = 1, Port B pin is I/O
CPBCOD	8	Port B CMOS or Open Drain CPBCOD = 0, CMOS output CPBCOD = 1, open-drain output
CPCF	3	Port C A16–A18 or $\overline{CS8}$–$\overline{CS10}$ CPCF = 0, Port C pin is A16–A18 CPCF = 1, Port C pin is $\overline{CS8}$–$\overline{CS10}$
CADLOG (Note 15)	4	Port C: A16–A19 Address or Logic Input CADLOG = 0, Port C pin or A19/$\overline{CS1}$ is logic input CADLOG = 1, Port C pin or A19/$\overline{CS1}$ is address input
CMISER	1	Default: CMISER = 0 CMISER = 1, lower-power mode

NOTES: 12. The Maple software will guide the user to the proper configuration choice.
13. In an unprogrammed or erased part, all configuration bits are 0.
14. PSD30X only.
15. PSD3X2/3X3 only.
16. PSD3X1 only.

Port Functions (Cont.)

Port A in Multiplexed Address/Data Mode

The default configuration of Port A is I/O. In this mode, every pin can be set as an input or output by writing into the respective pin's direction flip flop (DIR FF, in Figure 4). As an output, the pin level can be controlled by writing into the respective pin's data flip flop (DFF, in Figure 4). When DIR FF = 1, the pin is configured as an output. When DIR FF = 0, the pin is configured as an input. The controller can read the DIR FF bits by accessing the READ DIR register; it can read the DFF bits by accessing the READ DATA register. Port A pin levels can be read by accessing the READ PIN register. Individual pins can be configured as CMOS or open drain outputs. Open drain pins require external pull-up resistors. For addressing information, refer to Tables 6 and 7.

Alternatively, each bit of Port A can be configured as a low-order latched address bus bit. The address is provided by the port address latch, which latches the address on the trailing edge of ALE. PA0–PA7 can become A0–A7, respectively. This feature enables the user generate low-order address bits to access external peripherals or memory that require several low-order address lines.

Another mode of Port A (CPAF2 = 1) sets the entire port to track the inputs AD0/A0–AD7/A7, depending on specific address ranges defined by the PAD's CSADIN, CSADOUT1, and CSADOUT2 signals. This feature lets the user interface the microcontroller to shared external resources without requiring external buffers and decoders. In this mode, the port is effectively a bi-directional buffer. The direction is controlled by using the input signals ALE, $\overline{RD}$/E or $\overline{RD}$/E/$\overline{DS}$, $\overline{WR}$/V_{PP} or R/$\overline{W}$, and the internal PAD outputs $\overline{CS}$ADOUT1, $\overline{CS}$ADOUT2 and CSADIN (see Figure 5). When CSADOUT1 and ALE are true, the address on the input AD0/A0–AD7/A7 pins is output through Port A. (Carefully check the generation of CSADOUT1, and ensure that it is stable during the ALE pulse. When CSADOUT2 is active, a write operation is performed (see note to Figure 5). The data on the input AD0/A0–AD7/A7 pins flows out through Port A. When CSADIN and a read operation is performed (depending on the mode of the $\overline{RD}$/E or $\overline{RD}$/E/$\overline{DS}$, and $\overline{WR}$/V_{PP} or R/$\overline{W}$ pins), the data on Port A flows out through the AD0/A0–AD7/A7 pins. In this operational mode, Port A is tri-stated when none of the above-mentioned three conditions exist.

Port Functions (Cont.)

Port A in Non-Multiplexed Address/Data Mode

In this mode, Port A becomes the low order data bus byte of the chip. When reading an internal location, data is presented on Port A pins. When writing to an internal location, data present on Port A pins is written to that location.

Port B in Multiplexed Address/Data and in 8-Bit Non-Multiplexed Modes

The default configuration of Port B is I/O. In this mode, every pin can be set as an input or output by writing into the respective pin's direction flip flop (DIR FF, in Figure 6). As an output, the pin level can be controlled by writing into the respective pin's data flip flop (DFF, in Figure 6). When DIR FF = 1, the pin is configured as an output. When DIR FF = 0, the pin is configured as an input. The controller can read the DIR FF bits by accessing the READ DIR register; it can read the DFF bits by accessing the READ DATA register. Port B pin levels can be read by accessing the READ PIN register. Individual pins can be configured as CMOS or open drain outputs. Open drain pins require external pull-up resistors. For addressing information, refer to Tables 6 and 7.

Alternately, each bit of Port B can be configured to provide a chip-select output signal from PAD B. PB0–PB7 can provide $\overline{CS0}$–$\overline{CS7}$, respectively. Each of the signals $\overline{CS0}$–$\overline{CS3}$ is comprised of four product terms.Thus, up to four ANDed expressions can be ORed while deriving any of these signals. Each of the signals $\overline{CS4}$–$\overline{CS7}$ is comprised of two product terms. Thus, up to two ANDed expressions can be ORed while deriving any of these signals.

Port B in 16-Bit Non-Multiplexed Address/Data Mode (PSD30X)

In this mode, Port B becomes the high-order data bus byte of the chip. When reading an internal high-order data bus byte location, the data is presented on Port B pins. When writing to an internal high-order data bus byte location, data present on Port B is written to that location. See Table 9.

Accessing the I/O Port Registers

Tables 6 and 7 show the offset values with the respect to the base address defined by the CSIOPORT. They let the user access the corresponding registers.

Port C in All Modes

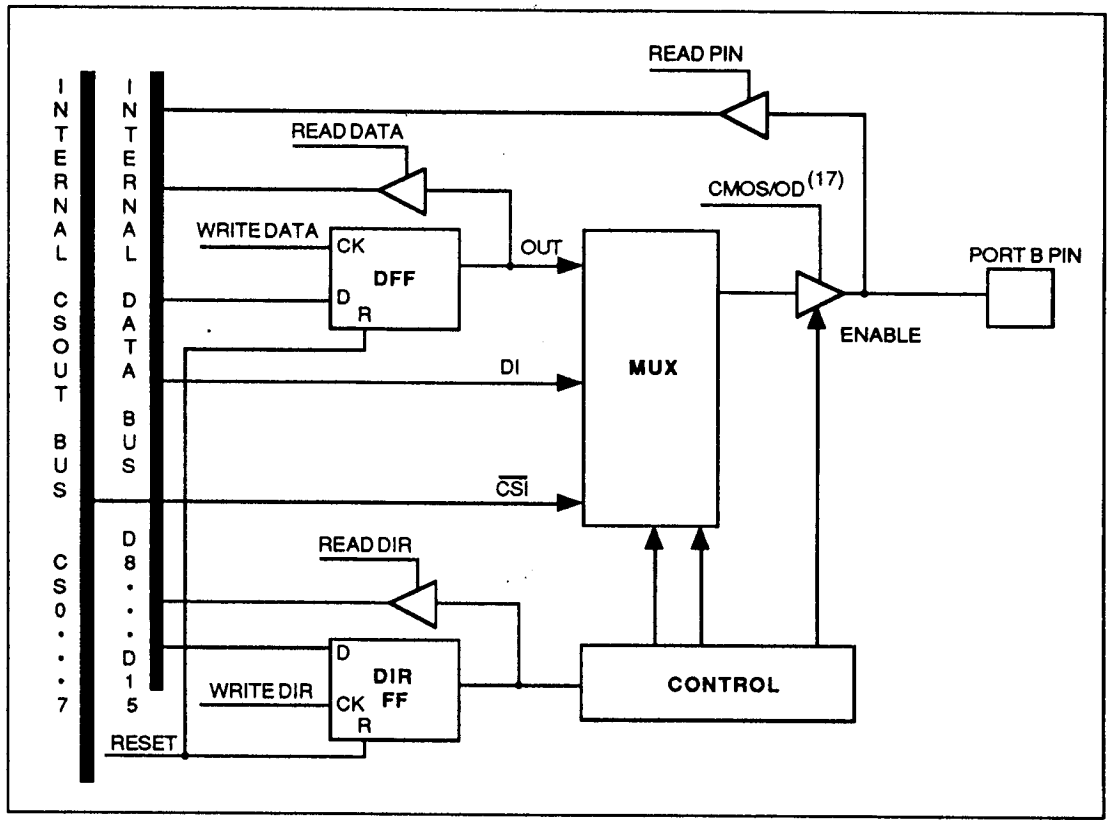
Each pin of Port C (shown in Figure 7) can be configured as an input to PAD A and PAD B or output from PAD B. As inputs, the pins are named A16–A18. Although the pins are given names of the high-order address bus, they can be used for any other address lines or logic inputs to PAD A and PAD B. For example, A8–A10 can also be connected to those pins, improving the boundaries of $\overline{CS0}$–$\overline{CS7}$ resolution to 256 bytes. As inputs, they can be individually configured to be logic or address inputs. A logic input uses the PAD only for Boolean equations that are implemented in any or all of the $\overline{CS0}$–$\overline{CS10}$ PAD B outputs. Port C addresses can be programmed to latch the inputs by the trailing edge ALE or to be transparent.

Alternately, PC0–PC2 can become $\overline{CS8}$–$\overline{CS10}$ outputs, respectively, providing the user with more external chip-select PAD outputs. Each of the signals $\overline{CS8}$–$\overline{CS10}$ is comprised of one product term.

ALE/AS and AD0/A0–AD15/A15 in Non-Multiplexed Modes

In non-multiplexed modes, AD0/A0–AD15/A15 are address inputs only and can become transparent (CLOT = 0) or ALE dependent (CLOT = 1). In transparent mode, the ALE/AS pin can be used as an additional logic input to the PADs. The non-multiplexed ALE dependent mode is useful in applications for which the host processor has a multiplex address/data bus and AD0/A0–AD7/A7 are not multiplexed with A0–A7 but rather are multiplexed with other address lines. In these applications, Port A serves as a data bus and each of its pins can be directly connected to the corresponding host's multiplexed pin, where that data bit is expected.
(See Table 8.)

Figure 6. Port B Pin Structure



NOTE: 17. CMOS/OD determines whether the output is open drain or CMOS.

Table 6. I/O Port Addresses in an 8-bit Data Bus Mode

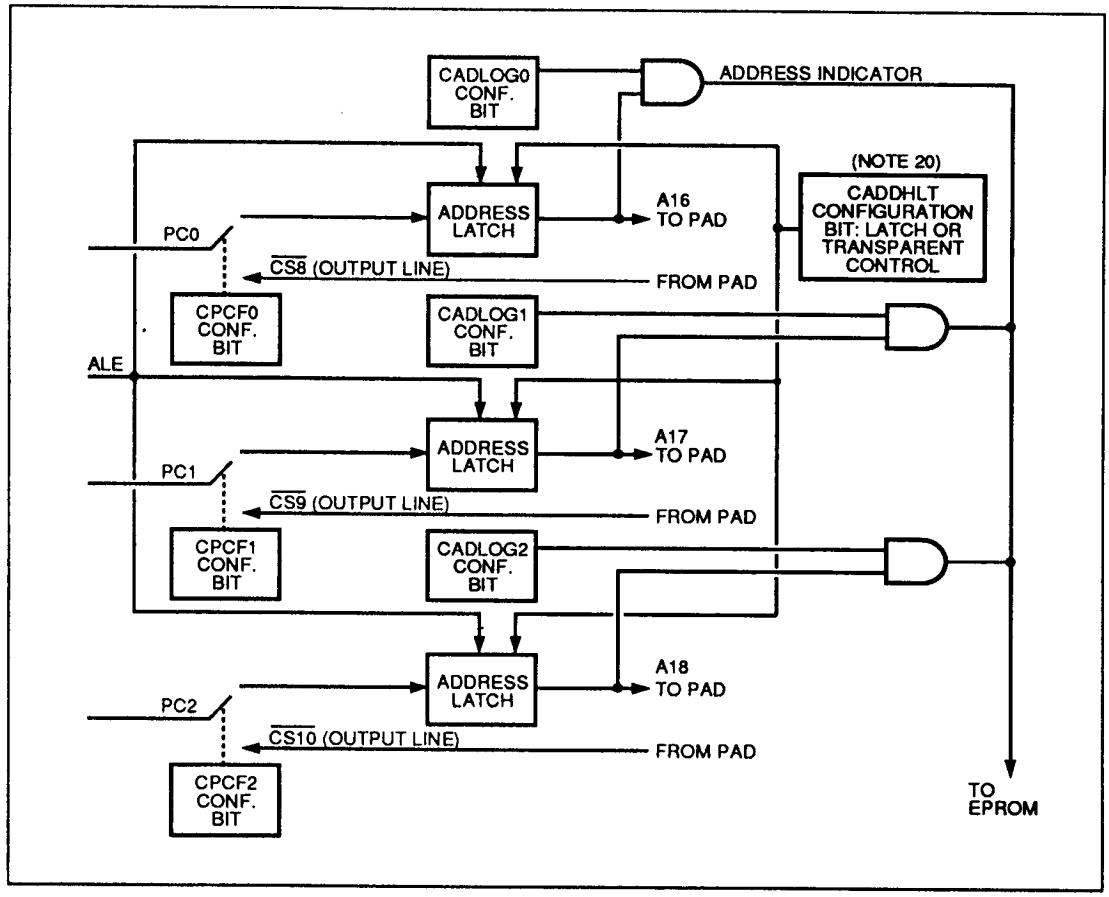
Register Name	Byte Size Access of the I/O Port Registers Offset from the CSIOPORT
Pin Register of Port A	+ 2 (accessible during read operation only)
Direction Register of Port A	+ 4
Data Register of Port A	+ 6
Pin Register of Port B	+ 3 (accessible during read operation only)
Direction Register of Port B	+ 5
Data Register of Port B	+ 7
Page Register	+18

Table 7. I/O Port Addresses in a 16-bit Data Bus Mode[18,19] (PSD30X)

Register Name	Word Size Access of the I/O Port Registers Offset from the CSIOPORT
Pin Register of Ports B and A	+ 2 (accessible during read operation only)
Direction Register of Ports B and A	+ 4
Data Register of Ports B and A	+ 6

NOTES: 18. When the data bus width is 16, Port B registers can only be accessed if the $\overline{BHE}$ signal is low.
19. I/O Ports A and B are still byte-addressable, as shown in Table 6. For I/O Port B register access, $\overline{BHE}$ must be low.

Figure 7. Port C Structure



NOTES: 20. The CADDHLT configuration bit determines if A18–A16 are transparent via the latch, or if they must be latched by the trailing edge of the ALE strobe.

21. PSD3X2/3X3: Individual pins can be configured independently as address or logic inputs (CADLOG, bits 0–2).
PSD3X1: All Port C pins are either address or logic inputs (CATD).

Port Functions (Cont.)

ALE/AS and AD0/A0–AD15/A15 in Non-Multiplexed Modes (PSD3X2/3X3)

In non-multiplexed modes, AD0/A0–AD15/A15 are address inputs only and can become transparent (CLOT = 0) or ALE dependent (CLOT = 1). In transparent mode, the ALE/AS pin can be used as an additional logic input to the PADs. The non-multiplexed ALE dependent mode is useful in applications for which the host processor has a multiplex address/data bus and AD0/A0–AD7/A7 are not multiplexed with A0–A7 but rather are multiplexed with other address lines. In these applications, Port A serves as a data bus and each of its pins can be directly connected to the corresponding host's multiplexed pin, where that data bit is expected. (See Table 8.)

ALE/AS and AD0/A0–AD7/A7 in Non-Multiplexed Modes (PSD31X)

In non-multiplexed modes, A0–A15 are address inputs only and can become transparent (CLOT = 0) or ALE dependent (CLOT = 1). In transparent mode, the ALE/AS pin can be used as an additional logic input to the PADs. The non-multiplexed ALE dependent mode is useful in applications for which the host processor has a multiplex address/data bus and AD0/A0–AD7/A7 are not multiplexed with A0–A7 but rather are multiplexed with other address lines. In these applications, Port A serves as a data bus and each of its pins can be directly connected to the corresponding host's multiplexed pin, where that data bit is expected. (See Table 8.)

A16–A19 Inputs

If one or more of the pins PC0, PC1 PC2 and $\overline{CSI}$/A19 are configured as inputs, the configuration bits CADDHLT and CATD define their functionality inside the part. CADDHLT determines if these inputs are to be latched by the trailing edge of the ALE or AS signal (CADDHLT = 1), or enabled into the PSD3XX at all times (CADDHLT = 0, transparent mode). CATD determines whether these lines are high-order address lines, that take part in the derivation of memory and I/O select signals inside the chip (CATD = 1), or logic input lines that have no impact on memory or I/O selections (CATD = 0). Logic input lines typically participate in the Boolean expressions implemented in the PAD.

EPROM

The EPROM has 8 banks of memory. Each bank can be placed in any address location by programming the PAD. Bank0–Bank7 is selected by PAD outputs ES0–ES7, respectively.

Device	EPROM Size	EPROM Architecture		EPROM Bank Architecture (8 ea)	
		x8	x16	x8	x16
PSD301	256Kb	32K x 8	16K x 16	4K x 8	2K x 16
PSD311	256Kb	32K x 8	–	4K x 8	–
PSD302	512Kb	64K x 8	32K x 16	8K x 8	4K x 16
PSD312	512Kb	64K x 8	–	8K x 8	–
PSD303	1Mb	128K x 8	64K x 16	16K x 8	8K x 16
PSD313	1Mb	128K x 8	–	16K x 8	–

SRAM

Each PSD3XX device has 16K bits of SRAM. Depending on the configuration of the data bus, the SRAM organization can be 2K x 8 (8-bit data bus) or 1K x 16 (16-bit data bus). The SRAM is selected by the RS0 output of the PAD.

Memory Paging (PSD3X2/3X3)

The page register consists of four flip-flops, which can be read from, or written to, through the I/O address space (CSIOPORT). The page register is connected to the D3–D0 lines. The Page Register address is CSIOPORT + 18H. The page register outputs are P3–P0, which are fed into the PAD. This enables the host microcontroller to enlarge its address space by a factor of 16 (there can be a maximum of 16 pages). See Figure 8.

Figure 8. Page Register (PSD3X2/3X3)

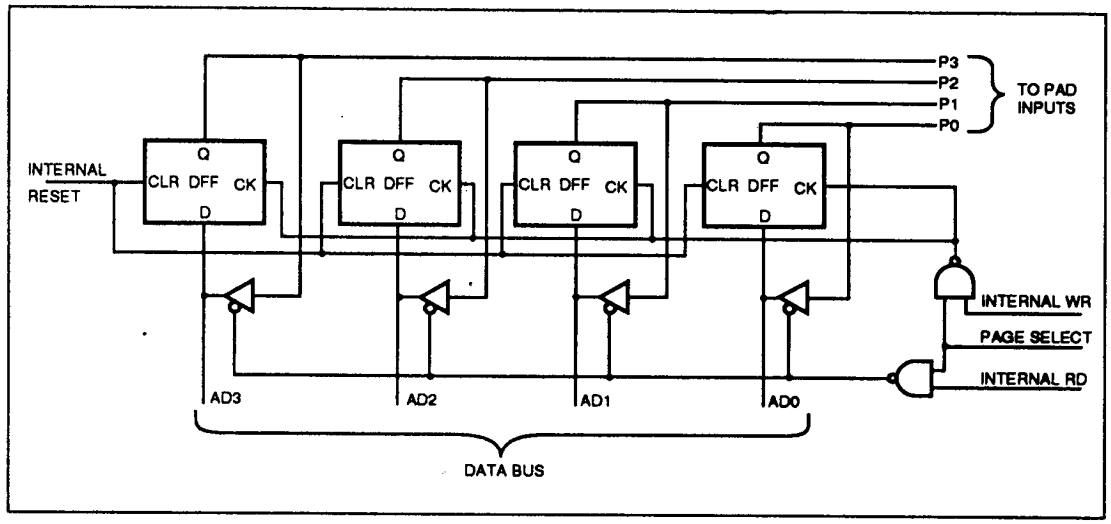


Table 8. Signal Latch Status in All Operating Modes

Signal Name	Configuration Bits	Configuration Mode	Signal Latch Status
AD8/A8–AD15/A15	CDATA , CADDRDAT, CLOT = 0	8-bit data, non-multiplexed	Transparent
	CDATA, CADDRDAT = 0, CLOT = 1		ALE Dependent
	CDATA = 1, CADDRDAT, CLOT = 0	16-bit data, non-multiplexed	Transparent
	CDATA = 1, CADDRDAT = 0, CLOT = 1		ALE Dependent
	CDATA = 0, CADDRDAT = 1	8-bit data, multiplexed	Transparent
	CDATA = 1, CADDRDAT = 1	16-bit data, multiplexed	ALE Dependent
AD0/A0-AD7/A7	CADDRDAT = 0, CLOT = 0	non-multiplexed modes	Transparent
	CADDRDAT = 0, CLOT = 1		ALE Dependent
	CADDRDAT = 1	multiplexed modes	ALE Dependent
$\overline{BHE}$/PSEN	CDATA = 0	8-bit data, $\overline{PSEN}$ is active	Transparent
	CDATA = 1, CADDRDAT = 0	16-bit data, non-multiplexed mode, $\overline{BHE}$ is active	Transparent
A19 and PC2–PC0	CDATA = 1, CADDRDAT = 1	16-bit data, multiplexed mode, $\overline{BHE}$ is active	ALE Dependent
	CADDHLT = 0	A16–A19 can become logic inputs	Transparent
	CADDHLT = 1	A16–A19 can become multiplexed address lines	ALE Dependent

Control Signals

The PSD3XX control signals are $\overline{WR}/V_{PP}$ or R/$\overline{W}$, $\overline{RD}$/E or $\overline{RD}$/E/$\overline{DS}$, ALE, $\overline{BHE}$/$\overline{PSEN}$ or $\overline{PSEN}$, $\overline{RESET}$, and A19/$\overline{CSI}$. Each of these signals can be configured to meet the output control signal requirements of various microcontrollers.

$\overline{WR}/V_{PP}$ or R/$\overline{W}$

In operational mode, this signal can be configured as $\overline{WR}$ or R/$\overline{W}$. As $\overline{WR}$, all write operations are activated by an active low signal on this pin. As R/$\overline{W}$, the pin operates with the E strobe of the $\overline{RD}$/E/$\overline{DS}$ or $\overline{RD}$/E pin. When R/$\overline{W}$ is high, an active high signal on the $\overline{RD}$/E/$\overline{DS}$ or $\overline{RD}$/E pin performs a read operation. When R/$\overline{W}$ is low, an active high signal on the $\overline{RD}$/E/$\overline{DS}$ or $\overline{RD}$/E pin performs a write operation.

$\overline{RD}$/E/$\overline{DS}$ (or $\overline{RD}$/E on PSD3X1)

In operational mode, this signal can be configured as $\overline{RD}$, E, or $\overline{DS}$. As $\overline{RD}$, all read operations are activated by an active low signal on this pin. As E, the pin operates with the R/$\overline{W}$ signal of the $\overline{WR}/V_{PP}$ or R/$\overline{W}$ pin. When R/$\overline{W}$ is high, an active high signal on the $\overline{RD}$/E/$\overline{DS}$ pin performs a read operation. When R/$\overline{W}$ is low, an active high signal on the $\overline{RD}$/E/$\overline{DS}$ pin performs a write operation.

As $\overline{DS}$, the pin functions with the R/$\overline{W}$ signal as an active low data strobe signal. As $\overline{DS}$, the R/$\overline{W}$ defines the mode of operation (Read or Write).

ALE or AS

ALE polarity is programmable. When programmed to be active high, a high on the pin causes the input address latches, Port A address latches, Port C, and A19 address latches to be transparent. The falling edge of ALE locks the information into the latches. When ALE is programmed to be active low, a low on the pin causes the input address latches, Port A address latches, Port C, and A19 address latches to be transparent. The rising edge of ALE locks the appropriate information into the latches.

$\overline{BHE}$/$\overline{PSEN}$

This pin's function depends on the PSD3XX data bus width. If it is 8 bits, the pin is $\overline{PSEN}$; if it is 16 bits, the pin is $\overline{BHE}$. In 8-bit mode, the $\overline{PSEN}$ function enables the user to work with two address spaces: program memory and data memory (if COMB/SEP = 1). In this mode, an active low signal on the PSEN pin causes the EPROM to be read if selected. The SRAM and I/O ports read operation are done by $\overline{RD}$ low (CRRWR = 0), or by E high and R/$\overline{W}$ high (CRRWR = 1, CEDS = 0) or by $\overline{DS}$ low and R/$\overline{W}$ high (CRRWR, CEDS = 1).

Whenever a member of the 8031 family (or any other similar microcontroller) is used, the $\overline{PSEN}$ pin must be connected to the $\overline{PSEN}$ pin of the microcontroller.

If COMB/SEP = 0, the address spaces of the program and the data are combined. In this configuration (except for the 8031-type case mentioned above), the $\overline{PSEN}$ pin must be tied high to V_{CC}, and the EPROM, SRAM, and I/O ports are read by $\overline{RD}$ low (CRRWR = 0), or by E high and R/$\overline{W}$ high (CRRWR = 1, CEDS = 0) or by $\overline{DS}$ low and R/$\overline{W}$ high (CRRWR, CEDS = 1). See Figures 9 and 10.

In $\overline{BHE}$ mode, this pin enables accessing of the upper-half byte of the data bus. A low on this pin enables a write or read operation to be performed on the upper half of the data bus (see Table 9).

RESET

This is an asynchronous input pin that clears and initializes the PSD3XX. Reset polarity is programmable (active low or active high). Whenever the PSD3XX reset input is driven active for at least 100 ns, the chip is reset. The PSD3XX must be reset before it can be used. Tables 10a, 10b and 11 indicate the state of the part during and after reset.

Control Signals (Cont.)

A19/$\overline{CSI}$

When configured as $\overline{CSI}$, a high on this pin deselects, and powers down, the chip. A low on this pin puts the chip in normal operational mode. For PSD3XX states during the power-down mode, see Tables 12 and 13, and Figure 11.

In A19 mode, the pin is an additional input to the PAD. It can be used as an address line (CADLOG3 = 1) or as a general-purpose logic input (CADLOG3 = 0). A19 can be configured as ALE dependent or as transparent input (see Table 8). In this mode, the chip is always enabled.

Figure 9. Combined Address Space

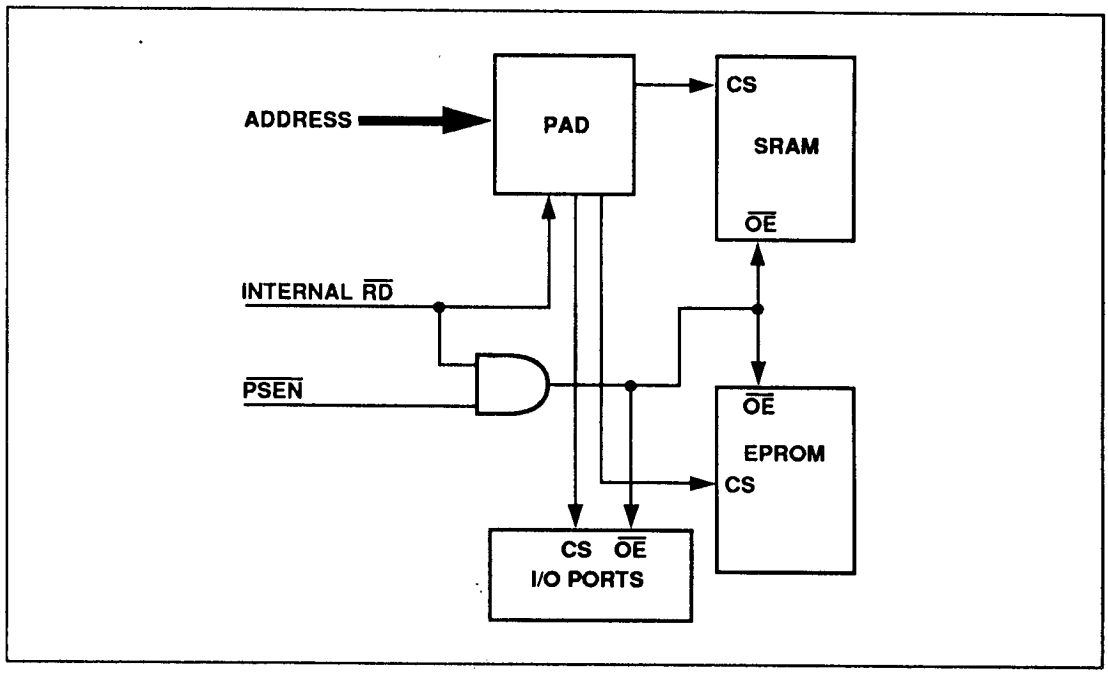


Table 9. High/Low Byte Selection Truth Table (In 16-Bit Configuration Only)

$\overline{BHE}$	A_0	Operation
0	0	Whole Word
0	1	Upper Byte From/To Odd Address
1	0	Lower Byte From/To Even Address
1	1	None

Figure 10. 8031-Type Separate Code and Data Address Spaces

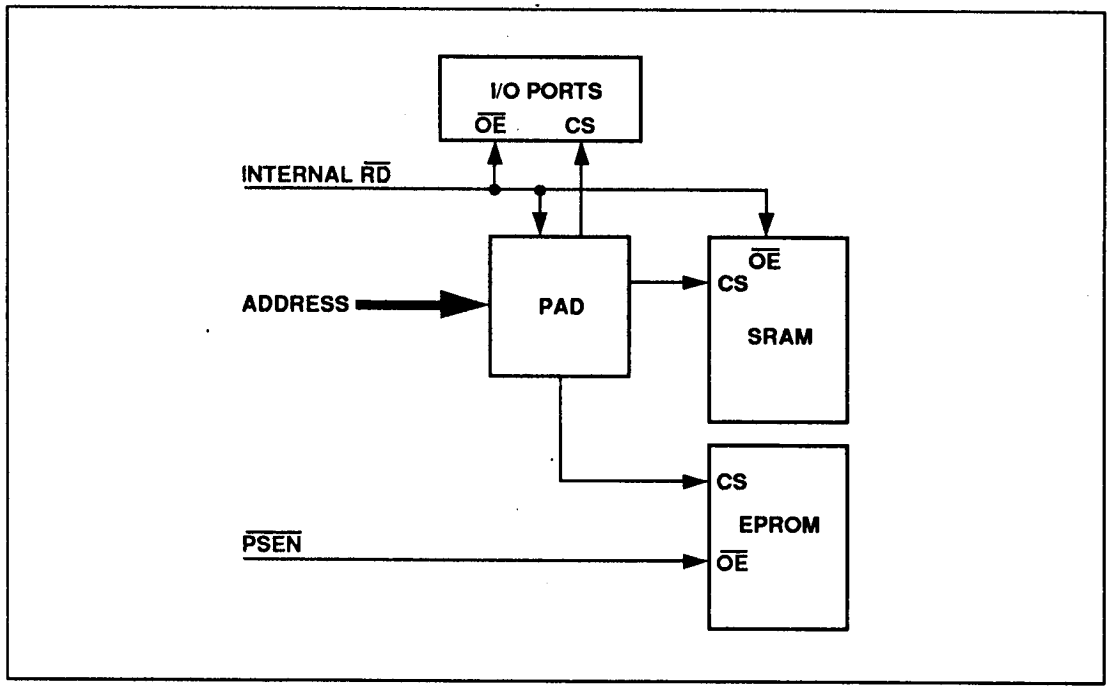


Table 10a. Signal States During Reset Cycle (RESET)

Signal	Condition
AD0/A0–AD15/A15	Input
PA0–PA7 (Port A)	Input
PB0–PB7 (Port B)	Input
PC0–PC2 (Port C)	Input

Table 10b. Signal States After Reset Cycle (RESET)

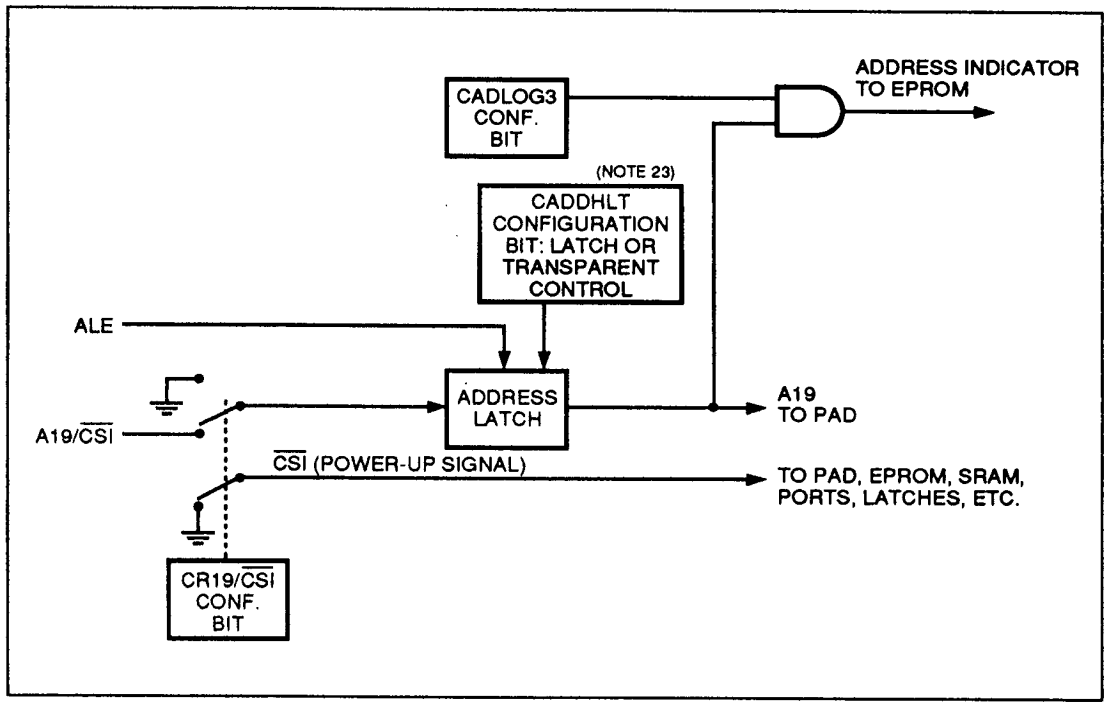
Signal	Configuration Mode	Condition
AD0/A0–AD7/A7	All	Input
A8–A15	All	Input
PA0–PA7) (Port A	I/O Tracking AD0/A0–AD7 Address outputs A0–A7	Input Input Low
PB0–PB7 (Port B)	I/O $\overline{CS7}$–$\overline{CS0}$ CMOS outputs $\overline{CS7}$–$\overline{CS0}$ open drain outputs	Input High Tri-stated
PC0–PC2 (Port C)	Address inputs A16–A18 $\overline{CS8}$–$\overline{CS10}$ CMOS outputs	Input High

Table 11. Internal States During and After Reset Cycle

Component	Signals	Contents
PAD	$\overline{CS0}$–$\overline{CS10}$	All = 1 (Note 22)
	CSADIN, CSADOUT1, CSADOUT2, CSIOPORT, RS0, ES0 – ES7	All = 0 (Note 22)
Data register A	n/a	0
Direction register A	n/a	0
Data register B	n/a	0
Direction register B	n/a	0

NOTE: 22. All PAD outputs are in a non-active state.

Figure 11. A19/$\overline{CSI}$ Cell Structure



NOTES: 23. The CADDHLT configuration bit determines if A19–A16 are transparent via the latch, or if they must be latched by the trailing edge of the ALE strobe.

Table 12a. Signal States During Power-Down Mode (PSD30X)

Signal	Configuration Mode	Condition
AD0/A0–AD15/A15	All	Input
PA0–PA7	I/O Tracking AD0/A0–AD7/A7 Address outputs A0–A7	Unchanged Input All 1's
PB0–PB7	I/O $\overline{CS0}$–$\overline{CS7}$ CMOS outputs $\overline{CS0}$–$\overline{CS7}$ open drain outputs	Unchanged All 1's Tri-stated
PC0–PC2	Address inputs A18–A16 $\overline{CS8}$–$\overline{CS10}$ CMOS outputs	Input All 1's

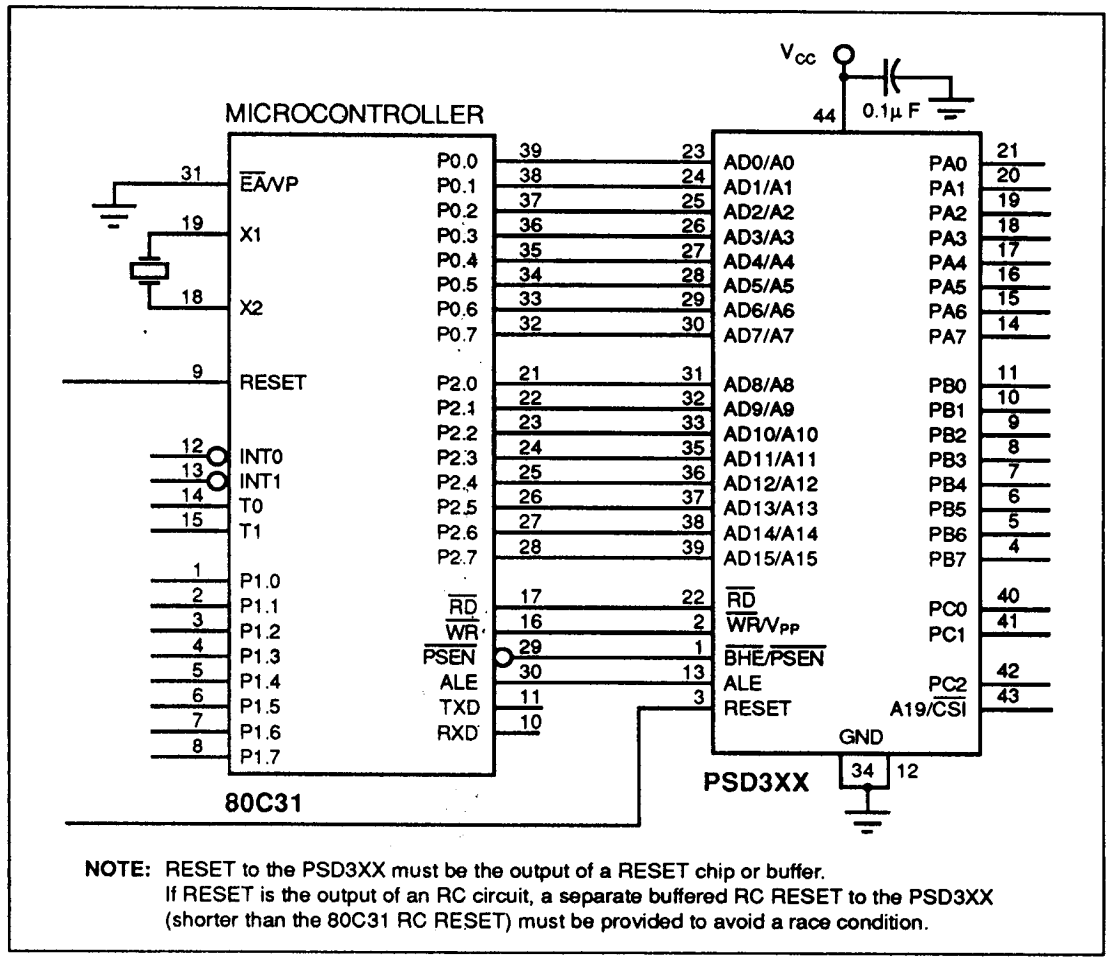
Table 12b. Signal States During Power-Down Mode (PSD31X)

Signal	Configuration Mode	Condition
AD0/A0–AD7/A7	All	Input
A8–A15	All	Input
PA0–PA7	I/O Tracking AD0/A0–AD7/A7 Address outputs A0–A7	Unchanged Input All 1's
PB0–PB7	I/O $\overline{CS0}$–$\overline{CS7}$ CMOS outputs CS0–CS7 open drain outputs	Unchanged All 1's Tri-stated
PC0–PC2	Address inputs A18–A16 $\overline{CS8}$–$\overline{CS10}$ CMOS outputs	Input All 1's

Table 13. Internal States During Power-Down

Component	Signals	Contents
PAD	$\overline{CS0}$–$\overline{CS10}$	All 1's (deselected)
	CSADIN, CSADOUT1, CSADOUT2, CSIOPORT, RS0, ES0–ES7	All 0's (deselected)
Data register A Direction register A Data register B Direction register B	n/a n/a n/a n/a	All unchanged

Figure 12. PSD3XX Interface With Intel's 80C31



NOTE: RESET to the PSD3XX must be the output of a RESET chip or buffer. If RESET is the output of an RC circuit, a separate buffered RC RESET to the PSD3XX (shorter than the 80C31 RC RESET) must be provided to avoid a race condition.

The configuration bits for Figure 12 are:

CALE	0	COMB/SEP	0 or 1 (both valid)
CDATA	0	CRRWR	0
CADDRDAT	1	CEDS	0
CRESET	1		

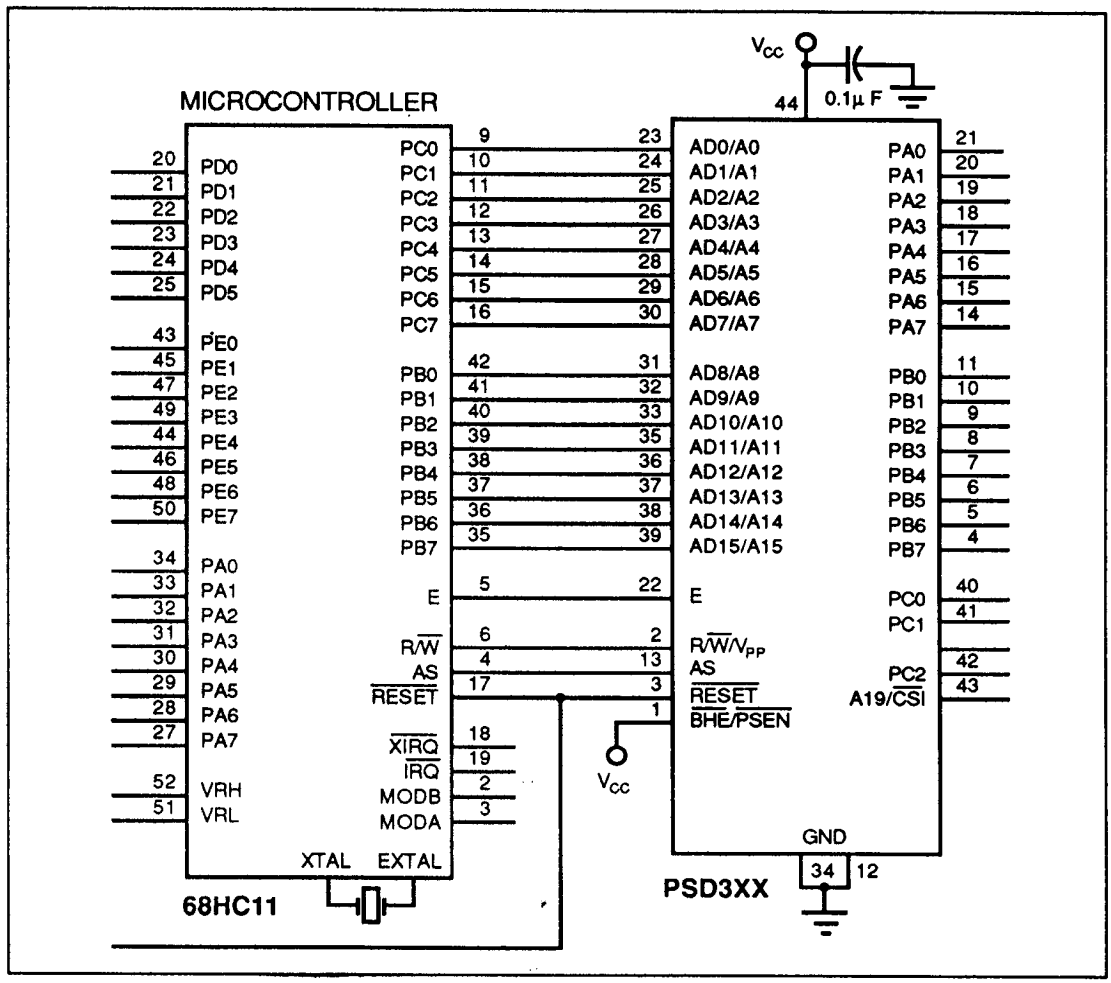
All other configuration bits may vary according to the application requirements.

System Applications

In Figure 12, the PSD3XX is configured to interface with Intel's 80C31, which is a 16-bit address/8-bit data bus microcontroller. Its data bus is multiplexed with the low-order address byte. The 80C31 uses signals $\overline{RD}$ to read from data memory and $\overline{PSEN}$ to read from code memory. It uses $\overline{WR}$ to write into the data memory. It also uses active high reset and ALE signals. The rest of the configuration bits as well as the unconnected signals (not shown) are application specific and, thus, user dependent.

In Figure 13, the PSD3XX is configured to interface with Motorola's 68HC11, which is a 16-bit address/8-bit data bus microcontroller. Its data bus is multiplexed with the low-order address byte. The 68HC11 uses E and R/W signals to derive the read and write strobes. It uses the term AS (address strobe) for the address latch pulse. RESET is an active low signal. The rest of the configuration bits as well as the unconnected signals (not shown) are specific and, thus, user dependent.

Figure 13. PSD3XX Interface With Motorola's 68HC11



The configuration bits for Figure 13 are:

CALE	0	COMB/SEP	0
CDATA	0	CRRWR	1
CADDRDAT	1	CEDS	0
CRESET	0		

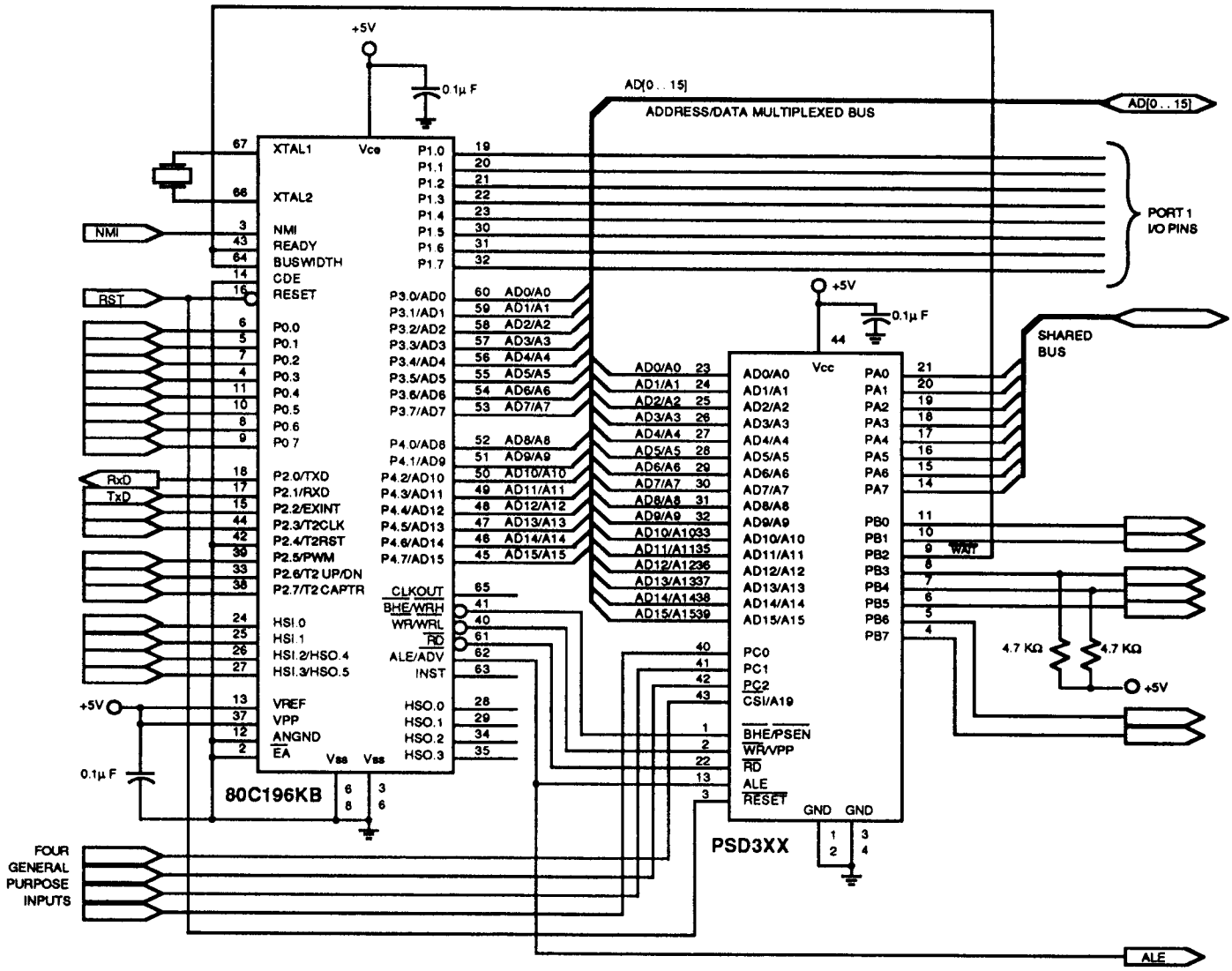
All other configuration bits may vary according to the application requirements.

System Applications (Cont.)

In Figure 14, the PSD3XX is configured to work directly with Intel's 80C196KB microcontroller, which is a 16-bit address/16-bit data bus processor. Address and data lines multiplexed. In the example shown, all configuration bits are set. The PSD3XX is configured to use PC0, PC1, PC2, and $\overline{CSI}$/A19 as A16, A17, A18, and A19 inputs, respectively. These signals are independent of the ALE pulse (latch-transparent). They are used as four general-purpose logic inputs that take part in the PAD equations implementation.

Port A is configured to work in the special track mode, in which (for certain conditions) PA0–PA7 tracks lines AD0/A0–AD7/A7. Port B is configured to generate $\overline{CS0}$–$\overline{CS7}$. In this example, PB2 serves as a $\overline{WAIT}$ signal that slows down the 80C196KB during the access of external peripherals. These 8-bit wide peripherals are connected to the shared bus of Port A. The $\overline{WAIT}$ signal also drives the buswidth input of the microcontroller, so that every external peripheral cycle becomes an 8-bit data bus cycle. PB3 and PB4 are open-drain output signals; thus, they are pulled up externally.

Figure 14.
PSD3XX Interface With Intel's 80C196KB.



The configuration bits for Figure 14 are:

CALE	0	CSECURITY	Don't care
CDATA	1	CPCF2, CPCF1, CPCF0	0, 0, 0
CADDRDAT	1	CPACOD7–CPACOD0	00H
CPAF1	Don't care	CPBF7–CPBF0	00H
CPAF2	1	CPBCOD7–CPBCOD0	18H
CA19/$\overline{CSI}$	1	CEDS	0
CRRWR	0	CADLOG3—CADLOG0	0H
COMB/SEP	0		
CADDHLT	0		
CRESET	0		