

Am29841 - 46

High Performance Bus Interface Latches

DISTINCTIVE CHARACTERISTICS

- High-speed parallel latches
 - Noninverting transparent $t_{PD} = 5.25\text{ns typ}$
 - Inverting transparent $t_{PD} = 6.0\text{ns typ}$
- Buffered common latch enable, clear and preset input
- Three-state outputs glitch-free during power-up and down. Outputs have Schottky clamp to ground
- 48mA Commercial I_{OL} , 32mA MIL I_{OL}
- Low input/output capacitance
 - 6pF inputs (typical)
 - 8pF outputs (typical)
- I_{OH} specified 2.0V and 2.4V

GENERAL DESCRIPTION

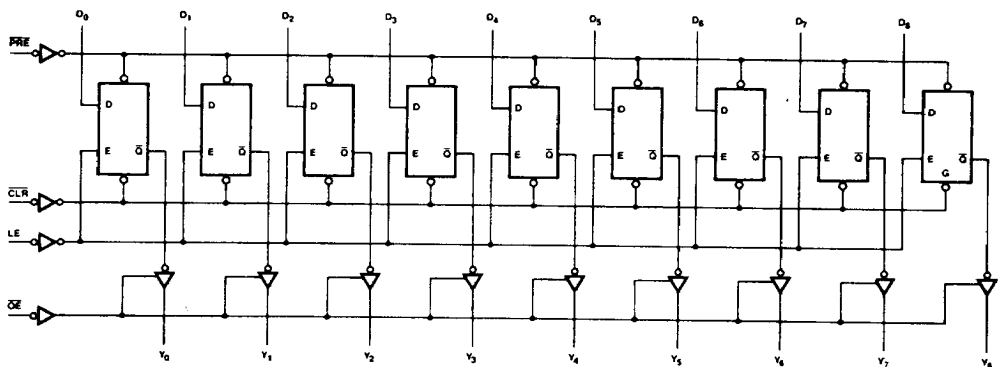
The Am29840 Series bus interface latches are designed to eliminate the extra packages required to buffer existing latches and provide extra data width for wider address/data paths or buses carrying parity. The Am29841 and Am29842 are buffered, 10-bit wide versions of the popular '373 function. The Am29843 and Am29844 are 9-bit wide buffered latches with Preset (PRE) and Clear (CLR) – ideal for parity bus interfacing in high performance systems. The Am29845 and Am29846 are 8-bit buffered latches with all the '843/4 controls plus multiple enables ($\overline{OE}_1, \overline{OE}_2, \overline{OE}_3$)

to allow multiuser control of the interface, e.g., $\overline{CS}$, DMA, and RD/WR. They are ideal for use as an output port requiring high I_{OL}/I_{OH} .

All of the Am29800 high performance interface family products are designed for high capacitance load drive capability while providing low capacitance bus loading at both inputs and outputs. All inputs are Schottky diode inputs, and all outputs are designed for low capacitance bus loading in the high impedance state.

BLOCK DIAGRAM

Am29843



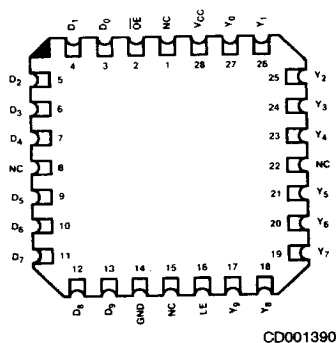
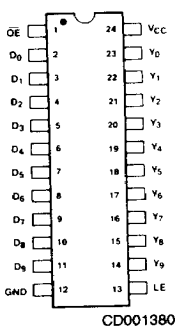
BD001050

PRODUCT SELECTOR GUIDE

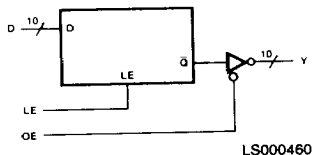
	Device		
	10-Bit	9-Bit	8-Bit
Noninverting	Am29841	Am29843	Am29845
Inverting	Am29842	Am29844	Am29846

CONNECTION DIAGRAM Top View

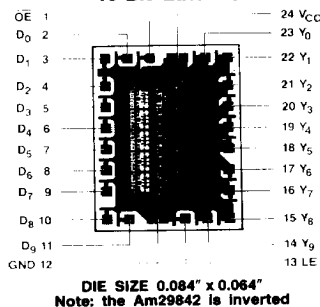
Am29841/Am29842 10-BIT LATCHES



LOGIC SYMBOL



METALLIZATION AND PAD LAYOUT Am29841* 10-Bit Latches



ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

Am29841 - 46

D

C

B

Screening Option
Blank - Standard processing
B - Burn-in

Temperature (See Operating Range)
C - Commercial (0°C to +70°C)
M - Military (-55°C to +125°C)

Package
D - 24-pin SLIM DIP (D-24-SLIM)
L - 28-pin Leadless Chip Carrier (L-28-1)
X - Dice

Device type
High Performance Bus Interface Latches

Valid Combinations

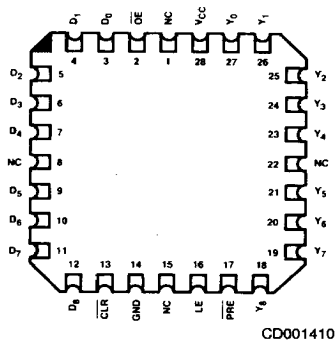
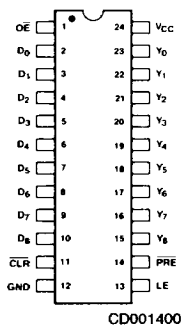
Am29841	DC, DCB, DM,
Am29842	DMB
Am29843	LC, LCB, LM,
Am29844	LMB
Am29845	XC, XM
Am29846	

Valid Combinations

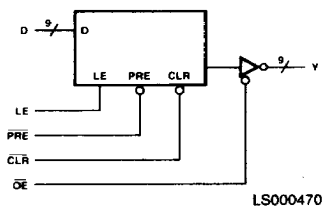
Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

CONNECTION DIAGRAM Top View

Am29843/Am29844 9-BIT LATCHES

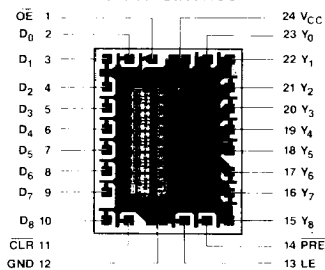


LOGIC SYMBOL



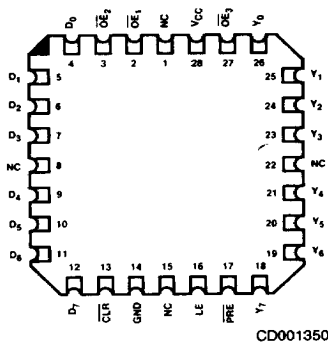
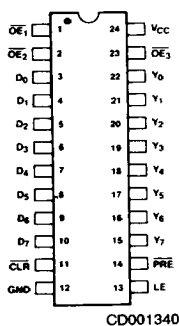
METALLIZATION AND PAD LAYOUT

Am29843* 9-Bit Latches

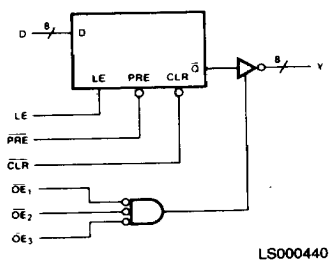


CONNECTION DIAGRAM Top View

Am29845/Am29846 8-BIT LATCHES

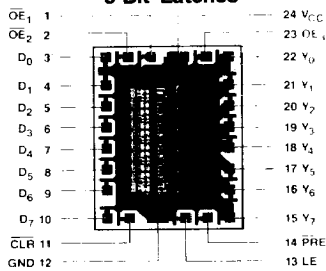


LOGIC SYMBOL



METALLIZATION AND PAD LAYOUT

Am29845* 8-Bit Latches



DIE SIZE 0.084" x 0.064"
Note: the Am29846 is inverted

PIN DESCRIPTION

Pin No.	Name	I/O	Description
Am29841/43/45 (Noninverting)			
11	CLR	I	When CLR is LOW, the outputs are LOW if OE is LOW. When CLR is HIGH, data can be entered into the latch.
	D _i	I	The latch data inputs.
13	LE	I	The latch enable input. The latches are transparent when LE is HIGH. Input data is latched on the HIGH-to-LOW transition.
	Y _i	O	The 3-state latch outputs.
1	OE	I	The output enable control. When OE is LOW, the outputs are enabled. When OE is HIGH, the outputs Y _i are in the high-impedance (off) state.
14	PRE	I	Preset line. When PRE is LOW, the outputs are HIGH if OE is LOW. Preset overrides CLR.
Am29842/44/46 (Inverting)			
11	CLR	I	When CLR is LOW, the outputs are LOW if OE is LOW. When CLR is HIGH, data can be entered into the latch.
	D _i	I	The latch inverting data inputs.
13	LE	I	The latch enable input. The latches are transparent when LE is HIGH. Input data is latched on the HIGH-to-LOW transition.
	Y _i	O	The 3-state latch outputs.
1	OE	I	The output enable control. When OE is LOW, the outputs are enabled. When OE is HIGH, the outputs Y _i are in the high-impedance (off) state.
14	PRE	I	Preset line. When PRE is LOW, the outputs are HIGH if OE is LOW. Preset overrides CLR.

FUNCTION TABLES

29841/43/45 (Noninverting)

Inputs					Internal Outputs		Function
CLR	PRE	OE	LE	D _i	Q _i	Y _i	
H	H	H	X	X	X	Z	Hi-Z
H	H	H	H	L	L	Z	Hi-Z
H	H	H	H	H	H	Z	Hi-Z
H	H	H	L	X	NC	Z	Latched (Hi-Z)
H	H	L	H	L	L	L	Transparent
H	H	L	H	H	H	H	Transparent
H	H	L	L	X	NC	NC	Latched
H	L	L	X	X	H	H	Preset
L	H	L	X	X	L	L	Clear
L	L	L	X	X	H	H	Preset
L	H	H	L	X	L	Z	Latched (Hi-Z)
H	L	H	L	X	H	Z	Latched (Hi-Z)

29842/44/46 (Inverting)

Inputs					Internal Outputs		Function
CLR	PRE	OE	LE	D _i	Q _i	Y _i	
H	H	H	X	X	X	Z	Hi-Z
H	H	H	H	H	L	Z	Hi-Z
H	H	H	H	L	H	Z	Hi-Z
H	H	H	L	X	NC	Z	Latched (Hi-Z)
H	H	L	H	H	L	L	Transparent
H	H	L	H	L	H	H	Transparent
H	H	L	L	X	NC	NC	Latched
H	L	L	X	X	H	H	Preset
L	H	L	X	X	L	L	Clear
L	L	L	X	X	H	H	Preset
L	H	H	L	X	L	Z	Latched (Hi-Z)
H	L	H	L	X	H	Z	Latched (Hi-Z)

ABSOLUTE MAXIMUM RATINGS

Storage Temperature -65°C to +150°C
 Ambient Temperature with
 Power Applied -55°C to +125°C
 Supply Voltage to Ground Potential
 Continuous -0.5V to +7.0V
 DC Voltage Applied to Outputs
 for High Output State -0.5V to V_{CCmax}
 DC input voltage -0.5V to +5.5V
 DC Output Current, into Outputs 100mA
 DC input Current -30mA to +5.0mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Temperature 0°C to +70°C
 Supply Voltage +4.75V to +5.25V

Military (M) Devices

Temperature -55°C to +125°C
 Supply Voltage +4.5V to +5.5V

Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

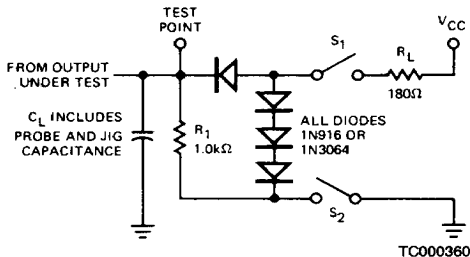
Parameters	Description	Test Conditions (Note 2)	Min	Typ (Note 1)	Max	Units
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{MIN}$ $V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -15\text{mA}$ $I_{OH} = -24\text{mA}$	2.4 2.0	3.3 3.1	Volts
V_{OL}	Output LOW Voltage	$V_{CC} = \text{MIN}$ $V_{IN} = V_{IH}$ or V_{IL}	$MIL, I_{OL} = 32\text{mA}$ $COM'L, I_{OL} = 48\text{mA}$		0.5 0.5	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs	2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs			0.8	Volts
V_I	Input Clamp Voltage	$V_{CC} = \text{MIN}, I_{IN} = -18\text{mA}$			-1.2	Volts
I_{IL}	Input LOW Current	$V_{CC} = \text{MAX}, V_{IN} = 0.4\text{V}$			-1.0	mA
I_{IH}	Input HIGH Current	$V_{CC} = \text{MAX}, V_{IN} = 2.7\text{V}$			50	μA
I_I	Input HIGH Current	$V_{CC} = \text{MAX}, V_{IN} = 5.5\text{V}$			1.0	mA
I_{OZ}	Output Off-State (High Impedance) Output Current	$V_{CC} = \text{MAX}$	$V_O = 0.4\text{V}$ $V_O = 2.4\text{V}$		-50 50	μA
I_{SC}	Output Short Circuit Current ³	$V_{CC} = \text{MAX}$	-75		-250	mA
I_{CC}	Supply Current	$V_{CC} = \text{MAX}$ Outputs Open	Over Temperature Range +70 +125°C		120 110 100	mA

Notes: 1. All typical values are $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$.

2. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

3. Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

SWITCHING TEST CIRCUIT



SWITCHING CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description	Test Conditions (Note 4)	COMMERCIAL		MILITARY		Units
			Min	Max	Min	Max	
t_{PLH} (Am29841, 3, 5)	Data (D_i) to Output Y_i (LE = HIGH)	$C_L = 50\text{pF}$	3.5	9.5	3.5	11	ns
t_{PHL}			3.5	9.5	3.5	11	ns
t_{PLH}		$C_L = 300\text{pF}$		12.5		14	ns
t_{PHL}				13		15	ns
t_s	Data to LE Setup Time	$C_L = 50\text{pF}$	2.5		2.5		ns
t_h	Data to LE Hold Time		2.5		3		ns
t_{PLH} (Am29842, 4, 6)	Data (D_i) to Output ($\bar{Y}_i$) (LE = HIGH)	$C_L = 50\text{pF}$	3.5	10		12	ns
t_{PHL}			3.5	10		12	ns
t_{PLH}		$C_L = 300\text{pF}$		12.5		14	ns
t_{PHL}				13		15	ns
t_{PLH}	Data to LE Setup Time	$C_L = 50\text{pF}$	2.5		2.5		ns
t_{PHL}	Data to LE Hold Time		2.5		3		ns
t_{PLH}	Latch Enable (LE) to Y_i	$C_L = 50\text{pF}$		12		16	ns
t_{PHL}				12		16	ns
t_{PLH}		$C_L = 300\text{pF}$		16		20	ns
t_{PHL}				16		20	ns
		$C_L = 50\text{pF}$					ns
							ns
t_{PLH}	Propagation Delay, Preset to Y_i			12		14	ns
t_s	Preset Recovery (PRE $\rightarrow$) Time			14		17	ns
t_{PHL}	Propagation Delay, Clear to Y_i			21		23	ns
t_s	Clear Recovery (CLR $\rightarrow$) Time			14		17	ns
t_{PWH}	LE Pulse Width	$C_L = 50\text{pF}$	6		6		ns
t_{PWL}	Preset Pulse Width		8		9		ns
t_{PWL}	Clear Pulse Width		8		9		ns
t_{ZH}	Output Enable Time $\overline{OE} \rightarrow Y_i$	$C_L = 300\text{pF}$		20		22	ns
t_{ZL}				23		25	ns
t_{ZH}		$C_L = 50\text{pF}$		14		15	ns
t_{ZL}				14		15	ns
t_{HZ}	Output Disable Time $\overline{OE} \rightarrow Y_i$	$C_L = 50\text{pF}$		15		15	ns
t_{LZ}				12		12	ns
t_{HZ}		$C_L = 5\text{pF}$		9		10	ns
t_{LZ}				9		10	ns

Note: 4. See test circuit and waveforms.

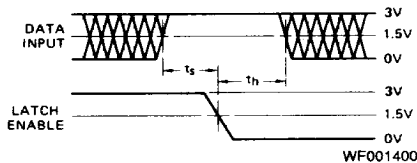
SWITCHING CHARACTERISTICS ($T_A = +25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$)

Parameters	Description	Test Conditions (Note 4)	Min	Typ	Max	Units
t_{PLH} (Am29841, 3, 5)	Data (D_i) to Output Y_i (LE = HIGH)	$C_L = 50\text{pF}$	3.5	5.7	8	ns
t_{PHL}			3.5	6.2	8	ns
t_{PLH}		$C_L = 300\text{pF}$		10	13	ns
t_{PHL}				10	13	ns
t_s	Data to LE Setup Time	$C_L = 50\text{pF}$	2.0	-0.2		ns
t_h	Data to LE Hold Time		2.5	0.7		ns
t_{PLH} (Am29842, 4, 6)	Data (D_i) to Output ($\bar{Y}_i$) (LE = HIGH)	$C_L = 50\text{pF}$	3.5	6.2	8.5	ns
t_{PHL}			3.5	6.5	8.5	ns
t_{PLH}		$C_L = 300\text{pF}$		10	13	ns
t_{PHL}				10	13	ns
t_s	Data to LE Setup Time	$C_L = 50\text{pF}$	2.5	0.3		ns
t_h	Data to LE Hold Time		2.5	0.2		ns
t_{PLH}	Latch Enable (LE) to Y_i	$C_L = 50\text{pF}$		8	10.5	ns
t_{PHL}				7.5	10	ns
t_{PLH}		$C_L = 300\text{pF}$			15	ns
t_{PHL}					15	ns
		$C_L = 50\text{pF}$				ns
						ns
t_{PLH}	Propagation Delay, Preset to Y_i			6.5	9	ns
t_s	Preset Recovery ($\overline{\text{PRE}}$ ) Time			7.3	12	ns
t_{PHL}	Propagation Delay, Clear to Y_i			15	18	ns
t_s	Clear Recovery ($\overline{\text{CLR}}$ ) Time			7.8	12	ns
t_{PWH}	LE Pulse Width	$C_L = 50\text{pF}$	4	2.5		ns
t_{PWL}	Preset Pulse Width		5			ns
t_{PWL}	Clear Pulse Width		6			ns
t_{ZH}	Output Enable Time $\overline{\text{OE}}$  to Y_i	$C_L = 300\text{pF}$			17	ns
t_{ZL}		$C_L = 50\text{pF}$			21	ns
t_{ZH}				7.3	12	ns
t_{ZL}	Output Disable Time $\overline{\text{OE}}$  to Y_i	$C_L = 50\text{pF}$		9.7	12	ns
t_{HZ}				10.4	14	ns
t_{LZ}		$C_L = 50\text{pF}$		4.7	11	ns
t_{HZ}				3.4	8	ns
t_{LZ}		$C_L = 5\text{pF}$ (Note 5)		3.8	8	ns

Note: 4. See test circuit and waveforms.
5. Not tested.

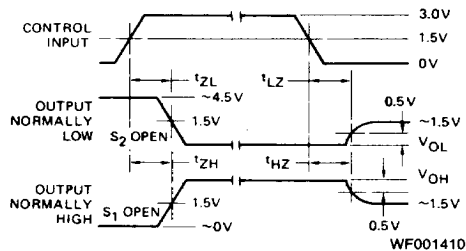
SWITCHING WAVEFORMS

SET UP, HOLD, AND RELEASE TIMES



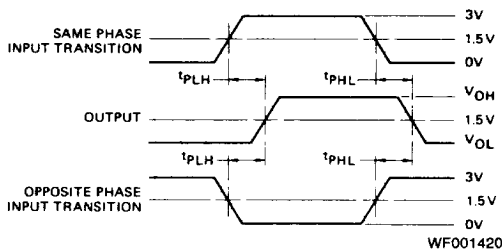
- Notes: 1. Diagram shown for HIGH data only. Output transition may be opposite sense.
2. Cross hatched area is don't care condition.

ENABLE AND DISABLE TIMES

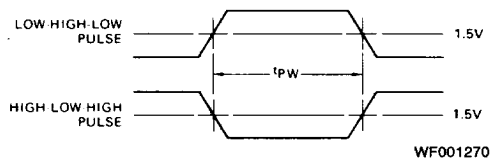


- Notes: 1. Diagram shown for Input Control Enable-LOW and Input Control Disable-HIGH.
2. S_1 and S_2 of Load Circuit are closed except where shown.

PROPAGATION DELAY



PULSE WIDTH



Note: Pulse Generator for All Pulses: Rate $\leq 10\text{MHz}$; $Z_0 = 50\Omega$; $t_r \leq 2.5\text{ns}$; $t_f \leq 2.5\text{ns}$.

INPUT/OUTPUT CURRENT INTERFACE CONDITIONS

