

Am29841A/Am29843A/Am29845A Am29941A/Am29943A/Am29945A

High-Performance Bus Interface Latches

DISTINCTIVE CHARACTERISTICS

- High-speed parallel latches
– transparent $t_{PD} = 5.0$ ns typical
- Buffered common latch enable, clear and preset input
- Three-state outputs glitch-free during power-up and down. Outputs have Schottky clamp to ground
- I_{OL} : 48 mA Commercial, 32 mA Military
- Higher speed, lower power versions of the Am29841, Am29843, and Am29845
- Am29900A DIP pinout option reduces lead inductance on V_{CC} and GND pins

GENERAL DESCRIPTION

The Am29841A, Am29843A, and Am29845A Buffered Latches are designed to eliminate the extra devices required to buffer stand alone latches and to provide extra data width for wider address/data paths or buses carrying parity. The Am29800A latches are produced with AMD's exclusive IMOX* bipolar process, and feature typical propagation delays of 5 ns, as well as high-capacitive drive capability.

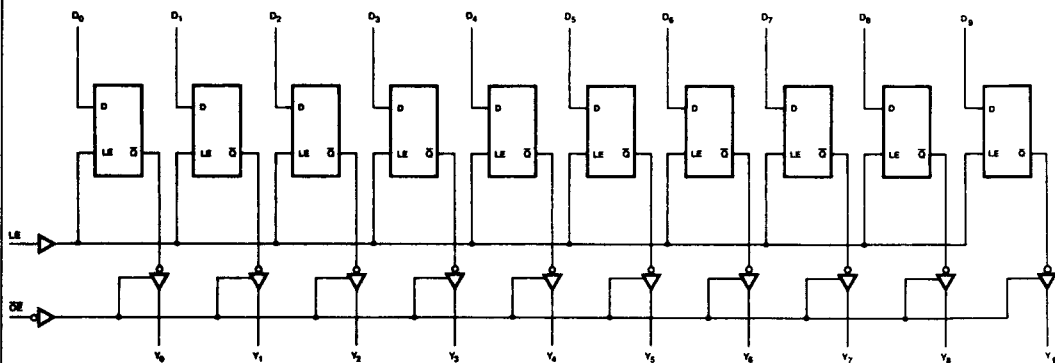
The Am29841A is a buffered, 10-bit version of the popular '373 function. The Am29843A is a 9-bit wide buffered latch with Preset (PRE) and Clear (CLR) — ideal for parity bus interfacing in high-performance microprogrammed sys-

tems. The Am29845A, an 8-bit buffered latch, has all the 9-bit controls, plus multiple enables ($\overline{OE}_1$, $\overline{OE}_2$, $\overline{OE}_3$), to allow multi-user control of the interface; e.g., CS, DMA, and RD/WR. The device is ideal for use as an output port requiring high I_{OL}/I_{OH} .

The Am29800A latches are available in the standard package options: DIPs, PLCCs, LCCs, and SOICs. In addition, a DIP pinout option, featuring center V_{CC} and GND pins, reduces the lead inductance of the V_{CC} and GND pins. The ordering part numbers for latches with this pinout are the Am29941A, Am29943A, and Am29945A; their pinouts are shown later in this data sheet.

BLOCK DIAGRAMS**

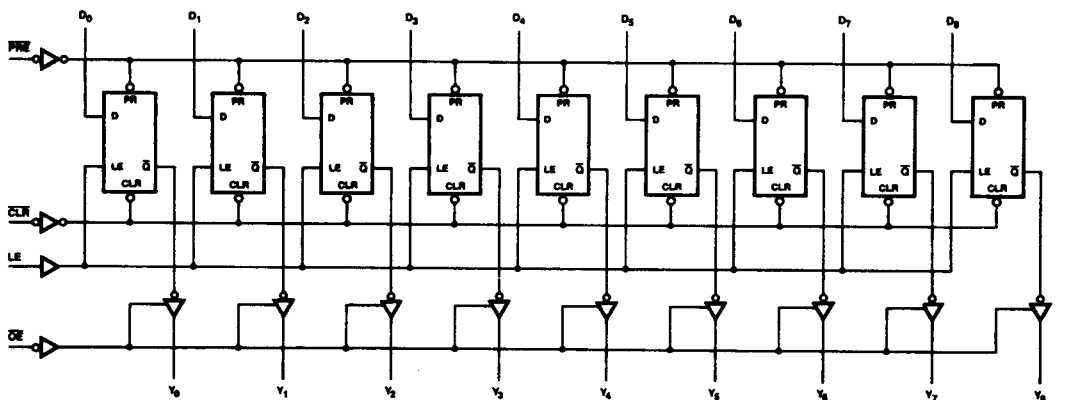
Am29841A



*IMOX is a trademark of Advanced Micro Devices, Inc.
**See following pages for additional Block Diagrams.

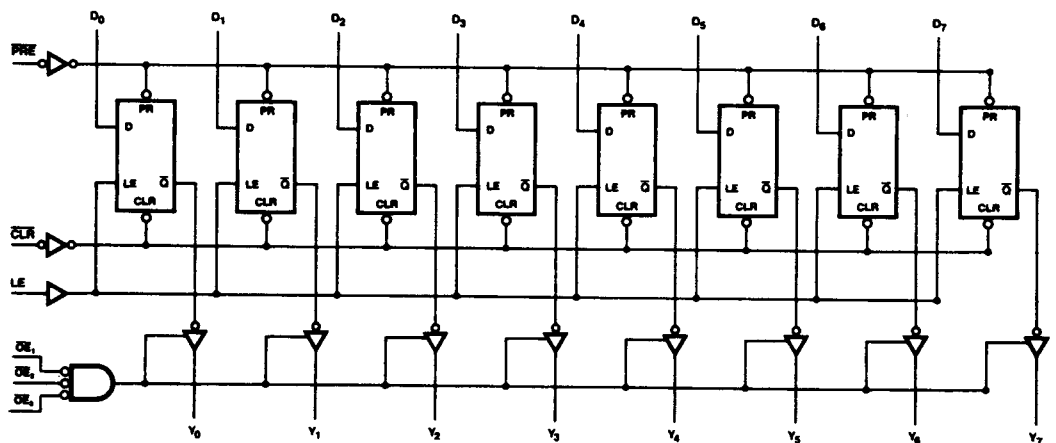
BLOCK DIAGRAMS (Cont'd.)

Am29843A



BD001057

Am29845A



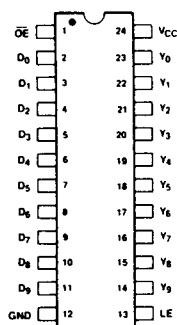
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CONNECTION DIAGRAMS Top View

Am29841A/Am29843A/Am29845A
Am29941A/Am29943A/Am29945A

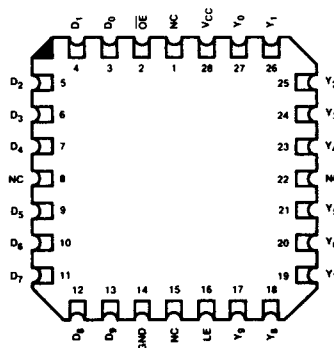
Am29841A

DIPs*



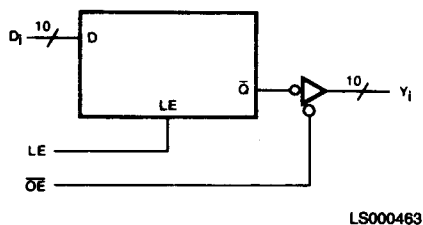
CD001380

LCC**

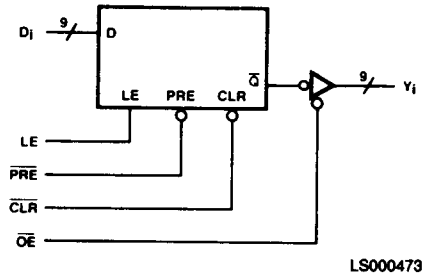


LOGIC SYMBOLS

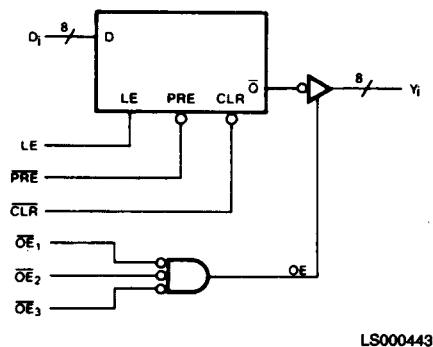
Am29841A



Am29843A



Am2985A



FUNCTION TABLES

Am29841A

Inputs			Internal	Outputs	Function
OE	LE	D _I	Q _I	Y _I	
H	X	X	X	Z	Hi-Z
H	H	L	H	Z	Hi-Z
H	H	H	L	Z	Hi-Z
H	L	X	NC	Z	Latched (Hi-Z)
L	H	L	H	L	Transparent
L	H	H	L	H	Transparent
L	L	X	NC	NC	Latched

H = HIGH
L = LOW
X = Don't Care

NC = No Change
Z = High Impedance

FUNCTION TABLES (Cont'd.)

Am29843A

Inputs					Internal	Outputs	Function
CLR	PRE	OE	LE	D ₁	Q ₁	Y ₁	
H	H	H	X	X	X	Z	Hi-Z
H	H	H	H	L	H	Z	Hi-Z
H	H	H	H	H	L	Z	Hi-Z
H	H	H	L	X	NC	Z	Latched (Hi-Z)
H	H	L	H	L	H	L	Transparent
H	H	L	H	H	L	H	Transparent
H	H	L	L	X	NC	NC	Latched
H	L	L	X	X	L	H	Preset
L	H	L	X	X	H	L	Clear
L	L	L	X	X	L	H	Preset
L	H	H	L	X	H	Z	Latched (Hi-Z)
H	L	H	L	X	L	Z	Latched (Hi-Z)

Am29845A

OE*	Inputs				Internal	Outputs	Function
	CLR	PRE	LE	D ₁	Q ₁	Y ₁	
L	H	H	X	X	X	Z	Hi-Z
L	H	H	H	L	H	Z	Hi-Z
L	H	H	H	H	L	Z	Hi-Z
L	H	H	L	X	NC	Z	Latched (Hi-Z)
H	H	H	H	L	H	L	Transparent
H	H	H	H	H	L	H	Transparent
H	H	H	L	X	NC	NC	Latched
H	H	L	X	X	L	H	Preset
H	L	H	X	X	H	L	Clear
H	L	L	X	X	L	H	Preset
L	L	H	L	X	H	Z	Latched (Hi-Z)
L	H	L	L	X	L	Z	Latched (Hi-Z)

*OE is an Active HIGH internal signal produced as follows:

OE ₁	OE ₂	OE ₃	OE
H	X	X	L
X	H	X	L
X	X	H	L
L	L	L	H

H = HIGH
L = LOW
NC = No Change
Z = High Impedance
X = Don't Care

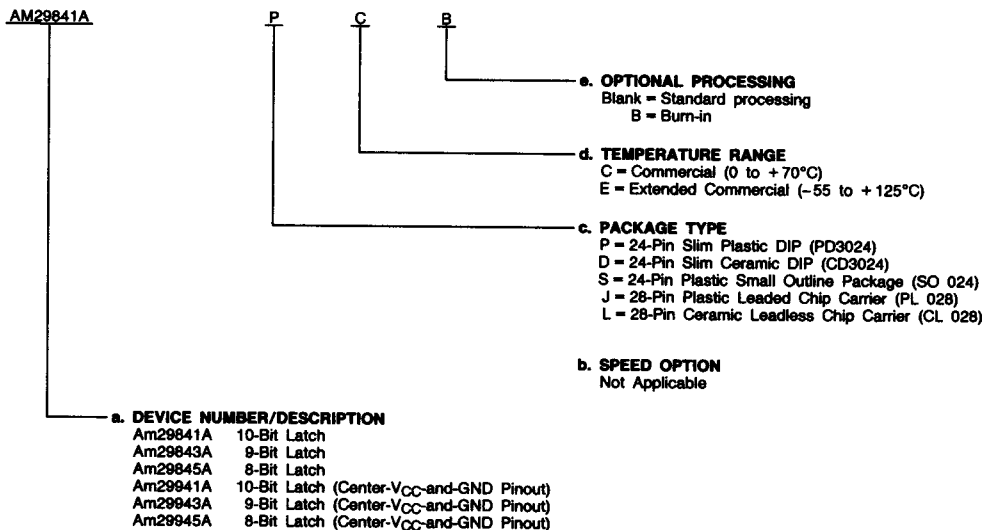
Am29841A/Am29843A/Am29845A
Am29941A/Am29943A/Am29945A

ORDERING INFORMATION

Standard Products

AMD products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

- a. Device Number
- b. Speed Option (if applicable)
- c. Package Type
- d. Temperature Range
- e. Optional Processing



Valid Combinations	
AM29841A	PC, PCB, DC, DCB, DE, SC, JC, LC
AM29843A	
AM29845A	
AM29941A	PC, PCB, DC, DCB, DE
AM29943A	
AM29945A	

Valid Combinations

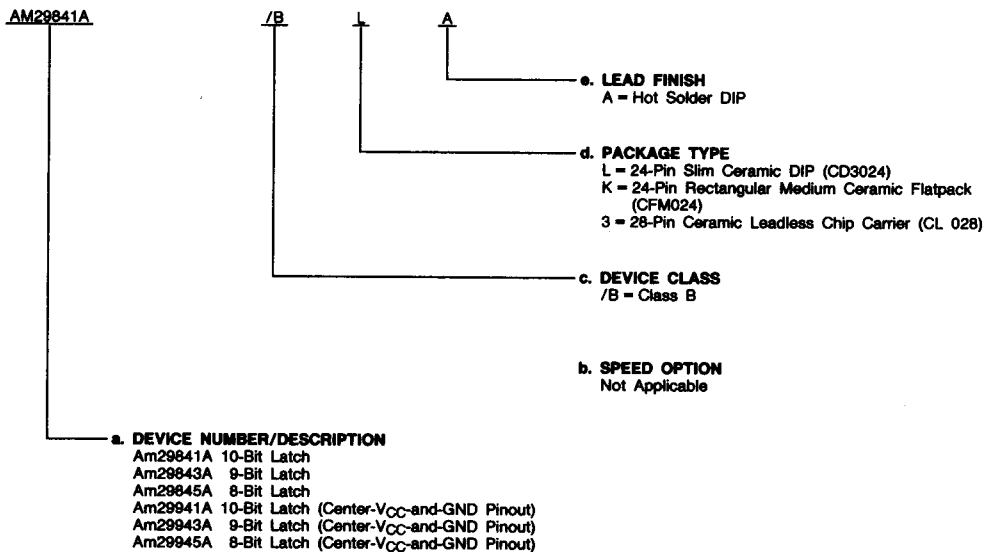
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released valid combinations, and to obtain additional data on AMD's standard military grade products.

ORDERING INFORMATION (Cont'd.)

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of:

- a. Device Number
- b. Speed Option (if applicable)
- c. Device Class
- d. Package Type
- e. Lead Finish



Valid Combinations	
AM29841A	/BLA, /BKA, /B3A
AM29843A	
AM29845A	
AM29841A	/BLA
AM29843A	
AM29845A	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

Group A Tests

Group A tests consist of Subgroups
1, 2, 3, 7, 8, 9, 10, 11.

Am29841A/Am29843A/Am29845A
Am29941A/Am29943A/Am29945A

PIN DESCRIPTION

D_i Data Inputs (Input)

D_i are the latch data inputs.

Y_i Data Outputs (Output)

Y_i are the three-state data outputs.

LE Latch Enable (Input, Active HIGH)

The latches are transparent when LE is HIGH. Input data is latched on a HIGH-to-LOW transition.

Am29841A

OE Output Enable (Input, Active LOW)

When OE is LOW, the latch data is passed to the Y_i outputs.
When OE is HIGH, the Y_i outputs are in the high-impedance state.

Am29843A

OE Output Enable (Input, Active LOW)

When OE is LOW, the latch data is passed to the Y_i outputs.
When OE is HIGH, the Y_i outputs are in the high-impedance state.

PRE Preset (Input, Active LOW)

When PRE is LOW, the outputs are HIGH if OE is LOW. PRE overrides the CLR pin. PRE will set the latch independent of the state of OE.

CLR Clear (Input, Active LOW)

When CLR is LOW, the internal latch is cleared. When CLR is LOW, the outputs are LOW if OE is LOW and PRE is HIGH. When CLR is HIGH, data can be entered into the latch.

Am29845A

OE_i Output Enables (Input, Active LOW)

When OE₁, OE₂, and OE₃ are all LOW, the latch data is passed to the Y_i outputs. If any or all OE_i are HIGH, the Y_i outputs are put in a high impedance state.

PRE Preset (Input, Active LOW)

When PRE is LOW, the outputs are HIGH if all OE_i are LOW. PRE overrides the CLR pin. PRE will set the latch independent of the state of OE.

CLR Clear (Input, Active LOW)

When CLR is LOW, the internal latch is cleared. When CLR is LOW, the Y_i outputs are LOW if all OE_i are LOW and PRE is HIGH. When CLR is HIGH, data can be entered into the latch.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	-65 to +150°C
Ambient Temperature with	
Power Applied	-55 to +125°C
Supply Voltage to Ground Potential	
Continuous	-0.5 V to +7.0 V
DC Voltage Applied to Outputs	
for High Output State	-0.5 V to +5.5 V
DC Input Voltage	-1.5 V to +6.0 V
DC Output Current, into Outputs	100 mA
DC Input Current	-30 mA to +5.0 mA

Stresses above those listed under **ABSOLUTE MAXIMUM RATINGS** may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices	
Temperature (T _A)	0 to +70°C
Supply Voltage (V _{CC})	+4.5 V to +5.5 V
Military (M) and Extended Commercial (E) Devices	
Temperature (T _C)	-55 to +125°C
Supply Voltage (V _{CC})	+4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified (for APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Units
V _{OH}	Output HIGH Voltage	V _{CC} = 4.5 V V _{IN} = V _{IH} or V _{IL}	I _{OH} = -15 mA	2.4		Volts
			I _{OH} = -24 mA	2.0		
V _{OL}	Output LOW Voltage	V _{CC} = 4.5 V V _{IN} = V _{IH} or V _{IL}	MIL, I _{OL} = 32 mA		0.5	Volts
			COM'L, I _{OL} = 48 mA		0.5	
V _{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for All Inputs (Note 1)		2.0		Volts
V _{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for All Inputs (Note 1)			0.8	Volts
V _I	Input Clamp Voltage	V _{CC} = 5.5 V, I _{IN} = -18 mA			-1.2	Volts
I _{IL}	Input LOW Current	V _{CC} = 5.5 V, V _{IN} = 0.4 V			-0.5	mA
I _{IH}	Input HIGH Current	V _{CC} = 5.5 V, V _{IN} = 2.7 V			50	μA
I _I	Input HIGH Current	V _{CC} = 5.5 V, V _{IN} = 5.5 V			100	μA
I _{OZL}	Output Off-State Current (High Impedance)	V _{CC} = 5.5 V	V _O = 0.4 V		-50	μA
I _{OZH}			V _O = 2.7 V		50	
I _{SC}	Output Short-Circuit Current	V _{CC} = 5.5 V, V _{OUT} = 0 V (Note 2)		-75	-250	mA
I _{OFF}	Bus Leakage Current	V _{CC} = 0 V, V _{OUT} = 2.9 V			100	μA
I _{CC}	Supply Current	V _{CC} = 5.5 V Outputs Unloaded	Outputs LOW		97	mA
			Outputs HIGH		70	
			Outputs Hi-Z		81	

Notes: 1. Input thresholds are tested during DC parameter testing, and may be tested in combination with other DC parameters.
2. Not more than one output shorted at a time. Duration of the short-circuit test should not exceed one second.

SWITCHING CHARACTERISTICS over operating range unless otherwise specified (for APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted)

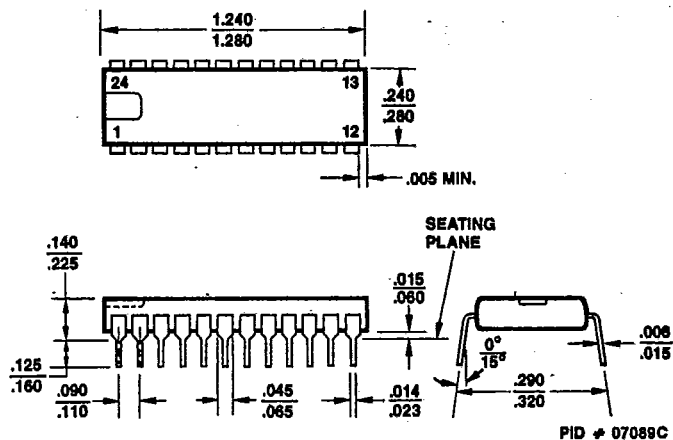
Parameter Symbol	Parameter Description		Test Conditions*	COMMERCIAL		MILITARY		Units
				Min.	Max.	Min.	Max.	
t _{PLH}	Data (D _i) to Output Y _i (LE = HIGH)		C _L = 50 pF R ₁ = 500 Ω R ₂ = 500 Ω		7		8.5	ns
t _{PHL}					9		10	ns
t _S	Data to LE Setup Time	2.5			3.5		ns	
t _H	Data to LE Hold Time	2.5			3.5		ns	
t _{PLH}	Latch Enable (LE) to Y _i				12		13	ns
t _{PHL}					12		13	ns
t _{PLH}	Propagation Delay, Preset to Y _i				12		14	ns
t _{PHL}					12		14	ns
t _{REC}	Preset (PRE ) to LE Setup Time	4			5		ns	
t _{PLH}	Propagation Delay, Clear to Y _i				13		14	ns
t _{PHL}					13		14	ns
t _{REC}	Clear (CLR ) to LE Setup Time			7		8		ns
t _{PWH}	LE Pulse Width	HIGH	4		5		ns	
t _{PWL}	Preset Pulse Width	LOW	5		7		ns	
t _{PWL}	Clear Pulse Width	LOW	4		5		ns	
t _{ZH}	Output Enable Time  to Y _i			10.5		13.5	ns	
t _{ZL}				11.5		14.5	ns	
t _{HZ}	Output Disable Time  to Y _i			8		10	ns	
t _{LZ}				8		10	ns	

*See Test Circuit and Waveforms.

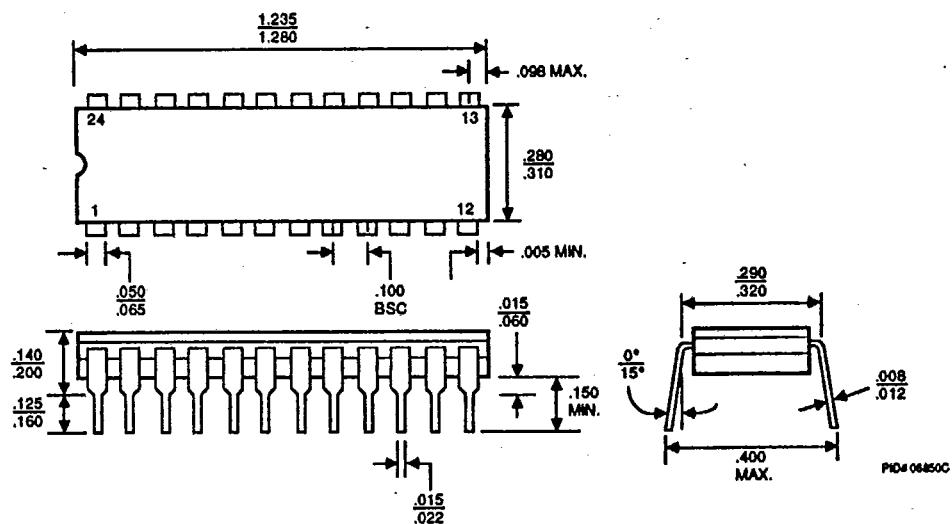
PACKAGE OUTLINES*

T-90-20

PD3024



CD3024

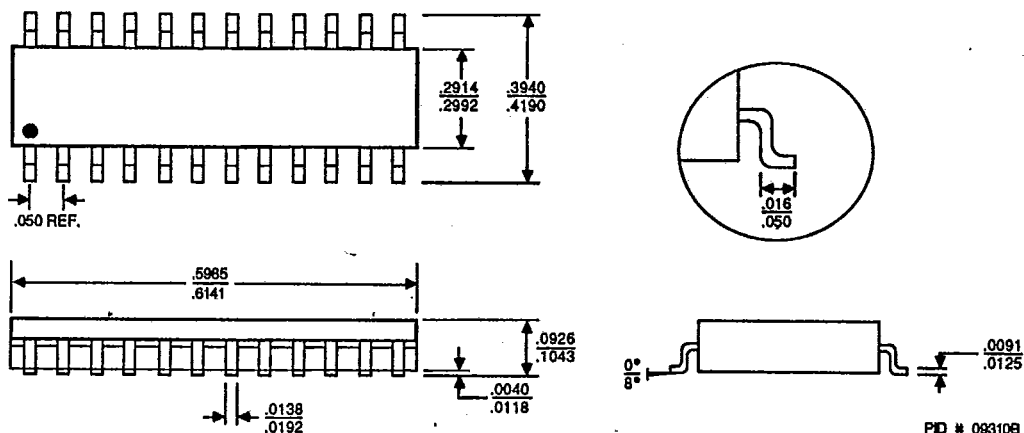


*For reference only.

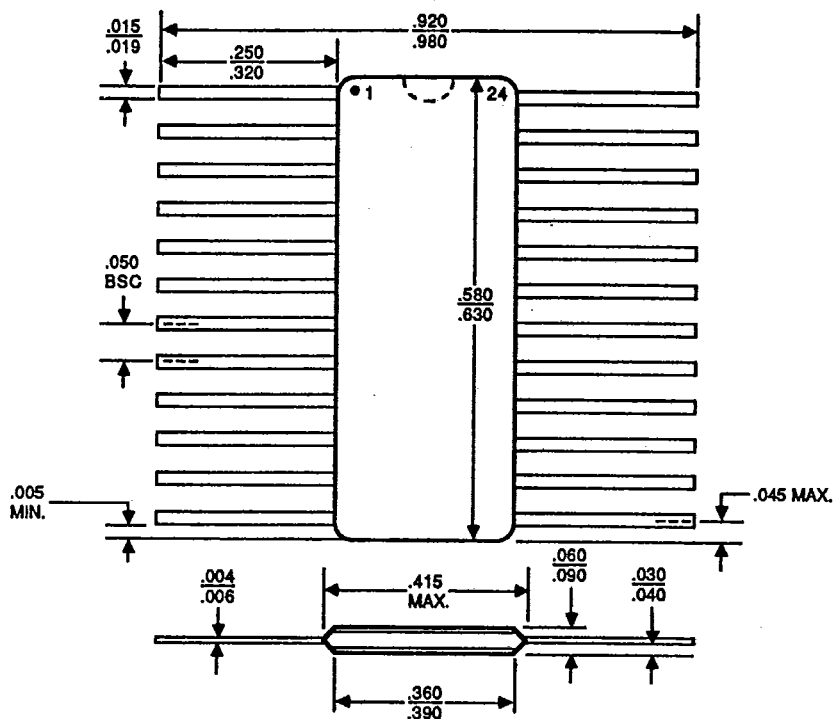
PACKAGE OUTLINES (Cont'd.)

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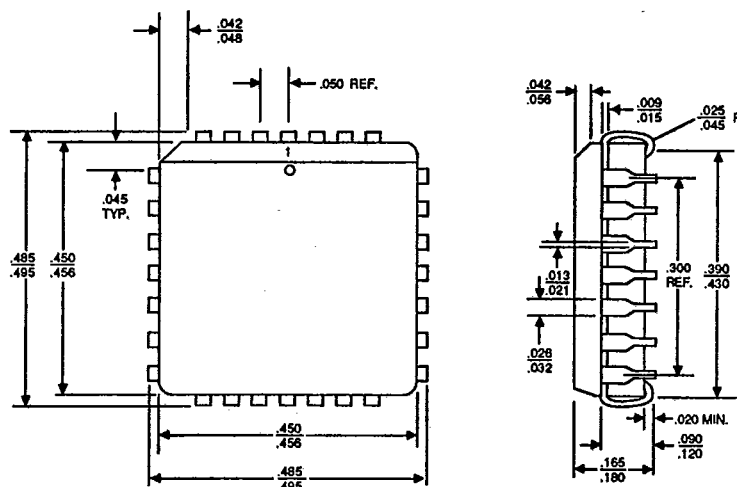
SO 024



CFM024

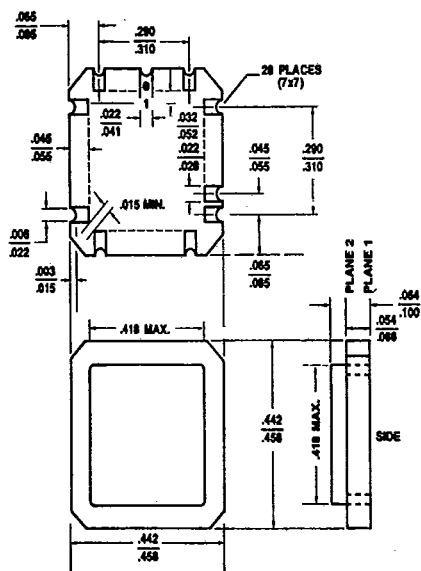


T-90-20

PL 028

PID # 06751E

CL 028



PID # 06595D

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