Am29833A/Am29853A

Parity Bus Transceivers

DISTINCTIVE CHARACTERISTICS

- High-speed bidirectional bus transceivers for processor organized devices
  - T-R delay = 6 ns typical
  - R_i-Parity delay = 9 ns typical
- Error flag with open-collector output
- Generates odd parity for all-zero protection

- 200 mV minimum input hysteresis (Commercial) on input data ports
- High drive capability:
  - 48 mA Commercial I_{OL}
- Higher speed, lower power versions of the Am29833 & Am29853

GENERAL DESCRIPTION

The Am29833A and Am29853A are high-performance parity bus transceivers designed for two-way communications. Each device can be used as an 8-bit transceiver, as well as a 9-bit parity checker/generator. In the transmit mode, data is read at the R port and output at the T port with a parity bit. In the receive mode, data and parity are read at the T port, and the data is output at the R port along with an $\overline{ERR}$ flag showing the result of the parity test.

In the Am29833A, the error flag is clocked and stored in a register which is read at the open-collector $\overline{ERR}$ output. The $\overline{CLR}$ input is used to clear the error flag register. In the Am29853A, a latch replaces this register, and the $\overline{EN}$ and $\overline{CLR}$ controls are used to pass, store, sample or clear the error flag output. When both output enables

are disabled in the Am29853A and Am29833A, the parity logic defaults to the transmit mode, so that the $\overline{ERR}$ pin reflects the parity of the R port.

The output enables, $\overline{OER}$ and $\overline{OET}$, are used to force the port outputs to the high-impedance state so that other devices can drive bus lines directly. In addition, the user can force a parity error by enabling both $\overline{OER}$ and $\overline{OET}$ simultaneously. This transmission of inverted parity gives the designer more system diagnostic capability.

Each of these devices is produced with AMD's proprietary IMOX™ bipolar process, and features typical propagation delays of 6 ns, as well as high-capacitive drive capability.
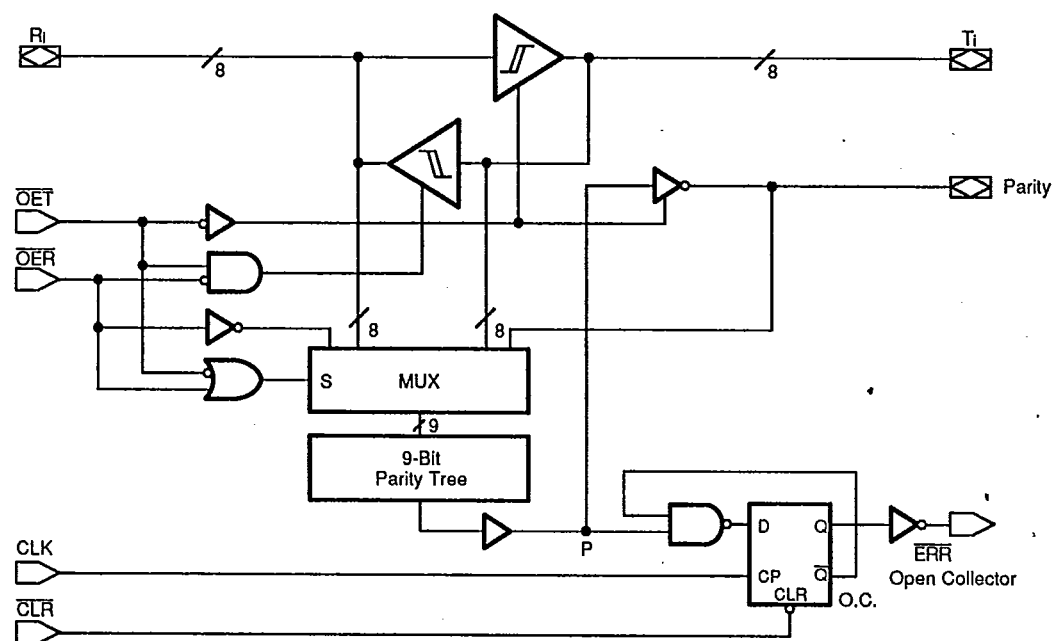
SIMPLIFIED BLOCK DIAGRAM
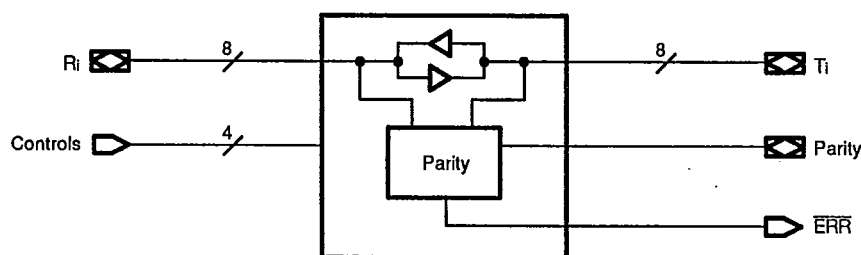
07140-001A

BLOCK DIAGRAMS
Am29833A

07140-002A

Am29853A
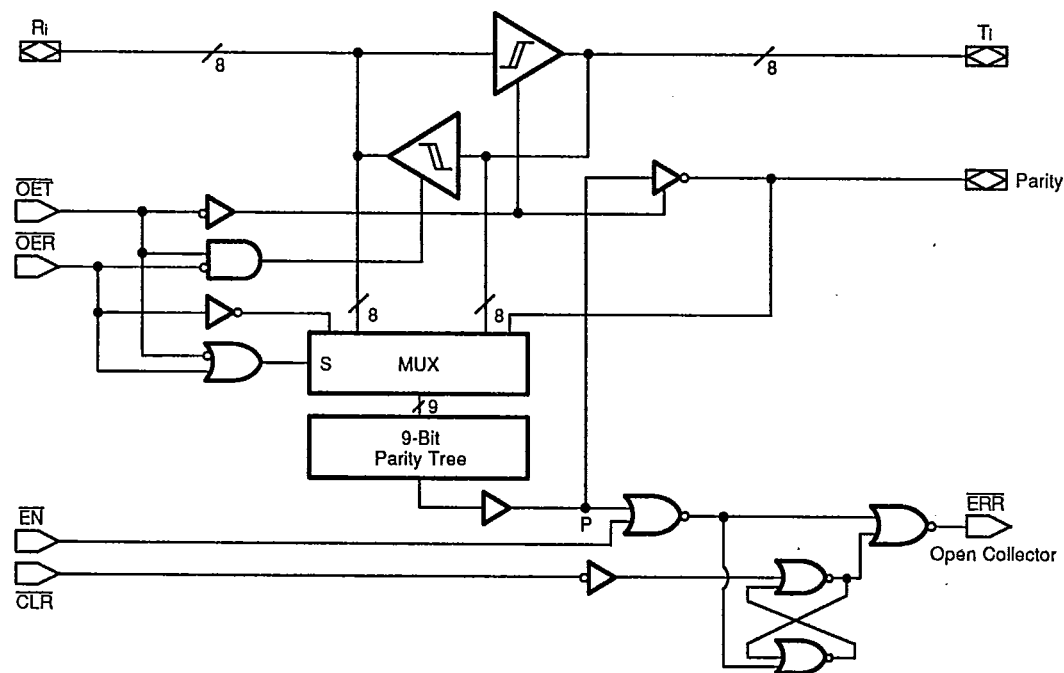
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Am29833A/Am29853A

CONNECTION DIAGRAMS
(Top View)

T-52-31

Am29833A

DIP

```
        ┌───∪───┐
 OER ⊏ 1 •   24 ⊐ Vcc
  R0 ⊏ 2      23 ⊐ T0
  R1 ⊏ 3      22 ⊐ T1
  R2 ⊏ 4      21 ⊐ T2
  R3 ⊏ 5      20 ⊐ T3
  R4 ⊏ 6      19 ⊐ T4
  R5 ⊏ 7      18 ⊐ T5
  R6 ⊏ 8      17 ⊐ T6
  R7 ⊏ 9      16 ⊐ T7
 ERR ⊏ 10     15 ⊐ Parity
 CLR ⊏ 11     14 ⊐ OET
 GND ⊏ 12     13 ⊐ CLK
        └───────┘
```

07140-004A

Am29853A

DIP

```
        ┌───∪───┐
 OER ⊏ 1 •   24 ⊐ Vcc
  R0 ⊏ 2      23 ⊐ T0
  R1 ⊏ 3      22 ⊐ T1
  R2 ⊏ 4      21 ⊐ T2
  R3 ⊏ 5      20 ⊐ T3
  R4 ⊏ 6      19 ⊐ T4
  R5 ⊏ 7      18 ⊐ T5
  R6 ⊏ 8      17 ⊐ T6
  R7 ⊏ 9      16 ⊐ T7
 ERR ⊏ 10     15 ⊐ Parity
 CLR ⊏ 11     14 ⊐ OET
 GND ⊏ 12     13 ⊐ EN
        └───────┘
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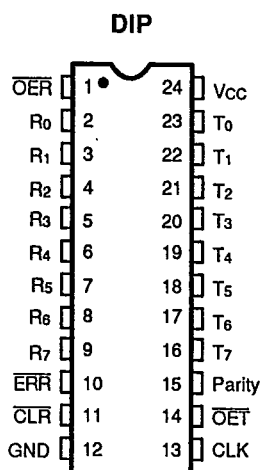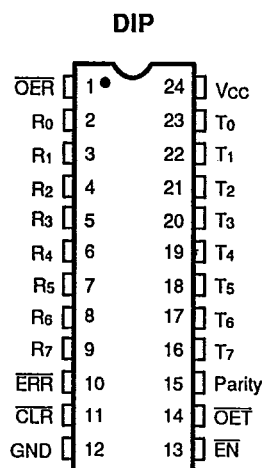
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FUNCTION TABLE   T-52-31
Am29833A (Register Option)

$\overline{OET}$	$\overline{OER}$	$\overline{CLR}$	CLK	R_i	Sum of H's of R_i	T_i	Sum of H's (T_i + Parity)	R_i	T_i	Parity	$\overline{ERR}$	Function
L	H	X	X	H	ODD	NA	NA	NA	H	L	NA	Transmit mode:
L	H	X	X	H	EVEN	NA	NA	NA	H	H	NA	transmits data from
L	H	X	X	L	ODD	NA	NA	NA	L	L	NA	R port to T port,
L	H	X	X	L	EVEN	NA	NA	NA	L	H	NA	generating parity. Receive path is disabled.
H	L	H	↑	NA	NA	H	ODD	H	NA	NA	H	Receive mode:
H	L	H	↑	NA	NA	H	EVEN	H	NA	NA	L	transmits data from
H	L	H	↑	NA	NA	L	ODD	L	NA	NA	H	T port to R port with
H	L	H	↑	NA	NA	L	EVEN	L	NA	NA	L	parity test resulting in error flag. Transmit path is disabled.
X	X	L	X	X	X	X	X	X	X	X	H	Clear error flag register.
H	H	H	X	X	X	X	X	Z	Z	Z	*	Both transmitting and
H	H	L	X	X	X	X	X	Z	Z	Z	H	receiving paths are disabled.
H	H	H	↑	L	ODD	X	X	Z	Z	Z	H	Parity logic
H	H	H	↑	H	EVEN	X	X	Z	Z	Z	L	defaults to transmit
L	L	X	X	H	ODD	NA	NA	NA	H	H	NA	mode. Forced-error
L	L	X	X	H	EVEN	NA	NA	NA	H	L	NA	checking.
L	L	X	X	L	ODD	NA	NA	NA	L	H	NA	
L	L	X	X	L	EVEN	NA	NA	NA	L	L	NA	

H = HIGH   Z = High Impedance   ODD = Odd Number
L = LOW   NA= Not Applicable   EVEN= Even Number
↑ = LOW-to-HIGH Transition   * = Store the State of the Last   i = 0, 1, 2, 3, 4, 5, 6, 7
X = Don't Care   Receive Cycle

FUNCTION TABLE
Am29853A (Latch Option)

T-52-31

OET	OER	CLR	EN	Ri	Sum of H's of Rl	Ti	Sum of H's (Ti + Parity)	Ri	Ti	Parity	ERR	Function
L	H	X	X	H	ODD	NA	NA	NA	H	L	NA	Transmit mode: transmits data from R port to T port, generating parity. Receive path is disabled.
L	H	X	X	H	EVEN	NA	NA	NA	H	H	NA	
L	H	X	X	L	ODD	NA	NA	NA	L	L	NA	
L	H	X	X	L	EVEN	NA	NA	NA	L	H	NA	
H	L	L	L	NA	NA	H	ODD	H	NA	NA	H	Receive mode: transmits data from T port to R port with parity test resulting in error flag. Transmit path is disabled.
H	L	L	L	NA	NA	H	EVEN	H	NA	NA	L	
H	L	L	L	NA	NA	L	ODD	L	NA	NA	H	
H	L	L	L	NA	NA	L	EVEN	L	NA	NA	L	
H	L	H	L	NA	NA	H	ODD	H	NA	NA	H	Receive mode: transmits data from T port to R port, passes parity test resulting in error flag. Transmit path is disabled.
H	L	H	L	NA	NA	H	EVEN	H	NA	NA	L	
H	L	H	L	NA	NA	L	ODD	L	NA	NA	H	
H	L	H	L	NA	NA	L	EVEN	L	NA	NA	L	
H	L	H	H	NA	NA	X	X	X	NA	NA	*	Store the state of error flag latch.
X	X	L	H	X	X	X	X	X	NA	NA	H	Clear error flag latch.
H	H	H	H	X	X	X	X	Z	Z	Z	*	Both transmitting and receiving paths are disabled. Parity logic defaults to transmit mode.
H	H	L	H	X	X	X	X	Z	Z	Z	H	
H	H	X	L	L	ODD	X	X	Z	Z	Z	H	
H	H	X	L	H	EVEN	X	X	Z	Z	Z	L	
L	L	X	X	H	ODD	NA	NA	NA	H	H	NA	Forced-error checking.
L	L	X	X	H	EVEN	NA	NA	NA	H	L	NA	
L	L	X	X	L	ODD	NA	NA	NA	L	H	NA	
L	L	X	X	L	EVEN	NA	NA	NA	L	L	NA	

H = HIGH
L = LOW
↑ = LOW-to-HIGH Transition
X = Don't Care

Z = High Impedance
NA = Not Applicable
* = Store the State of the Last Receive Cycle

ODD = Odd Number
EVEN = Even Number
i = 0, 1, 2, 3, 4, 5, 6, 7

TRUTH TABLES
Error Flag Output

Am29833A

Inputs		Internal to Device	Outputs Pre-state	Output	
CLR	CLK	Point "P"	$\overline{ERR}_{n-1}$	$\overline{ERR}$	Function
H	↑	H	H	H	
H	↑	X	L	L	Sample (1's Capture)
H	↑	L	X	L	
L	X	X	X	H	Clear

Note:
$\overline{OET}$ is HIGH and $\overline{OER}$ is LOW.

Am29853A

Inputs		Internal to Device	Outputs Pre-state	Output	
$\overline{EN}$	$\overline{CLR}$	Point "P"	$\overline{ERR}_{n-1}$	$\overline{ERR}$	Function
L	L	L	X	L	Pass
L	L	H	X	H	
L	H	L	X	L	
L	H	X	L	L	Sample (1's Capture)
L	H	H	H	H	
H	L	X	X	H	Clear
H	H	X	L	L	Store
H	H	X	H	H	

Note:
$\overline{OET}$ is HIGH and $\overline{OER}$ is LOW.

ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option (If applicable)
c. Package Type
d. Temperature Range
e. Optional Processing

AM29833A
AM29853A

P C

e. OPTIONAL PROCESSING
Blank = Standard processing

d. TEMPERATURE RANGE
C = Commercial (0 to +70°C)

c. PACKAGE TYPE
P = 24-Pin (300-mil) Plastic DIP (PD3024)

b. SPEED OPTION
Not Applicable

a. DEVICE NUMBER/DESCRIPTION
Am29833A
Parity Transceiver, Register Option

Am29853A
Parity Transceiver, Latch Option

Valid Combinations	
AM29833A	PC
AM29853A	

Valid Combinations
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

PIN DESCRIPTION
Am29833A/Am29853A

$\overline{\text{OER}}$
Output Enable Receive (Input, Active LOW)

When LOW in conjunction with $\overline{\text{OET}}$ HIGH, the devices are in the Receive mode (R_i are outputs, T_i and Parity are inputs).

$\overline{\text{OET}}$
Output Enable Transmit (Input, Active LOW)

When LOW in conjunction with $\overline{\text{OER}}$ HIGH, the devices are in the Transmit mode (R_i are inputs, T_i and Parity are outputs).

R_i
Receive Port (Input/Output, Three-State)

R_i are the 8-bit data inputs in the Transmit mode, and the outputs in the Receive mode.

T_i
Transmit Port (Input/Output, Three-State)

T_i are the 8-bit data outputs in the Transmit mode, and the inputs in the Receive mode.

Parity
Parity Flag (Input/Output, Three-State)

In the Transmit mode, the Parity signal is an active output used to generate odd parity. In the Receive mode, the T_i and Parity inputs are combined and checked for odd parity. When both output enables are HIGH, the Parity Flag is in the high impedance state. When both output enables are LOW, the Parity bit forces a parity error.

Am29833A Only

$\overline{\text{ERR}}$
Error Flag (Output, Open Collector)

In the Receive mode, the parity of the T_i bits is calculated and compared to the Parity input. $\overline{\text{ERR}}$ goes LOW when the comparison indicates a parity error. $\overline{\text{ERR}}$ stays LOW until the register is cleared.

$\overline{\text{CLR}}$
Clear (Input, Active LOW)

When $\overline{\text{CLR}}$ goes LOW, the Error Flag Register is cleared ($\overline{\text{ERR}}$ goes HIGH).

CLK
Clock (Input, Positive Edge-Triggered)

This pin is the clock input for the Error Flag register.

Am29853A Only

$\overline{\text{ERR}}$
Error Flag (Output, Open Collector)

In the Receive mode, the parity of the T_i bits is calculated and compared to the Parity input. $\overline{\text{ERR}}$ goes LOW when the comparison indicates a parity error. $\overline{\text{ERR}}$ stays LOW until the latch is cleared.

$\overline{\text{CLR}}$
Clear (Input, Active LOW)

When $\overline{\text{CLR}}$ goes LOW, and $\overline{\text{EN}}$ is HIGH, the Error Flag latch is cleared ($\overline{\text{ERR}}$ goes HIGH).

$\overline{\text{EN}}$
Latch Enable (Input, Active LOW)

This pin is the latch enable for the Error Flag latch.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−65°C to +150°C
Ambient Temperature with Power Applied	−55 to +125°C
Supply Voltage to Ground Potential Continuous	−0.5 V to +7.0 V
DC Voltage Applied to Outputs For High Output State	−0.5 V to +5.5 V
DC Input Voltage	−1.5 V to +6.0 V
DC Output Current, Into Outputs	100 mA
DC Input Current	−30 mA to +5.0 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A)	0 to +70°C
Supply Voltage (V_{CC})	+4.5 to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions			Min.	Max.	Unit
V_{OH}	Output HIGH Voltage Except ($\overline{ERR}$)	$V_{CC} = 4.5$ V, $V_{IN} = V_{IH}$ or V_{IL}		$I_{OH} = -15$ mA	2.4		V
				$I_{OH} = -24$ mA	2.0		
V_{OL}	Output LOW Voltage	$V_{CC} = 4.5$ V, $V_{IN} = V_{IH}$ or V_{IL}	$\overline{ERR}$	$I_{OL} = 48$ mA		0.5	V
			All Other Outputs	$I_{OL} = 48$ mA		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all inputs (Note 1)			2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all inputs (Note 1)				0.8	V
V_I	Input Clamp Voltage	$V_{CC} = 4.5$ V, $I_{IN} = -18$ mA				−1.2	V
V_{HYST}	Hysteresis for Inputs R_i, T_i				200		mV
I_{ZL}	I/O Port LOW Current	$V_{CC} = 5.5$ V, $V_{IN} = 0.4$ V				−550	μA
I_{IL}	Input LOW Current	$V_{CC} = 5.5$ V, $V_{IN} = 0.4$ V				−0.5	mA
I_{IH}	Input HIGH Current	$V_{CC} = 5.5$ V, $V_{IN} = 2.7$ V				50	μA
I_I	Input HIGH Current	$V_{CC} = 5.5$ V, $V_{IN} = 5.5$ V				100	μA
I_{ZH}	I/O Port HIGH Current	$V_{CC} = 5.5$ V, $V_{IN} = 2.7$ V				100	μA
I_{ZI}	I/O Port HIGH Current	$V_{CC} = 5.5$ V, $V_{IN} = 5.5$ V				150	μA
I_{SC}	Output Short-Circuit Current	$V_{CC} = 5.5$ V, $V_O = 0$ V (Note 2)			−75	−250	mA
I_{OFF}	Bus Leakage Current	$V_{CC} = 0$ V, $V_O = 2.9$ V				100	μA
I_{CC}	Power Supply Current	$V_{CC} = 5.5$ V Outputs Loaded	Outputs LOW		·	180	mA
			Outputs HIGH			155	
			Outputs Hi-Z			170	

Notes:

1. Input thresholds are tested during DC parameter testing, and may be tested in combination with other DC parameters.

2. Not more than one output shorted at a time. Duration of the short-circuit test should not exceed one second.

SWITCHING CHARACTERISTICS over operating ranges unless otherwise specified   T–52–31

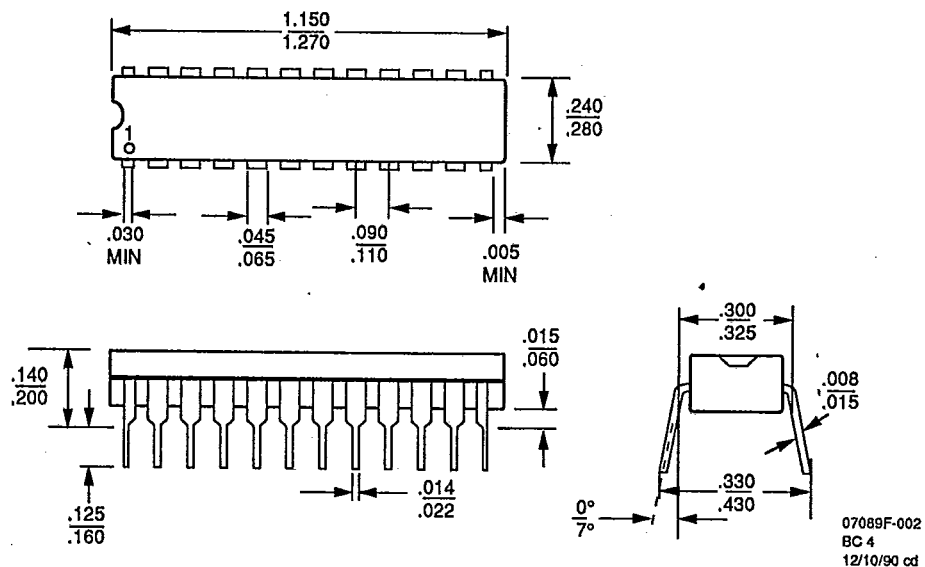| Parameter Symbol	Parameter Description		Test Conditions*	Min.	Max.	Unit
t$_{PLH}$	Propagation Delay to R$_i$ to T$_i$,				10	ns
t$_{PHL}$	T$_i$ to R$_i$				10	ns
t$_{PLH}$	Propagation Delay R$_i$ to Parity				15	ns
t$_{PHL}$					15	ns
t$_{ZH}$	Output Enable Time $\overline{OER}$, $\overline{OET}$ to R$_i$, T$_i$			12		ns
t$_{ZL}$	and Parity				12	ns
t$_{HZ}$	Output Disable Time $\overline{OER}$, $\overline{OET}$ to R$_i$, T$_i$			12		ns
t$_{LZ}$	and Parity		C$_L$ = 50 pF		12	ns
t$_S$	T$_i$, Parity to CLK Setup Time (Note 1)		R$_1$ = 500 Ω	12		ns
t$_H$	T$_i$, Parity to CLK Hold Time (Note 1)		R$_2$ = 500 Ω	.0		ns
t$_{REC}$	Clear ($\overline{CLR}$⌐) to CLK Setup Time (Note 2)			15		ns
t$_{PWH}$	Clock Pulse Width (Note 1)	HIGH		7		ns
t$_{PWL}$		LOW		7		ns
t$_{PWL}$	Clear Pulse Width	LOW		7		ns
t$_{PHL}$	Propagation Delay CLK to $\overline{ERR}$ (Note 1)				12	ns
t$_{PLH}$	Propagation Delay $\overline{CLR}$ to $\overline{ERR}$				16	ns
t$_{PLH}$	Propagation Delay T$_i$, Parity to $\overline{ERR}$				22	ns
t$_{PHL}$	(PASS Mode Only) Am29853A				18	ns
t$_{PLH}$	Propagation Delay $\overline{OER}$ to Parity				15	ns
t$_{PHL}$					15	ns

*See test circuit and waveforms (Chapter 2).

Notes:

1. For Am29853A, replace CLK with $\overline{EN}$.

2. Not applicable to Am29853A.

PD3024
24-Pin 300-mil Plastic SKINNYDIP

T-90-20

1.150
1.270

.240
.280

1

.030
MIN

.045
.065

.090
.110

.005
MIN

.015
.060

.140
.200

.125
.160

.014
.022

.300
.325

.008
.015

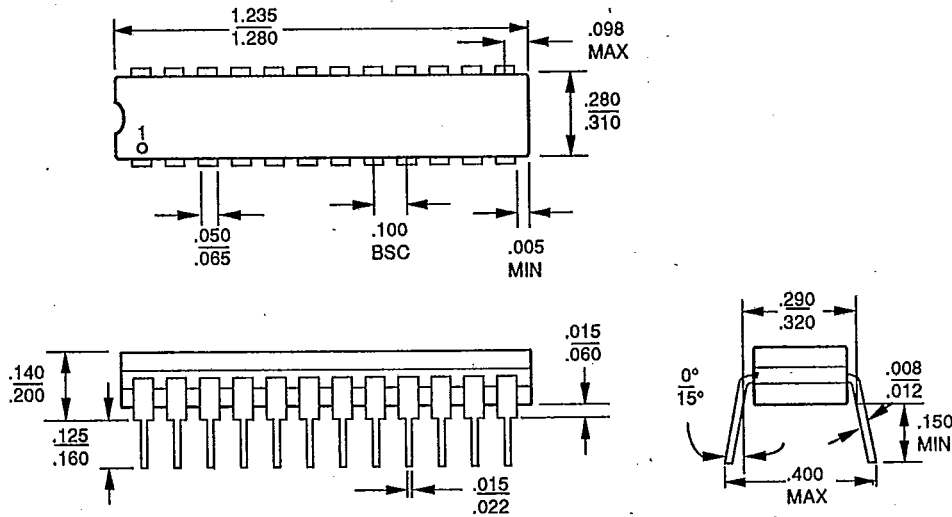.330
.430

0°
7°

07089F-002
BC 4
12/10/90 cd

Note:
For reference only. All dimensions measured in inches. BSC is an ANSI standard for Basic Space Centering.
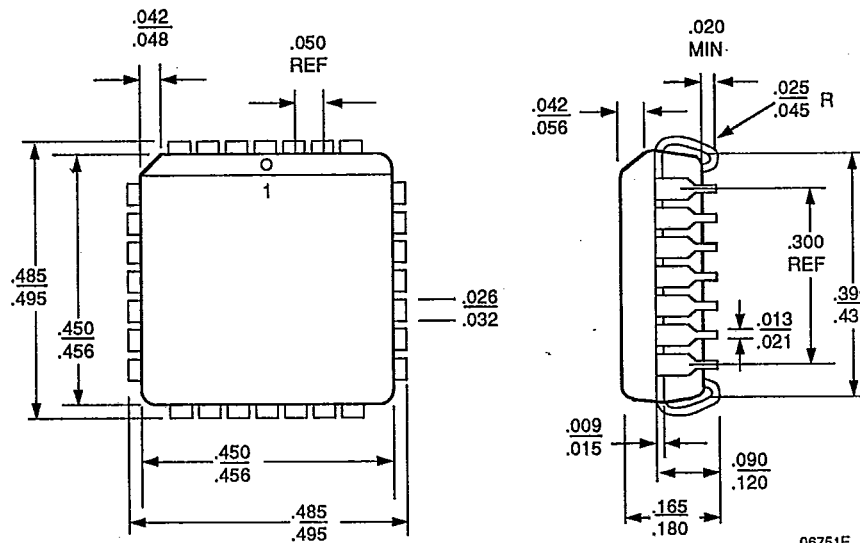
6–3

T-90-20

CD3024
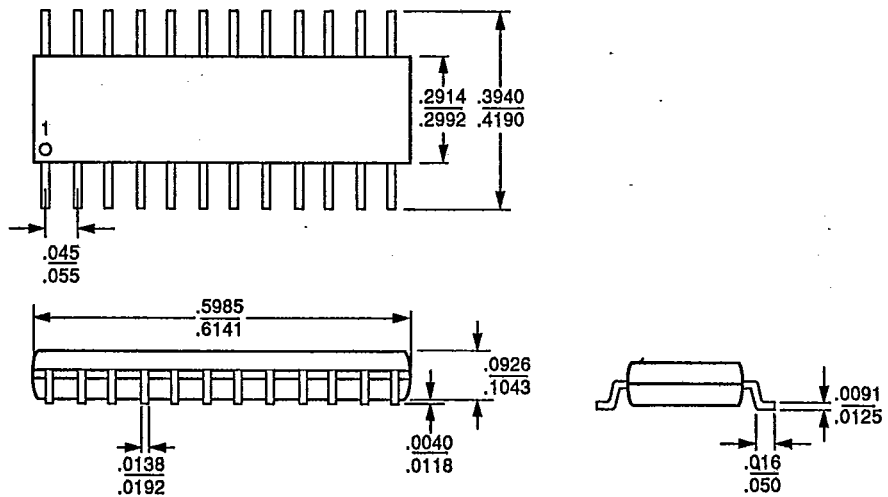## 24-Pin 300-mil Ceramic SKINNYDIP

06850C

PL 028
28-Pin Plastic Leaded Chip Carrier

06751E

SO 024
24-Pin Plastic Small Outline Package

T-90-20

.2914 .3940
.2992 .4190

.045
.055

.5985
.6141

.0926
.1043

.0040
.0118

.0138
.0192

.0091
.0125

.016
.050

09310B