NOV 2 1 1988

Am29C117

16-Bit CMOS Microprocessor

DISTINCTIVE CHARACTERISTICS

- High-Speed Microprocessor
  - Am29C117-2 supports up to 65 ns microcycle times.
- Very Low Power
- Optimized for High-Performance Controllers
  - The architecture is optimized for controllers providing an excellent solution for applications requiring bit-manipulation power.
- Flow-Through Architecture
  - Separate input and output ports avoid bus turnaround for higher throughput.
- Instruction Set is identical to the Am29C116
  - The Am29C117 has an identical architecture and instruction set with the exception of the two-port I/O structure and the additional Two-Address Immediate Instruction.
- 16-Bit Barrel Shifter
- 32 Working Registers
- 68-Lead Pin Grid Array and Plastic Leaded Chip Carrier Packages.

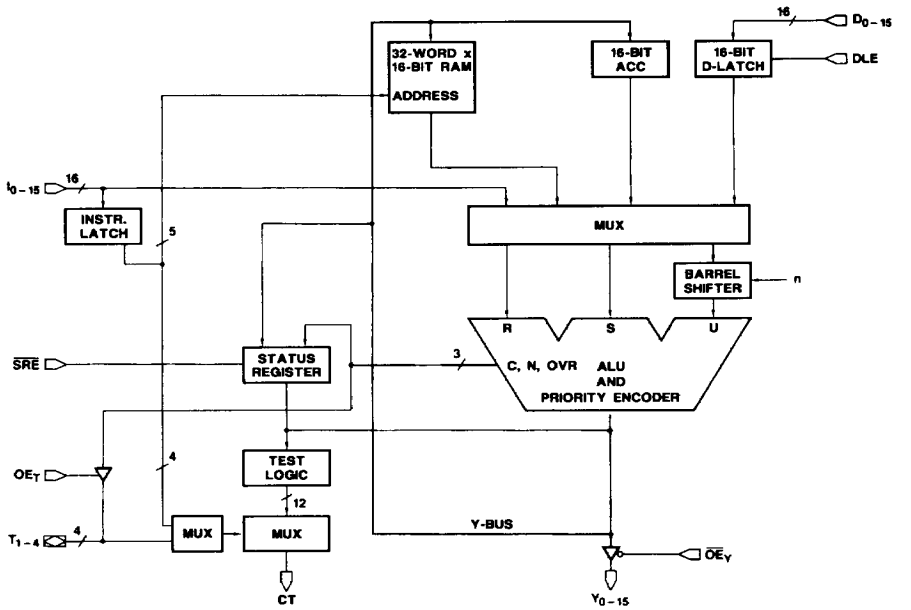
GENERAL DESCRIPTION

The Am29C117 is a microprogrammable 16-bit CMOS microprocessor whose architecture and instruction set are identical to the Am29C116's except for the I/O bus structure. Since the device has separate input and output ports, designers can avoid quick bus turnaround requirements.

The architecture and instruction set are not only optimized for high-performance peripheral controllers, but also suitable for microprogrammed processor applications when combined with the Am29C517A 16 x 16 Multiplier.

The instruction set contains unique functions besides ordinary logic and arithmetic functions: bit manipulation instructions (set, reset and test), rotate merge/compare instructions, prioritize instruction, and CRC instruction.

BLOCK DIAGRAM



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RELATED AMD PRODUCTS

Part No.	Description
Am29027	Arithmetic Accelerator
Am2910A	Microprogram Controller
Am29C10A	CMOS 12-Bit Sequencer
Am29C111	CMOS 16-Bit Microsequencer
Am29114	8-Level Real-Time Interrupt Controller
Am29116	16-Bit Bipolar Microprocessor
Am29C116/-1/-2	16-Bit CMOS Microprocessors
Am29117	2-Port 16-Bit Microprocessor
Am29118	8-Bit Am29C116 I/O Support
Am29130	16-Bit Barrel Shifter
Am2914	Vectored Priority Interrupt Controller
Am29PL141	64 x 32 Field-Programmable Controller
Am29CPL141	CMOS 64 Word Field-Programmable Controller
Am29LPL141	Low-Power Version of Am29PL141
Am29PL142	128 x 32 Field-Programmable Controller
Am29C323	CMOS 32-Bit Parallel Multiplier
Am29325	32-Bit Floating-Point Processor
Am29C325	CMOS 32-Bit Floating-Point Processor
Am29C327	CMOS Double-Precision Floating-Point Processor
Am29331	16-Bit Microprogram Sequencer
Am29C331	CMOS 16-Bit Microsequencer
Am29334	Four-Port Dual-Acccess Register File
Am29C334	CMOS Four-Port Dual-Access Register File
Am29337	16-Bit Bounds Checker
Am29C516A	CMOS 16 x 16 Multiplier
Am29C517A	CMOS 2-Port 16 x 16 Multiplier
Am29540	Programmable FFT Address Sequencer

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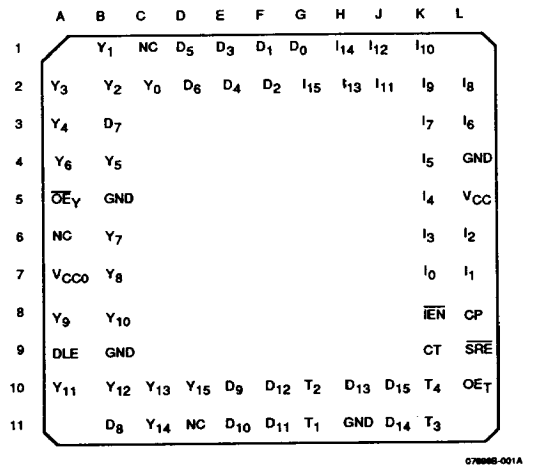
CONNECTION DIAGRAMS

PGA
(Pins Facing Up)



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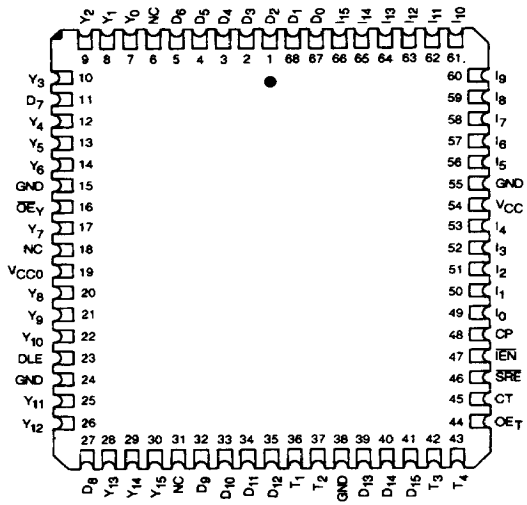
LCC*
Top View



CD009862

*Also available in a 68-pin PLCC; pinout identical to LCC.
V_{CC} are power connections for the logic.
V_{CC0} are power connections for the output drivers.

Note: Pin 1 is marked for orientation.

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PGA PIN DESIGNATIONS

(Sorted by Pin Number)

PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME
A-2	Y_3	**B-9**	GND	**F-10**	D_{12}	**K-4**	I_5
A-3	Y_4	**B-10**	Y_{12}	**F-11**	D_{11}	**K-5**	I_4
A-4	Y_6	**B-11**	D_8	**G-1**	D_0	**K-6**	I_3
A-5	OE_Y	**C-1**	NC	**G-2**	I_{15}	**K-7**	I_0
A-6	NC	**C-2**	Y_0	**G-10**	T_2	**K-8**	$\overline{IEN}$
A-7	V_{CC0}	**C-10**	Y_{13}	**G-11**	T_1	**K-9**	CT
A-8	Y_9	**C-11**	Y_{14}	**H-1**	I_{14}	**K-10**	T_4
A-9	DLE	**D-1**	D_5	**H-2**	I_{13}	**K-11**	T_3
A-10	Y_{11}	**D-2**	D_6	**H-10**	D_{13}	**L-2**	I_8
B-1	Y_1	**D-10**	Y_{15}	**H-11**	GND	**L-3**	I_6
B-2	Y_2	**D-11**	NC	**J-1**	I_{12}	**L-4**	GND
B-3	D_7	**E-1**	D_3	**J-2**	I_{11}	**L-5**	V_{CC}
B-4	Y_5	**E-2**	D_4	**J-10**	D_{15}	**L-6**	I_2
B-5	GND	**E-10**	D_9	**J-11**	D_{14}	**L-7**	I_1
B-6	Y_7	**E-11**	D_{10}	**K-1**	I_{10}	**L-8**	CP
B-7	Y_8	**F-1**	D_1	**K-2**	I_9	**L-9**	$\overline{SRE}$
B-8	Y_{10}	**F-2**	D_2	**K-3**	I_7	**L-10**	OE_T

(Sorted by Pin Name)

PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME
L-8	**CP**	J-10	**D_{15}**	J-2	**I_{11}**	A-7	**V_{CC0}**
K-9	**CT**	A-9	**DLE**	J-1	**I_{12}**	C-2	**Y_0**
G-1	**D_0**	B-5	**GND**	H-2	**I_{13}**	B-1	**Y_1**
F-1	**D_1**	L-4	**GND**	H-1	**I_{14}**	B-2	**Y_2**
F-2	**D_2**	B-9	**GND**	G-2	**I_{15}**	A-2	**Y_3**
E-1	**D_3**	H-11	**GND**	K-8	**$\overline{IEN}$**	A-3	**Y_4**
E-2	**D_4**	K-7	**I_0**	C-1	**NC**	B-4	**Y_5**
D-1	**D_5**	L-7	**I_1**	D-11	**NC**	A-4	**Y_6**
D-2	**D_6**	L-6	**I_2**	A-6	**NC**	B-6	**Y_7**
B-3	**D_7**	K-6	**I_3**	L-10	**OE_T**	B-7	**Y_8**
B-11	**D_8**	K-5	**I_4**	A-5	**OE_Y**	A-8	**Y_9**
E-10	**D_9**	K-4	**I_5**	L-9	**$\overline{SRE}$**	B-8	**Y_{10}**
E-11	**D_{10}**	L-3	**I_6**	G-11	**T_1**	A-10	**Y_{11}**
F-11	**D_{11}**	K-3	**I_7**	G-10	**T_2**	B-10	**Y_{12}**
F-10	**D_{12}**	L-2	**I_8**	K-11	**T_3**	C-10	**Y_{13}**
H-10	**D_{13}**	K-2	**I_9**	K-10	**T_4**	C-11	**Y_{14}**
J-11	**D_{14}**	K-1	**I_{10}**	L-5	**V_{CC}**	D-10	**Y_{15}**

V_{CC} are power connections for the logic.
V_{CC0} are power connections for the output drivers.

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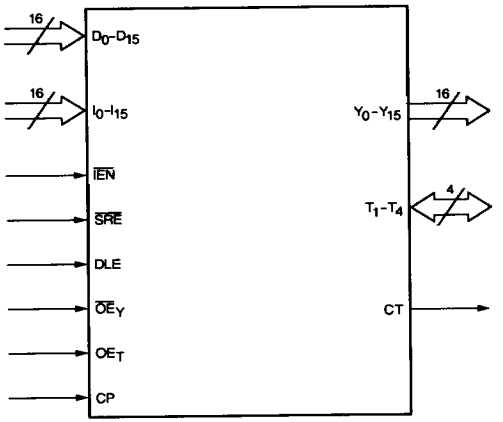
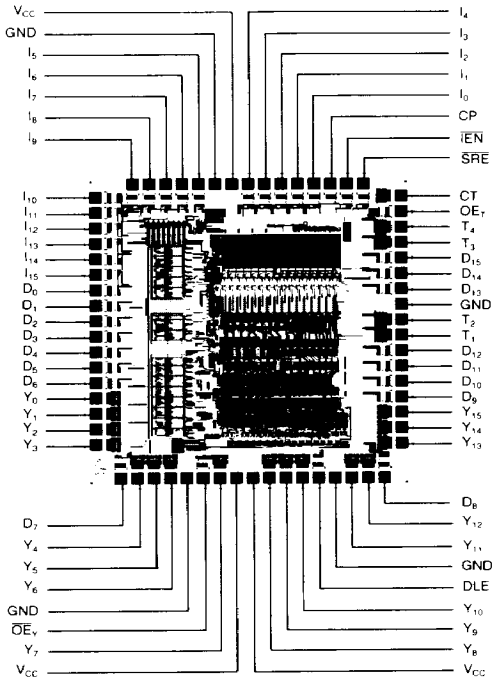
LOGIC SYMBOL



LS002610

METALLIZATION AND PAD LAYOUT



Die Size: 0.184" x 0.184"
Component Count: 14,000

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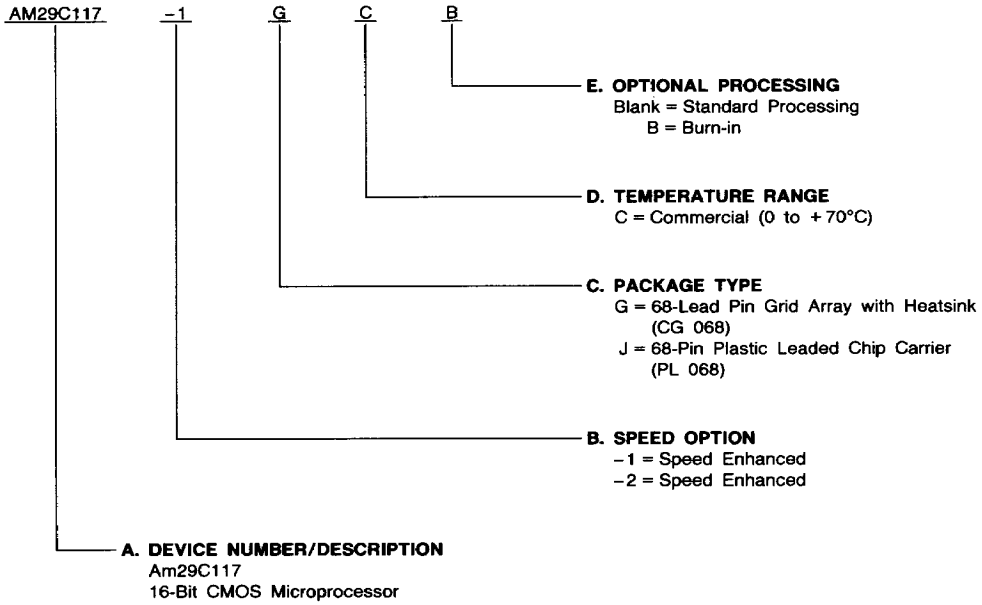
ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Package Type
D. Temperature Range
E. Optional Processing



Valid Combinations	
AM29C117	GC, GCB, JC
AM29C117-1	
AM29C117-2	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

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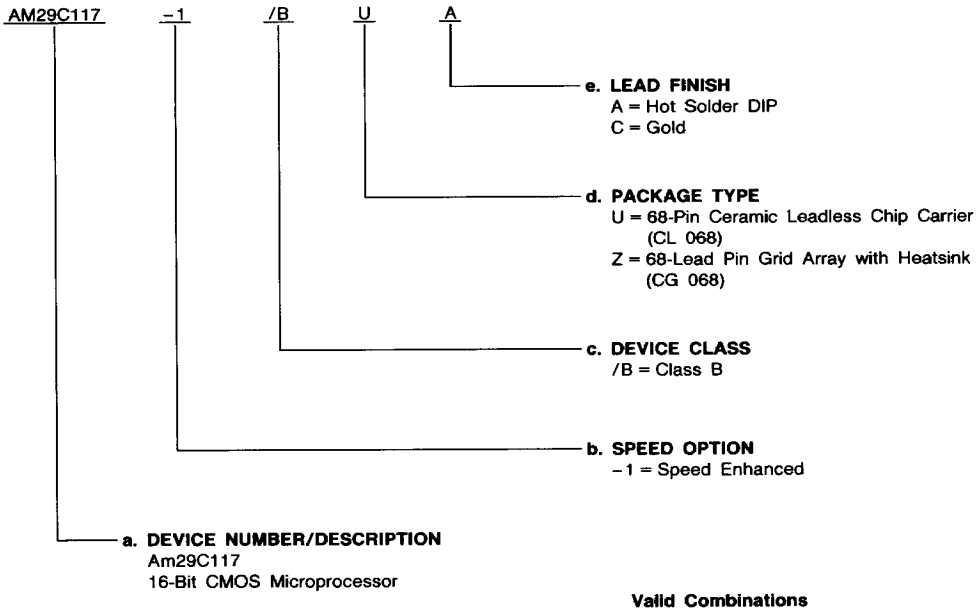
MILITARY ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) is formed by a combination of: **a. Device Number**
b. Speed Option (if applicable)
c. Device Class
d. Package Type
e. Lead Finish



Valid Combinations	
AM29C117-1	/BUA, /BZC

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

Group A Tests

Group A tests consist of Subgroups
1, 2, 3, 7, 8, 9, 10, 11.

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PIN DESCRIPTION

$D_0 - D_{15}$ Data Input Lines (Input)
$D_0 - D_{15}$ are used as external data inputs which allow data to be directly loaded into the 16-Bit Data Latch.

$Y_0 - Y_{15}$ Data Output Lines (Output)
When $\overline{OE}_Y$ is HIGH, the 16-bit Y outputs are disabled (high impedance); having $\overline{OE}_Y$ LOW allows the ALU data to be output on $Y_0 - Y_{15}$.

DLE Data Latch Enable (Input)
When DLE is HIGH, the 16-Bit Data Latch is transparent and is latched when DLE is LOW.

$\overline{OE}_Y$ Output Enable (Input)
When $\overline{OE}_Y$ is HIGH, the 16-bit Y outputs are disabled (high impedance); when $\overline{OE}_Y$ is LOW, the 16-bit Y outputs are enabled.

$I_0 - I_{15}$ Instruction Inputs (Input)
Sixteen Instruction Inputs, used to select the operation to be performed in the Am29C117. Also used as data inputs while performing immediate instructions.

$\overline{IEN}$ Instruction Enable (Input)
When $\overline{IEN}$ is LOW, data can be written into RAM when the clock is LOW. The Accumulator can accept data during the LOW-to-HIGH transition of the clock. Having $\overline{IEN}$ LOW, the Status Register can be updated when $\overline{SRE}$ is LOW. With $\overline{IEN}$ HIGH, the conditional test output, CT, is disabled as a function of the instruction inputs.

$\overline{SRE}$ Status Register Enable (Input)
When $\overline{SRE}$ and $\overline{IEN}$ are both LOW, the Status Register is updated at the end of all instructions with the exception of NO-OP, Save Status, and Test Status. Having either $\overline{SRE}$ or $\overline{IEN}$ HIGH will inhibit the Status Register from changing.

Clock Pulse (Input)
The clock input to the Am29C117. The RAM latch is transparent when the clock is HIGH. When the clock goes LOW, the RAM output is latched. Data is written into the RAM during the LOW period of the clock, provided $\overline{IEN}$ is LOW, and if the instruction being executed designates the RAM as the destination of operation. The Accumulator and Status Register will accept data on the LOW-to-HIGH transition of the clock if $\overline{IEN}$ is also LOW. The Instruction Latch becomes transparent when it exits an immediate instruction mode during a LOW-to-HIGH transition of the clock.

$T_1 - T_4$ Test I/O Pins (Input/Output)
Under the control of OE_T, the four lower status bits, Z, C, N, and OVR become outputs on $T_1 - T_4$, respectively, when OE_T goes HIGH. When OE_T is LOW, $T_1 - T_4$ are used as inputs to generate the CT output.

OE_T Output Enable (Input)
When OE_T is LOW, 4-bit T outputs are disabled (high impedance); when OE_T is HIGH, the 4-bit T outputs are enabled.

CT Conditional Test (Output)
The condition code multiplexer selects one of the twelve condition code signals and places it on the CT output. A HIGH on the CT output indicates a passed condition and a LOW indicates a failed condition.

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Suggestions for Power and Ground Pin Connections

The Am29C117 operates in an environment of fast signal rise times and substantial switching currents. Therefore, care must be exercised during circuit board design and layout, as with any high-performance component. The following is a suggested layout, but since systems vary widely in electrical configuration, an empirical evaluation of the intended layout is recommended.

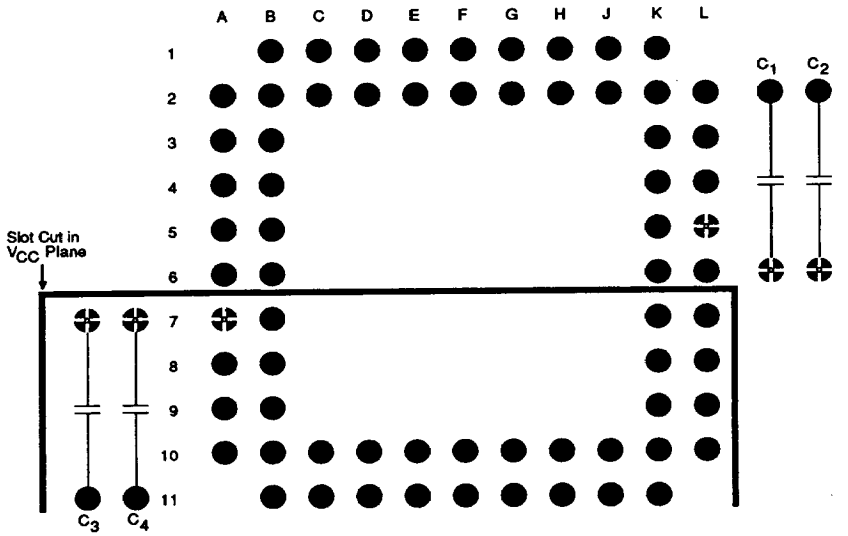
The V_{CC0} pin, which carries output driver switching currents, tends to be electrically noisy. The V_{CC} pins, which supply the internal logic of the device, tend to produce less noise, and the circuits they supply may be adversely affected by noise spikes on the V_{CC} plane. For this reason, it is best to provide isolation between the V_{CC0} and V_{CC} pins, as well as independent decoupling for each; isolating the GND pins is not required.

Printed Circuit Board Layout Suggestions

1. Use of a multilayer PC board with separate V_{CC}, GND, and signal planes is highly recommended.
2. The V_{CC0} and V_{CC} pins should be connected to the V_{CC} plane. The V_{CC0} pin should be isolated from the V_{CC} pins by means of a slot cut in the V_{CC} plane (see suggested layout diagram that follows). By physically separating the V_{CC0} and V_{CC} pins, coupled noise will be reduced.
3. All GND pins should be connected directly to the ground plane.
4. The V_{CC0} pin should be decoupled to ground with a 0.1-μF ceramic capacitor and a 10-μF electrolytic capacitor, placed as closely to the Am29C117 as is practical. The V_{CC} pins should be decoupled to ground in a similar manner.

A suggested layout is shown below:

Bottom View



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Suggested PC Board Layout

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FUNCTIONAL DESCRIPTION

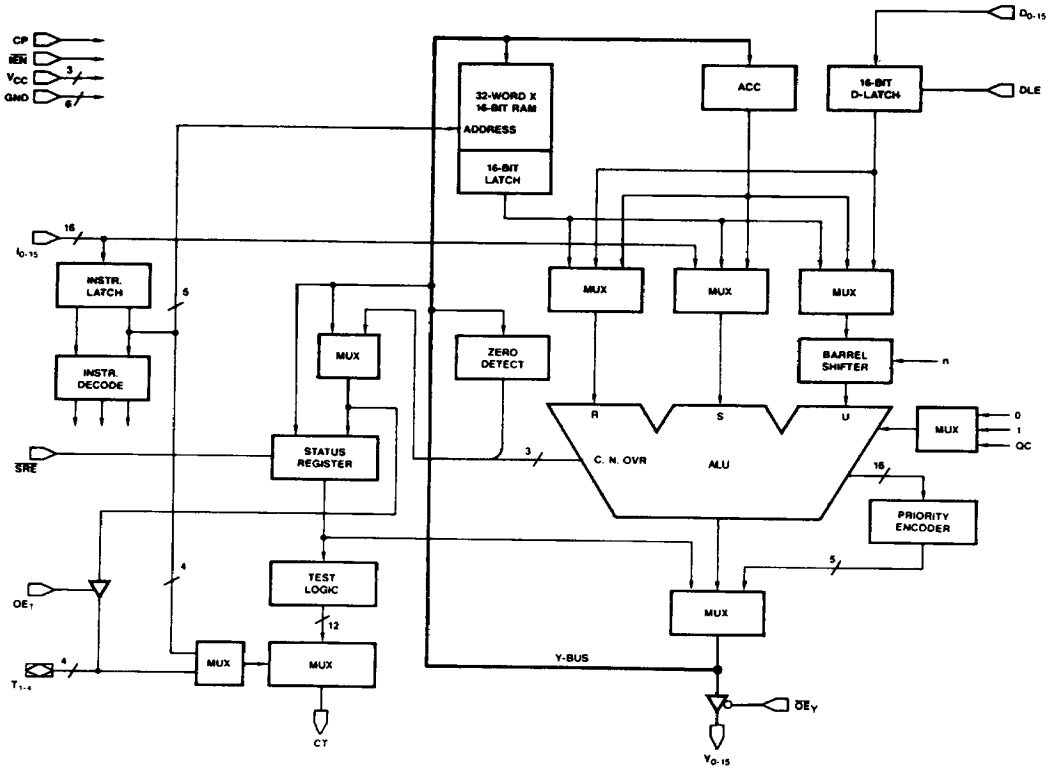

Figure 1. Detailed Block Diagram

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Architecture of the Am29C117

The Am29C117 is a high-performance, microprogrammable 16-bit CMOS microprocessor.

As shown in the Detailed Block Diagram (Figure 1), the device consists of the following elements interconnected with 16-bit data paths.

- 32-Word by 16-Bit RAM
- Accumulator
- Data Latch
- Barrel Shifter
- Arithmetic Logic Unit (ALU)
- Priority Encoder
- Status Register
- Condition-Code Generator/Multiplexer
- Three-State Output Buffers
- Instruction Latch and Decoder

32-Word by 16-Bit RAM

The 32-Word by 16-Bit RAM is a single-port RAM with a 16-bit latch at its output. The latches are transparent when the clock input (CP) is HIGH and latched when the clock input is LOW. Data is written into the RAM while the clock is LOW if the $\overline{IEN}$ input is also LOW and if the instruction being executed defines the RAM as the destination of the operation. For byte instructions, only the lower 8 RAM bits are written into; for word instructions, all 16 bits are written into. With the use of an external multiplexer on five of the instruction inputs, it is possible to select separate read and write addresses for the same instruction.

Accumulator

The 16-bit Accumulator is an edge-triggered register. The Accumulator accepts data on the LOW-to-HIGH transition of the clock input if the $\overline{IEN}$ input is LOW and if the instruction being executed defines the Accumulator as the destination of the operation. For byte instructions, only the lower 8 bits of the Accumulator are written into; for word instructions, all 16 bits are written into.

Data Latch

The 16-bit Data Latch holds the data input to the Am29C117 on the D bus. The latch is transparent when the DLE input is HIGH and latched when the DLE input is LOW.

Barrel Shifter

A 16-bit Barrel Shifter is used as one of the ALU inputs. This permits rotating data from either the RAM, the Accumulator, or the Data Latch up to 15 positions. In the word mode, the Barrel Shifter rotates a 16-bit word; in the byte mode, it rotates only the lower 8 bits.

Arithmetic Logic Unit (ALU)

The Am29C117 contains a 16-bit ALU with full carry look-ahead across all 16 bits in the arithmetic mode. The ALU is capable of operating on either one, two, or three operands, depending upon the instruction being executed. It has the ability to execute all conventional one- and two-operand operations, such as pass, complement, two's complement, add, subtract, AND, NAND, OR, NOR, EXOR, and EX-NOR. In addition, the ALU can also execute three-operand instructions such as Rotate and Merge, and Rotate and Compare with Mask. All ALU operations can be performed on either a word or byte basis; byte operations being performed on the lower eight bits only.

The ALU produces three status outputs, C (carry), N (negative), and OVR (overflow). The appropriate flags are generated at the byte or word level, depending upon whether the device is executing in the byte or word mode. The Z (zero) flag, although not generated by the ALU, detects zero at both the byte and word level.

The carry input to the ALU is generated by the Carry Multiplexer, which can select an input of zero, one, or the stored carry bit from the Status Register, QC. Using QC as the carry input allows execution of multiprecision addition and subtractions.

Priority Encoder

The Priority Encoder produces a binary-weighted code to indicate the locations of the highest order ONE at its input. The input to the Priority Encoder is generated by the ALU which performs an AND operation on the operand to be prioritized and a mask. The mask determines which bit locations to eliminate from prioritization. In the word mode, if no bit is HIGH, the output is a binary zero. If bit 15 is HIGH, the output is a binary one. Bit 14 produces a binary two, etc. Finally, if only bit 0 is HIGH, a binary 16 is produced.

In the byte mode, bits 8 through 15 do not participate. If none of bits 7 through 0 are HIGH, the output is a binary zero. If bit 7 is HIGH, a binary one is produced. Bit 6 produces a binary two, etc. Finally, if only bit 0 is HIGH, a binary 8 is produced.

Status Register

The Status Register holds the 8-bit status word. With the Status-Register Enable ($\overline{SRE}$) input LOW and the $\overline{IEN}$ input LOW, the Status Register is updated at the end of all instructions except NO-OP, Save-Status, and Test-Status instructions. $\overline{SRE}$ going HIGH or $\overline{IEN}$ going HIGH inhibits the Status Register from changing.

The lower four bits of the Status Register contain the ALU status bits of Zero (Z), Carry (C), Negative (N), and Overflow (OVR). The upper four bits contain a Link bit and three user-definable status bits (Flag1, Flag2, Flag3).

With $\overline{SRE}$ LOW and $\overline{IEN}$ LOW, the lower four status bits are updated after each instruction except those mentioned above: NO-OP, Save Status, Status Test, and the Status Set/Reset instruction for the upper four bits. Under the same conditions, the upper four status bits are changed only during their respective Status Set/Reset instructions and during Status Load instructions in the word mode. The Link-Status bit is also updated after each shift instruction.

The Status Register can be loaded from the internal Y-Bus, and can also be selected as a source for the internal Y-Bus. When the Status Register is loaded in the word mode, all 8 bits are updated; in the byte mode, only the lower 4 bits (Z, C, N, OVR) are updated.

When the Status Register is selected as a source in the word mode, all eight bits are loaded into the lower byte of the destination; the upper byte of the destination is loaded with all zeros. In the byte mode, the Status Register again loads into the lower byte of the destination, but the upper byte remains unchanged. This Store and Load combination allows saving and restoring the Status Register for interrupt and subroutine processing. The four lower status bits (Z, C, N, OVR) can be read directly via the bidirectional T-Bus. These four bits are available as outputs on the T_{1-4} outputs whenever OE_T is HIGH.

Condition-Code Generator/Multiplexer

The Condition-Code Generator/Multiplexer contains the logic necessary to develop the 12 condition-code test signals. The multiplexer portion can select one of these test signals and place it on the CT output for use by the microprogram sequencer. The Multiplexer may be addressed in two different ways. One way is through the Test Instruction. This instruction specifies the test condition to be placed in the CT output, but

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does not allow an ALU operation at the same time. The second method uses the bidirectional T-Bus as an input. This requires extra bits in the microword, but provides the ability to simultaneously test and execute. The test instruction lines, I_{0-4}, have priority over T_{1-4} for testing status.

Three-State Output Buffers

There are two sets of Three-State Output Buffers in the Am29C117. One set controls the 16-bit Y-Bus. These outputs are enabled by placing a LOW on the $\overline{OE}_Y$ input.

The second set of Three-State Output Buffers controls the bidirectional 4-bit T-Bus and is enabled by placing a HIGH on the OE_T input. This allows storing the four internal ALU status bits (Z, C, N, OVR) externally. A LOW OE_T input forces the T outputs into the high-impedance state. External devices can then drive the T-Bus to select a test condition for the CT output.

Instruction Latch and Decoder

The 16-bit Instruction Latch is normally transparent to allow decoding of the instruction inputs by the Instruction Decoder into the internal control signals for the Am29C117. All instructions except Immediate Instructions are executed in a single clock cycle.

Immediate instructions require two clock cycles for execution. During the first clock cycle, the Instruction Decoder recognizes that an immediate instruction is being specified and captures the data on the instruction inputs in the Instruction Latch. During the second clock cycle, the data on the instruction inputs is used as one of the operands for the function specified during the first clock cycle. At the end of the second clock cycle, the Instruction Latch is returned to its transparent state.

Instruction Set

The instruction set of the Am29C117 is very powerful. In addition to the single- and two-operand logical and arithmetic instructions, the Am29C117 instruction set contains functions particularly useful in controller applications: bit set, bit reset, bit test, rotate and merge, rotate and compare, and cyclic-redundancy-check (CRC) generation. Complex instructions like Rotate and Merge, Rotate and Compare, and Prioritize are executed in a single mircocycle.

Three data types are supported by the Am29C117.

- Bit
- Byte
- Word (16-bit)

In the byte mode data is written into the lower half of the word and the upper half is unchanged. The special case is when the Status Register is specified as the destination. In the byte mode, the LSH (OVR, N, C, Z) of the Status Register is updated; and in the word mode, all eight bits of the Status Register are updated. The Status Register does not change for Save Status and Test Status instructions. In the Test Status instructions the CT output has the result and the Y-Bus is undefined.

The Am29C117 Instruction Set can be divided into eleven types of instructions. These are:

- Single Operand
- Two Operand
- Single Bit Shift
- Rotate and Merge
- Bit Oriented
- Rotate by n Bits
- Rotate and Compare
- Prioritize
- Cyclic-Redundancy-Check
- Status
- No-Operation (NO-OP)

Each instruction type is arbitrarily divided into quadrants. Two of the sixteen instruction lines decode to four quadrants labeled from 0 to 3. The quadrants were defined mainly for convenience in classification of the instruction set and addressing modes, and can be used together with the opcodes to distinguish the instructions.

The following pages describe each of the instruction types in detail. Table 1 illustrates Operand Source-Destination Combinations for each instruction type.

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TABLE 1. OPERAND SOURCE-DESTINATION COMBINATIONS

Instruction Type	Operand Combinations (Note 1)		
	Source (R/S)		Destination
Single Operand	RAM (Note 2) ACC D D(0E) D(SE) I 0		RAM ACC Y-Bus Status ACC and Status
	Source (R)	Source (S)	Destination
Two Operand	RAM RAM D D ACC D	ACC I RAM ACC I I	RAM ACC Y-Bus Status ACC and Status
	Source (U)		Destination
Single Bit Shift	RAM ACC ACC D D D		RAM ACC Y-Bus RAM ACC Y-Bus
	Source (R/S)		Destination
Bit Oriented	RAM ACC D		RAM ACC Y-Bus
	Source (U)		Destination
Rotate By n Bits	RAM ACC D		RAM ACC Y-Bus
	Rotated Source (U)	Mask (S)	Non-Rotated Source/ Destination (R)
Rotate and Merge	D D D D ACC RAM	I RAM I ACC I I	ACC ACC RAM RAM RAM ACC
	Rotated Source (U)	Mask (S)	Non-Rotated Source/ Destination (R)
Rotate and Compare	D D D RAM	I I ACC I	 RAM RAM ACC

Instruction Type	Operand Combinations (Note 1)		
	Source (R)	Mask (S)	Destination
Prioritize (Note 3)	RAM ACC D	RAM ACC I 0	RAM ACC Y-Bus
	Data In	Destination	Polynomial
Cyclic-Redundancy-Check (CRC)	QLINK	RAM	ACC
	Bits Affected		
Set Reset Status	OVR, N, C, Z LINK Flag1 Flag2 Flag3		
	Source		Destination
Store Status	Status		RAM ACC Y-Bus
	Source (R)	Source (S)	Destination
Status Load	D ACC D	ACC I I	Status Status and ACC
	Test Condition (CT)		
Test Status	(N⊕OVR) + Z N⊕OVR Z OVR Low C Z + $\overline{C}$ N LINK Flag1 Flag2 Flag3		
No Operation (NO-OP)	-		

Notes: 1. When there is no dividing line between the R & S Operand or Source and Destination, the two must be used as a given pair. But where there exists such a separation, any combination of them is possible.
2. In the Single Operand Instruction, RAM cannot be used when both Accumulator (ACC) and Status are designated as a Destination.
3. In the Prioritize Instruction, Operand and Mask must be different sources.

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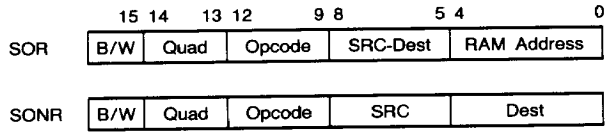
Single Operand Instructions

The Single Operand Instructions contain four indicators: Byte or Word mode, Opcode, Source, and Destination. They are further subdivided into two types. The first type uses RAM as a source or destination or both, and the second type does not use RAM as a source or destination. Both types have different instruction formats as shown below. Under the control of instruction inputs, the desired function is performed on the source and the result is either stored in the specified destination or placed on the Y-Bus, or both. For a special case where 8-bit to 16-bit conversion is needed, the Am29C117 is capable of extending sign bit (D(SE)) or binary zero (D(0E)) over 16 bits in the word mode. The least significant four bits of the Status Register (OVR, N, C, Z) are affected by the function performed in this category. The most significant bits of the Status Register (Flag1, Flag2, Flag3, LINK) are not affected. The only limitation in this type is that the RAM cannot be used as a source when both the Accumulator (ACC) and the Status Register are specified as a destination.

SINGLE OPERAND FIELD DEFINITIONS:



SINGLE OPERAND INSTRUCTION

15 14 13 12 9 8 5 4 0

Instruction[1]	B/W[2]	Quad[3]	Opcode	R/S[4]	Dest[4]	RAM Address
SOR	0 = B 1 = W	10	1100 MOVE SRC → Dest 1101 COMP $\overline{SRC}$ → Dest 1110 INC SRC + 1 → Dest 1111 NEG $\overline{SRC}$ + 1 → Dest	0000 SORA RAM ACC 0010 SORY RAM Y-Bus 0011 SORS RAM Status 0100 SOAR ACC RAM 0110 SODR D RAM 0111 SOIR I RAM 1000 SOZR 0 RAM 1001 SOZER D(0E) RAM 1010 SOSER D(SE) RAM 1011 SORR RAM RAM		00000 R00 RAM Reg 00 .. .. 11111 R31 RAM Reg 31

Instruction	B/W	Quad	Opcode	R/S[4]	Destination
SONR	0 = B 1 = W	11	1100 MOVE SRC → Dest 1101 COMP $\overline{SRC}$ → Dest 1110 INC SRC + 1 → Dest 1111 NEG $\overline{SRC}$ + 1 → Dest	0100 SOA ACC 0110 SOD D 0111 SOI I 1000 SOZ 0 1001 SOZE D(0E) 1010 SOSE D(SE)	00000 NRY Y-Bus 00001 NRA ACC 00100 NRS Status[5] 00101 NRAS ACC, Status[5]

Notes:
1. The instruction mnemonic designates different instruction formats used in the Am29C117. They are useful in microcode assembly.
2. B = Byte Mode, W = Word Mode.
3. See Instruction Set description.
4. R = Source; S = Source; Dest = Destination.
5. When status is destination,
   Status i ← Yi i = 0 to 3 (Byte mode)
   i = 0 to 7 (Word mode)

Y-BUS AND STATUS — SINGLE OPERAND INSTRUCTIONS

Instruction	Opcode	Description	B/W	Y-Bus	Flag3	Flag2	Flag1	LINK	OVR	N	C	Z
SOR SONR	MOVE	SRC → Dest	0 = B 1 = W	Y ← SRC	NC	NC	NC	NC	0	U	0	U
	COMP	$\overline{SRC}$ → Dest		Y ← $\overline{SRC}$	NC	NC	NC	NC	0	U	0	U
	INC	SRC +1 → Dest		Y ← SRC +1	NC	NC	NC	NC	U	U	U	U
	NEG	$\overline{SRC}$ +1 → Dest		Y ← $\overline{SRC}$ +1	NC	NC	NC	NC	U	U	U	U

SRC = Source
U = Update
NC = No Change

0 = Reset
1 = Set
i = 0 to 15 when not specified

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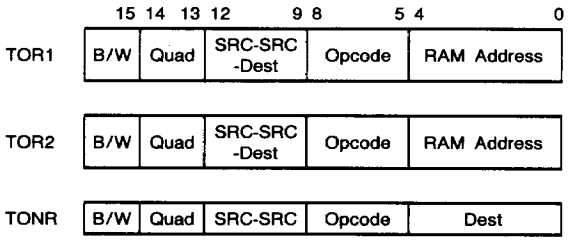
Two Operand Instructions

The Two Operand Instructions contain five indicators: Byte or Word mode, Opcode, R Source, S Source, and Destination. They are further subdivided into two types. The first type uses RAM as the source and/or destination and the second type does not use RAM as source or destination. The first type has two formats; the only difference is in the quadrant. Under the control of instruction inputs, the desired function is performed on the specified sources and the result is stored in the specified destination or placed on the Y-Bus, or both. The least significant four bits of the Status Register (OVR, N, C, Z) are affected by the arithmetic functions performed and only the N and Z bits are affected by the logical functions performed. The OVR and C bits of the Status Register are forced to ZERO for logical functions. Add with carry and Subtract with carry instructions are useful for Multiprecision Add or Subtract.

TWO OPERAND FIELD DEFINITIONS:



TWO OPERAND INSTRUCTIONS (Cont'd.)

Instruction	B/W	Quad			R[1]	S[1]	Dest[1]	Opcode			RAM Address		
TOR1	0 = B 1 = W	00	0000 0010 0011 1000 1010 1011 1100 1110 1111	TORAA TORIA TODRA TORAY TORIY TODRY TORAR TORIR TODRR	RAM RAM D RAM RAM D RAM RAM D	ACC I RAM ACC I RAM ACC I RAM	ACC ACC ACC Y-Bus Y-Bus Y-Bus RAM RAM RAM	0000 0001 0010 0011 0100 0101 0110 0111 1000 1001 1010 1011	SUBR SUBRC[2] SUBS SUBSC[2] ADD ADDC AND NAND EXOR NOR OR EXNOR	S minus R S minus R with carry R minus S R minus S with carry R plus S R plus S with carry R • S R • S R ⊕ S R + S R + S R ⊕ S	00000 . . 11111	R00 . . R31	RAM Reg 00 . . . . RAM Reg 31
Instruction	**B/W**	**Quad**			**R[1]**	**S[1]**	**Dest[1]**	**Opcode**			**RAM Address**		
TOR2	0 = B 1 = W	10	0001 0010 0101	TODAR TOAIR TODIR	D ACC D	ACC I I	RAM RAM RAM	0000 0001 0010 0011 0100 0101 0110 0111 1000 1001 1010 1011	SUBR SUBRC[2] SUBS SUBSC[2] ADD ADDC AND NAND EXOR NOR OR EXNOR	S minus R S minus R with carry R minus S R minus S with carry R plus S R plus S with carry R • S R • S R ⊕ S R + S R + S R ⊕ S	00000 . . 11111	R00 . . R31	RAM Reg 00 . . . . RAM Reg 31

Notes: 1. R = Source
S = Source
Dest = Destination
2. During subtraction the carry is interpreted as $\overline{\text{borrow}}$.

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TWO OPERAND INSTRUCTIONS

Instruction	B/W	Quad	R[1]	S[1]	Opcode			Destination		
TONR	0 = B 1 = W	11	0001 TODA 0010 TOAI 0101 TODI	D ACC ACC I D I	0000 0001 0010 0011 0100 0101 0110 0111 1000 1001 1010 1011	SUBR SUBRC[3] SUBS SUBSC[3] ADD ADDC AND NAND EXOR NOR OR EXNOR	S minus R S minus R with carry R minus S R minus S with carry R plus S R plus S with carry $\underline{R \cdot S}$ $\overline{R \cdot S}$ $\underline{R \oplus S}$ $\overline{R + S}$ $\underline{R + S}$ $\overline{R \oplus S}$	00000 00001 00100 00101	NRY NRA NRS NRAS	Y-Bus ACC Status[2] ACC, Status[2]

Notes: 1. R = Source
S = Source
2. When status is destination,
Status $i \leftarrow Y_i$ i = 0 to 3 (Byte mode)
i = 0 to 7 (Word mode)
3. During subtraction the carry is interpreted as $\overline{\text{borrow}}$.

Y-BUS AND STATUS CONTENTS — TWO OPERAND INSTRUCTIONS

Instruction	Opcode	Description	B/W	Y-Bus	Flag3	Flag2	Flag1	LINK	OVR	N	C	Z
TOR1 TOR2 TONR	SUBR	S minus R	0 = B	$Y \leftarrow S + \overline{R} + 1$	NC	NC	NC	NC	U	U	U	U
	SUBRC	S minus R with carry	1 = W	$Y \leftarrow S + \overline{R} + QC$	NC	NC	NC	NC	U	U	U	U
	SUBS	R minus S		$Y \leftarrow R + \overline{S} + 1$	NC	NC	NC	NC	U	U	U	U
	SUBSC	R minus S with carry		$Y \leftarrow R + \overline{S} + QC$	NC	NC	NC	NC	U	U	U	U
	ADD	R plus S		$Y \leftarrow R + S$	NC	NC	NC	NC	U	U	U	U
	ADDC	R plus S with carry		$Y \leftarrow R + S + QC$	NC	NC	NC	NC	U	U	U	U
	AND	$R \cdot S$		$Y \leftarrow R_i$ AND S_i	NC	NC	NC	NC	0	U	0	U
	NAND	$\overline{R \cdot S}$		$Y_i \leftarrow R_i$ NAND S_i	NC	NC	NC	NC	0	U	0	U
	EXOR	$R \oplus S$		$Y_i \leftarrow R_i$ EXOR S_i	NC	NC	NC	NC	0	U	0	U
	NOR	$\overline{R + S}$		$Y_i \leftarrow R_i$ NOR S_i	NC	NC	NC	NC	0	U	0	U
	OR	$R + S$		$Y_i \leftarrow R_i$ OR S_i	NC	NC	NC	NC	0	U	0	U
	EXNOR	$\overline{R \oplus S}$		$Y_i \leftarrow R_i$ EXNOR S_i	NC	NC	NC	NC	0	0	0	U

U = Update
NC = No Change
0 = Reset
1 = Set
i = 0 to 15 when not specified

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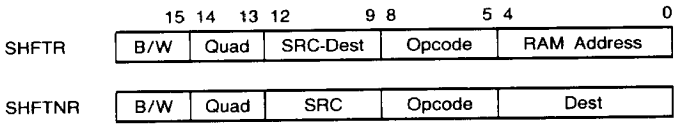
Single Bit Shift Instructions

The Single Bit Shift Instructions contain four indicators: Byte or Word mode, Direction and Shift Linkage, Source, and Destination. They are further subdivided into two types. The first type uses RAM as the source and/or destination and the second type does not use RAM as source or destination. Under the control of the instruction inputs, the desired shift function is performed on the specified source and the result is stored in the specified destination or placed on the Y-Bus, or both. The direction and shift linkage indicator defines the direction of the shift (up or down) as well as what will be shifted into the vacant bit. On a shift-up instruction, the LSB may be loaded with ZERO, ONE, or the Link-Status bit (QLINK). The MSB is loaded into the Link-Status bit as shown in Figure 2. On a shift-down instruction, the MSB may be loaded with ZERO, ONE, the contents of the Status Carry flip-flop, (QC), the Exclusive-OR of the Negative-Status bit, and the Overflow-Status bit (QN ⊕ QOVR), or the Link-Status bit. The LSB is loaded into the Link-Status bit as shown in Figure 3. The N and Z bits of the Status Register are affected but the OVR and C bits are forced to ZERO. The Shift-Down with QN ⊕ QOVR is useful for Two's Complement multiplication.

SINGLE BIT SHIFT FIELD DEFINITIONS:



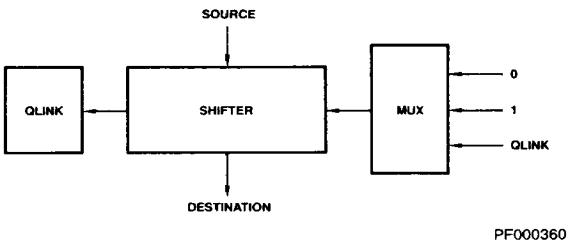


Figure 2. Shift-Up Function

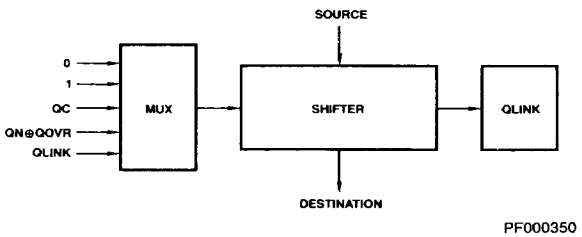


Figure 3. Shift-Down Function

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SINGLE BIT SHIFT INSTRUCTIONS

Instruction	B/W	Quad	U[1]		Dest[1]	Opcode			RAM Address
SHFTR	0 = B 1 = W	10	0110 0111	SHRR SHDR	RAM D	0000 SHUPZ Up 0 0001 SHUP1 Up 1 0010 SHUPL Up QLINK 0100 SHDNZ Down 0 0101 SHDN1 Down 1 0110 SHDNL Down QLINK 0111 SHDNC Down QC 1000 SHDNOV Down QN⊕QOVR			00000 R00 RAM Reg 00 . . . . . . 11111 R31 RAM Reg 31

Instruction	B/W	Quad	U[1]			Opcode			Destination
SHFTNR	0 = B 1 = W	11	0110 0111	SHA SHD	ACC D	0000 SHUPZ Up 0 0001 SHUP1 Up 1 0010 SHUPL Up QLINK 0100 SHDNZ Down 0 0101 SHDN1 Down 1 0110 SHDNL Down QLINK 0111 SHDNC Down QC 1000 SHDNOV Down QN⊕QOVR			00000 NRY Y-Bus 00001 NRA ACC

Note 1. U = Source
Dest = Destination

Y-BUS AND STATUS — SINGLE BIT SHIFT INSTRUCTIONS

Instruction	Opcode	Description	B/W	Y-Bus	Flag3	Flag2	Flag1	LINK	OVR	N	C	Z
SHR SHNR	SHUPZ SHUP1 SHUPL	Up 0 Up 1 Up QLINK	1 = W	$Y_i \leftarrow SRC_{i-1}$, i = 1 to 15; $Y_0 \leftarrow$ Shift Input	NC	NC	NC	SRC_{15}*	0	SRC_{14}	0	U
			0 = B	$Y_i \leftarrow SRC_{i-1}$, i = 1 to 7; $Y_0 \leftarrow$ Shift Input; $Y_8 \leftarrow SRC_7$, $Y_i \leftarrow SRC_{i-8}$ for i = 9 to 15	NC	NC	NC	SRC_7*	0	SRC_6	0	U
	SHDNZ SHDN1 SHDNL SHDNC SHCNOV	Down 0 Down 1 Down QLINK Down QC Down QN⊕QOVR	1 = W	$Y_i \leftarrow SRC_{i+1}$, i = 0 to 14; $Y_{15} \leftarrow$ Shift Input	NC	NC	NC	SRC_0*	0	Shift Input	0	U
			0 = B	$Y_i \leftarrow SRC_{i+1}$, i = 0 to 6; $Y_i \leftarrow SRC_{i-7}$, i = 8 to 14; $Y_{7,15} \leftarrow$ Shift Input	NC	NC	NC	SRC_0*	0	Shift Input	0	U

SRC = Source
U = Update
NC = No Change
0 = Reset
1 = Set
i = 0 to 15 when not specified

*Shifted Output is loaded into the QLINK.

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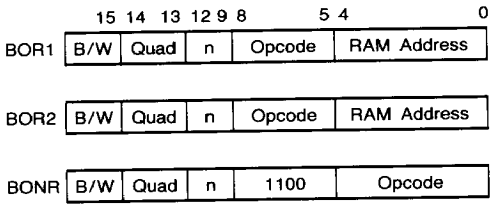
Bit Oriented Instructions

The Bit Oriented Instructions contain four indicators: Byte or Word mode, Operation, Source/Destination, and the Bit Position of the bit to be operated on (Bit 0 is the least significant bit). They are further subdivided into two types. The first type uses the RAM as both source and destination and has two kinds of formats which differ only by quadrant. The second type does not use the RAM as a source or a destination. Under the control of the instruction inputs, the desired function is performed on the specified source and the result is stored in the specified destination or placed on the Y-Bus, or both. The operations which can be performed are: Set Bit n which forces the n^{th} bit to a ONE leaving other bits unchanged; Reset Bit n which forces the n^{th} bit to ZERO leaving the other bits unchanged; Test Bit n, which sets the ZERO Status Bit depending on the state of bit n leaving all the bits unchanged; Load 2^n, which loads ONE in Bit position n and ZERO in all other bit positions; Load $\overline{2^n}$ which loads ZERO in bit position n and ONE in all other bit positions; increment by 2^n, which adds 2^n to the operand; and decrement by 2^n which subtracts 2^n from the operand. For all the Load, Set, Reset and Test instructions, the N and Z bits are affected and OVR and C bit of the Status Register are forced to ZERO. For all arithmetic instructions the LSH (OVR, C, N, Z bits) of the Status Register is affected.

BIT ORIENTED FIELD DEFINITIONS:



BIT ORIENTED INSTRUCTIONS

Instruction	B/W	Quad	n	Opcode			RAM Address		
BOR1	0 = B 1 = W	11	0 to 15	1101 1110 1111	SETNR RSTNR TSTNR	Set RAM, Bit n Reset RAM, Bit n Test RAM, Bit n	00000 .. 11111	R00 .. R31	RAM Reg 00 .... RAM Reg 31
Instruction	**B/W**	**Quad**	**n**	**Opcode**			**RAM Address**		
BOR2	0 = B 1 = W	10	0 to 15	1100 1101 1110 1111	LD2NR LDC2NR A2NR S2NR	$2^n \rightarrow$RAM $\overline{2^n} \rightarrow$RAM RAM plus $2^n \rightarrow$RAM RAM minus $2^n \rightarrow$RAM	00000 .. 11111	R00 .. R31	RAM Reg 00 .... RAM Reg 31
Instruction	**B/W**	**Quad**	**n**				**Opcode**		
BONR	0 = B 1 = W	11	0 to 15	1100			00000 00001 00010 00100 00101 00110 00111 10000 10001 10010 10100 10101 10110 10111	TSTNA RSTNA SETNA A2NA S2NA LD2NA LDC2NA TSTND RSTND SETND A2NDY S2NDY LS2NY LDC2NY	Test ACC, Bit n Reset ACC, Bit n Set ACC, Bit n ACC plus $2^n \rightarrow$ACC ACC minus $2^n \rightarrow$ACC $2^n \rightarrow$ACC $\overline{2^n} \rightarrow$ACC Test D, Bit n Reset D, Bit n Set D, Bit n D plus $2^n \rightarrow$ Y-Bus D minus $2^n \rightarrow$ Y-Bus $2^n \rightarrow$ Y-Bus $\overline{2^n} \rightarrow$ Y-Bus

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Y-BUS AND STATUS — BIT ORIENTED INSTRUCTIONS

Instruction	Opcode	Description	B/W	Y-Bus	Flag3	Flag2	Flag1	LINK	OVR	N	C	Z
BOR1	SETNR RSTNR	Set RAM, Bit n Reset RAM, Bit n	0 = B 1 = W	$Y_i \leftarrow RAM_i$ for $i \neq n$; $Y_n \leftarrow 1$ $Y_i \leftarrow RAM_i$ for $i \neq n$; $Y_n \leftarrow 0$	NC NC	NC NC	NC NC	NC NC	0 0	U U	0 0	0 U
	TSTNR	Test RAM, Bit n		$Y_i \leftarrow 0$ for $i \neq n$; $Y_n \leftarrow SRC_n$	NC	NC	NC	NC	0	U	0	U
BOR2	LD2NR	$2^n \rightarrow$ RAM		$Y_i \leftarrow 0$ for $i \neq n$; $Y_n \leftarrow 1$	NC	NC	NC	NC	0	U	0	0
	LDC2NR	$\overline{2^n} \rightarrow$ RAM		$Y_i \leftarrow 1$ for $i \neq n$; $Y_n \leftarrow 0$	NC	NC	NC	NC	0	U	0	0
	A2NR	RAM + $2^n \rightarrow$ RAM		$Y \leftarrow RAM + 2^n$	NC	NC	NC	NC	U	U	U	U
	S2NR	RAM – $2^n \rightarrow$ RAM		$Y \leftarrow RAM - 2^n$	NC	NC	NC	NC	U	U	U	U
BONR	TSTNA	Test ACC, Bit n		$Y_i \leftarrow 0$ for $i \neq n$; $Y_n \leftarrow ACC_n$	NC	NC	NC	NC	0	U	0	U
	RSTNA	Reset ACC, Bit n		$Y_i \leftarrow ACC_i$ for $i \neq n$; $Y_n \leftarrow 0$	NC	NC	NC	NC	0	U	0	U
	SETNA	Set ACC, Bit n		$Y_i \leftarrow ACC_i$ for $i \neq n$; $Y_n \leftarrow 1$	NC	NC	NC	NC	0	U	0	0
	A2NA	ACC + $2^n \rightarrow$ ACC		$Y \leftarrow ACC + 2^n$	NC	NC	NC	NC	U	U	U	U
	S2NA	ACC – $2^n \rightarrow$ ACC		$Y \leftarrow ACC - 2^n$	NC	NC	NC	NC	U	U	U	U
	LD2NA	$2^n \rightarrow$ ACC		$Y_i \leftarrow 0$ for $i \neq n$; $Y_n \leftarrow 1$	NC	NC	NC	NC	0	U	0	0
	LDC2NA	$\overline{2^n} \rightarrow$ ACC		$Y_i \leftarrow 1$ for $i \neq n$; $Y_n \leftarrow 0$	NC	NC	NC	NC	0	U	0	0
	TSTND	Test D, Bit n		$Y_i \leftarrow 0$ for $i \neq n$; $Y_n \leftarrow D_n$	NC	NC	NC	NC	0	U	0	U
	RSTND	Reset D, Bit n*		$Y_i \leftarrow D_i$ for $i \neq n$; $Y_n \leftarrow 0$	NC	NC	NC	NC	0	U	0	U
	SETND	Set D, Bit n*		$Y_i \leftarrow D_i$ for $i \neq n$; $Y_n \leftarrow 1$	NC	NC	NC	NC	0	U	0	0
	A2NDY	D + $2^n \rightarrow$ Y-Bus		$Y \leftarrow D + 2^n$	NC	NC	NC	NC	U	U	U	U
	S2NDY	D – $2^n \rightarrow$ Y-Bus		$Y \leftarrow D - 2^n$	NC	NC	NC	NC	U	U	U	U
	LD2NY	$2^n \rightarrow$ Y-Bus		$Y_i \leftarrow 0$ for $i \neq n$; $Y_n \leftarrow 1$	NC	NC	NC	NC	0	U	0	0
	LDC2NY	$\overline{2^n} \rightarrow$ Y-Bus		$Y_i \leftarrow 1$ for $i \neq n$; $Y_n \leftarrow 0$	NC	NC	NC	NC	0	U	0	0

SRC = Source
U = Update
NC = No Change
0 = Reset
1 = Set
i = 0 to 15 when not specified

*Destination is not D-Latch but Y-Bus.

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Rotate By n Bits Instructions

The Rotate By n Bits Instructions contain four indicators: Byte or Word mode, Source, Destination, and the number of places the source is to be rotated. They are further subdivided into two types. The first type uses RAM as a source and/or a destination and the second type does not use RAM as a source or destination. The first type has two different formats and the only difference is in the quadrant. The second type has only one format as shown in the table. Under the control of instruction inputs, the n indicator specifies the number of bit positions the source is to be rotated up (0 to 15), and the result is either stored in the specified destination or placed on the Y-Bus, or both. An example of this instruction is given in Figure 4. In the Word mode, all 16 bits are rotated up while in the Byte mode, only the lower 8 bits (0-7) are rotated up. In the Word mode, a rotate up by n bits is equivalent to a rotate down by (16-n) bits. Similarly, in the Byte mode a rotate up by n bits is equivalent to a rotate down by (8-n) bits. The N and Z bits of the Status Register are affected and OVR and C bits are forced to ZERO.

n = 4, Word Mode:

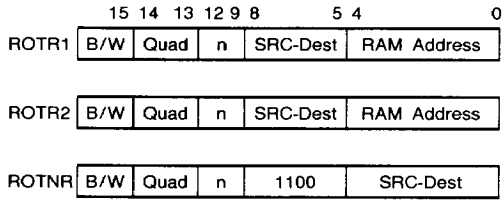
Source	0001	0011	0111	1111
Destination	0011	0111	1111	0001

n = 4, Byte Mode:

Source	0001	0011	0111	1111
Destination	0001	0011	1111	0111

Figure 4. Rotate By n Example

ROTATE BY n BITS FIELD DEFINITIONS:



ROTATE BY n BITS INSTRUCTIONS

Instruction	B/W	Quad	n	U[1]		Dest[1]	RAM Address		
ROTR1	0 = B 1 = W	00	0 to 15	1100 1110 1111	RTRA RTRY RTRR	RAM RAM RAM	ACC Y-Bus RAM	00000 . 11111	R00 . R31	RAM Reg 00 . RAM Reg 31
Instruction	**B/W**	**Quad**	**n**	**U[1]**		**Dest[1]**	**RAM Address**		
ROTR2	0 = B 1 = W	01	0 to 15	0000 0001	RTAR RTDR	ACC D	RAM RAM	00000 . 11111	R00 . R31	RAM Reg 00 . RAM Reg 31
Instruction	**B/W**	**Quad**	**n**				**U[1]**	**Dest[1]**	
ROTNR	0 = B 1 = W	11	0 to 15	1100			11000 11001 11100 11101	RTDY RTDA RTAY RTAA	D D ACC ACC	Y-Bus ACC Y-Bus ACC

Note: 1. U = Source
Dest = Destination

Y-BUS AND STATUS — ROTATE BY n BITS INSTRUCTIONS

Instruction	Op-code	B/W	Y-Bus	Flag3	Flag2	Flag1	LINK	OVR	N	C	Z
ROTR1 ROTR2 ROTNR		1 = W	$Y_i \leftarrow SRC_{(i-n) \bmod 16}$	NC	NC	NC	NC	0	SRC_{15-n}	0	U
		0 = B	$Y_i \leftarrow SRC_{i+8} = SRC_{(i-n) \bmod 8}$ for i = 0 to 7	NC	NC	NC	NC	0	SRC_{8-n}	0	U

SRC = Source
U = Update
NC = No Change
0 = Reset
1 = Set
i = 0 to 15 when not specified

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Rotate and Merge Instructions

The Rotate and Merge Instructions contain five indicators: Byte or Word mode, Rotated Source, Non-Rotated Source/ Destination, Mask, and the number of bit positions a source is to be rotated. The function performed by the Rotate and Merge instruction is illustrated in Figure 5. The rotated source, U, is rotated up by the Barrel Shifter n places. The mask input then selects, on a bit-by-bit basis, the rotated U input or R input. A ZERO in bit i of the mask will select the i^{th} bit of the R input as the i^{th} output bit, while ONE in bit i will select the i^{th} rotated U input as the output bit. The output word is stored in the non-rotated operand location. The N and Z bits are affected. The OVR and C bits of the Status Register are forced to ZERO. An example of this instruction is given in Figure 6.

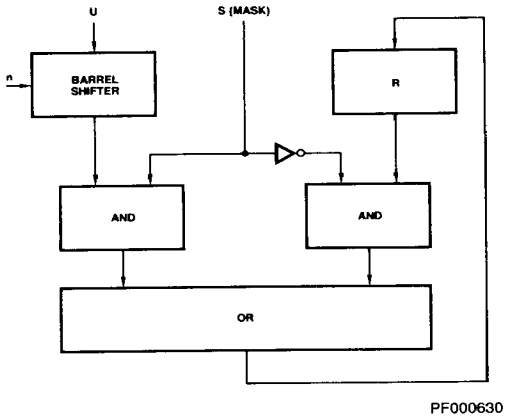

Figure 5. Rotate and Merge Function

n = 4, Word Mode:

U	0011	0001	0101	0110
Rotated U	0001	0101	0110	0011
R	1010	1010	1010	1010
Mask (S)	0000	1111	0000	1111
Destination	1010	0101	1010	0011

Figure 6. Rotate and Merge Example

ROTATE AND MERGE FIELD DEFINITIONS:

	15 14	13 12 9 8		5 4	0
ROTM	B/W	Quad	n	ROT SRC- Non ROT SRC- Mask	RAM Address

ROTATE AND MERGE INSTRUCTION

Instruction	B/W	Quad	n			U[1]	R/Dest[1]	S[1]	RAM Address		
ROTM	0 = B 1 = W	01	0 to 15	0111	MDAI	D	ACC	I	00000	R00	RAM Reg 00
				1000	MDAR	D	ACC	RAM	..	..	....
				1001	MDRI	D	RAM	I	11111	R31	RAM Reg 31
				1010	MDRA	D	RAM	ACC			
				1100	MARI	ACC	RAM	I			
				1110	MRAI	RAM	ACC	I			

U = Rotated Source
R/Dest = Non-Rotated Source and Destination
S = Mask

Y-BUS AND STATUS — ROTATE AND MERGE INSTRUCTIONS

Instruction	Opcode	B/W	Y-Bus	Flag3	Flag2	Flag1	LINK	OVR	N	C	Z
ROTM		1=W	$Y_i \leftarrow (\text{Non Rot Op})_i \cdot \overline{(\text{mask})_i} + (\text{Rot Op})_{(i-n) \bmod 16} \cdot (\text{mask})_i$	NC	NC	NC	NC	0	U	0	U
		0 = B	$Y_i \leftarrow (\text{Non Rot Op})_i \cdot \overline{(\text{mask})_i} + (\text{Rot Op})_{(i-n) \bmod 8} \cdot (\text{mask})_i$	NC	NC	NC	NC	0	U	0	U

U = Update
NC = No Change
0 = Reset
1 = Set
i = 0 to 15 when not specified

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Rotate and Compare Instructions

The Rotate and Compare Instructions contain five indicators: Byte or Word mode, Rotated Source, Non-Rotated Source, Mask, and the number of bit positions the rotated source is to be rotated up. Under the control of instruction inputs, the function performed by the Rotate and Compare Instruction is illustrated in Figure 7. The rotated operand is rotated by the Barrel Shifter n places. The mask is inverted and ANDed on a bit-by-bit basis with the output of the Barrel Shifter and R input. Thus, a ONE in the mask input eliminates that bit from the comparison. A ZERO allows the comparison. If the comparison passes, the Zero flag is set. If it fails, the Zero flag is reset. The N and Z bit are affected. The OVR and C bits of the Status Register are forced to ZERO. An example of this instruction is given in Figure 8.

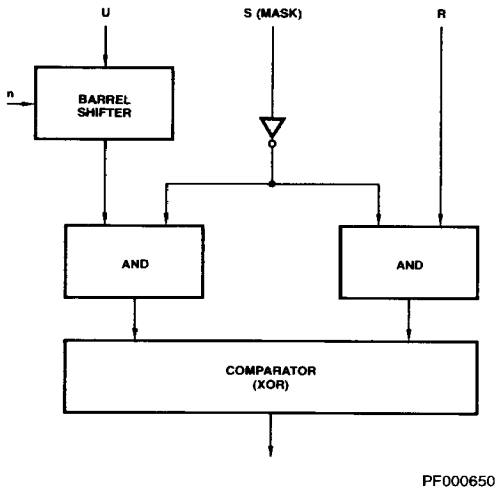


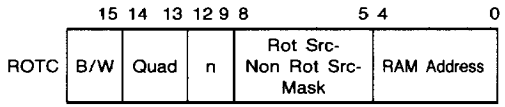
Figure 7. Rotate and Compare Function

n = 4, Word Mode

U	0011	0001	0101	0110
U Rotated	0001	0101	0110	0011
R	0001	0101	1111	0000
Mask (S)	0000	0000	1111	1111
Z (status) = 1				

Figure 8. Rotate and Compare Example

ROTATE AND COMPARE FIELD DEFINITIONS:



ROTATE AND COMPARE INSTRUCTIONS

Instruction	B/W	Quad	n			U[1]	R[1]	S[1]	RAM Address		
ROTC	0 = B 1 = W	01	0 to 15	0010 0011 0100 0101	CDAI CDRI CDRA CRAI	D D D RAM	ACC RAM RAM ACC	I I ACC I	00000 .. 11111	R00 .. R31	RAM Reg 00 ... RAM Reg 31

U = Rotated Source
R = Non-Rotated Source
S = Mask

Y-BUS AND STATUS — ROTATE AND COMPARE INSTRUCTIONS

Instruction	Opcode	B/W	Y-Bus	Flag3	Flag2	Flag1	LINK	OVR	N	C	Z
ROTC		1 = W	$Y_i \leftarrow (\text{Non Rot Op})_i \cdot \overline{(\text{mask})}_i \oplus (\text{Rot Op})_{(i-n) \bmod 16} \cdot \overline{(\text{mask})}_i$	NC	NC	NC	NC	0	U	0	U
		0 = B	$Y_i \leftarrow (\text{Non Rot Op})_i \cdot \overline{(\text{mask})}_i \oplus (\text{Rot Op})_{(i-n) \bmod 8} \cdot \overline{(\text{mask})}_i$	NC	NC	NC	NC	0	U	0	U

U = Update
NC = No Change
0 = Reset
1 = Set
i = 0 to 15 when not specified

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Prioritize Instructions

The Prioritize Instructions contain four indicators: Byte or Word mode, Operand Source (R), Mask Source (S), and Destination. They are further subdivided into two types. The function performed by the Prioritize instruction is shown in Figure 9. The R operand is ANDed with the complement of the Mask operand. A ZERO in the Mask operand allows the corresponding bit in the R operand to participate in the priority encoding function. A ONE in the Mask operand forces the corresponding bit in the R operand to a ZERO, eliminating it from participation in the priority encoding function.

The Priority Encoder accepts a 16-bit input and produces a 5-bit binary-weighted code indicating the bit position of the highest-priority active bit. If none of the inputs are active, the output is ZERO. In the Word mode, if input bit 15 is active, the output is 1, etc. Figure 10 lists the output as a function of the highest-priority active-bit position in both the Word and Byte mode. The N and Z bits are affected and the OVR and C bits of the Status Register are forced to ZERO. The only limitation in this instruction is that the operand and the mask must be different sources.

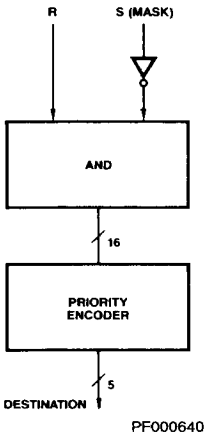

Figure 9. Prioritize Function

WORD MODE		BYTE MODE*	
Highest Priority Active Bit	**Encoder Output**	**Highest Priority Active Bit**	**Encoder Output**
None	0	None	0
15	1	7	1
14	2	6	2
.	.	.	.
.	.	.	.
1	15	1	7
0	16	0	8

*Bits 8 through 15 do not participate

Figure 10. Encoder Output

PRIORITIZE FIELD DEFINITIONS:

15	14	13	12	9	8	5	4	0
B/W	Quad		Destination		Source (R)		RAM Address/ Mask (S)	
B/W	Quad		Mask (S)		Destination		RAM Address/ Source (R)	
B/W	Quad		Mask (S)		Source (R)		RAM Address/ Destination	
B/W	Quad		Mask (S)		Source (R)		Destination	

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PRIORITIZE INSTRUCTION

Instruction	B/W	Quad	Destination			Source (R)			RAM Address/Mask (S)		
PRT1	0 = B 1 = W	10	1000 1010 1011	PRIA PR1Y PR1R	ACC Y-Bus RAM	0111 1001	RPT1A PR1D	ACC D	00000 .. 11111	R00 .. R31	RAM Reg 00 .... RAM Reg 31
Instruction	**B/W**	**Quad**	**Mask (S)**			**Destination**			**RAM Address/Source (R)**		
PRT2	0 = B 1 = W	10	1000 1010 1011	PRA PRZ PRI	Acc 0 I	0000 0010	PR2A PR2Y	ACC Y-Bus	00000 .. 11111	R00 .. R31	RAM Reg 00 .... RAM Reg 31
Instruction	**B/W**	**Quad**	**Mask (S)**			**Source (R)**			**RAM Address/Dest**		
PRT3	0 = B 1 = W	10	1000 1010 1011	PRA PRZ PRI	ACC 0 I	0011 0100 0110	PR3R PR3A PR3D	RAM ACC D	00000 .. 11111	R00 .. R31	RAM Reg 00 .... RAM Reg 31
Instruction	**B/W**	**Quad**	**Mask (S)**			**Source (R)**			**Destination**		
PRTNR	0 = B 1 = W	11	1000 1010 1011	PRA PRZ PRI	ACC 0 I	0100 0110	PRTA PRTD	ACC D	00000 00001	NRY NRA	Y-Bus ACC

Y-BUS AND STATUS — PRIORITIZE INSTRUCTIONS

Instruction	Opcode	B/W	Y-Bus	Flag3	Flag2	Flag1	LINK	OVR	N	C	Z
PRT1 PRT2		1 = W	$Y_i \leftarrow$ CODE ($SCR_n \cdot \overline{mask_n}$); $Y_m \leftarrow 0$; i = 0 to 4 and n = 0 to 15 m = 5 to 15	NC	NC	NC	NC	0	U	0	U
PRT3 PRTNR		0 = B	$Y_i \leftarrow$ CODE ($SCR_n \cdot \overline{mask_n}$); $Y_m \leftarrow 0$; i = 0 to 3 and n = 0 to 7 m = 4 to 15	NC	NC	NC	NC	0	U	0	U

SRC = Source
U = Update
NC = No Change
0 = Reset
1 = Set
i = 0 to 15 when not specified

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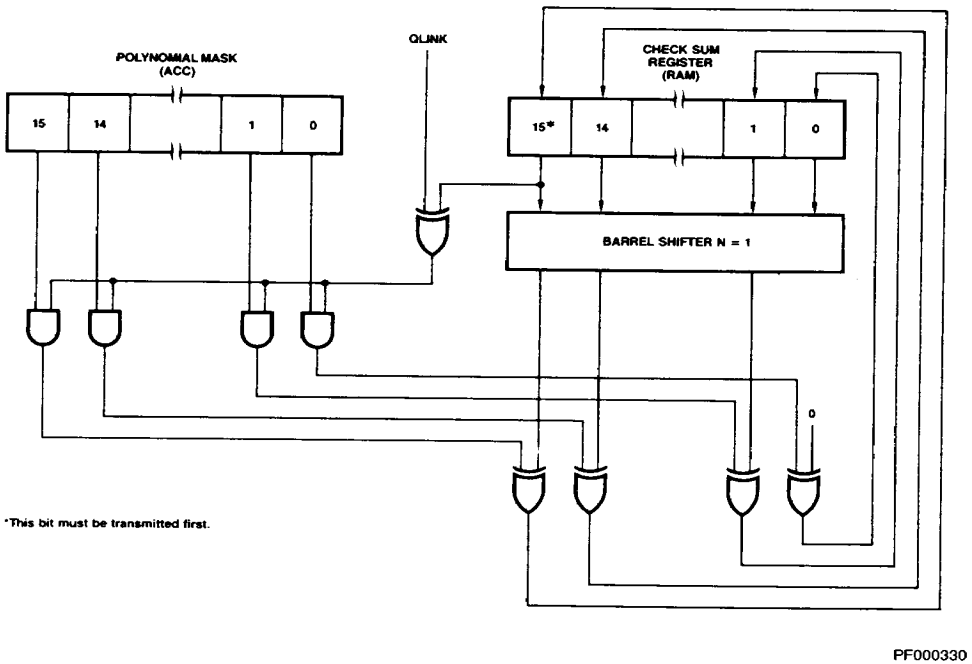
Cyclic-Redundancy-Check Instructions

The Cyclic-Redundancy-Check (CRC) Instructions contain one indicator: Address of a RAM register to use as the check sum register. The CRC Instruction provides a method for generation of the check bits in a CRC calculation. Two CRC Instructions are provided – CRC Forward and CRC Reverse. The reason for providing two instructions is that CRC standards do not specify which data bit is to be transmitted first, the LSB or the MSB, but they do specify which check bit must be transmitted first. Figure 11 illustrates the method used to generate these check bits for the CRC Forward function, and Figure 12 illustrates the method used for the CRC Reverse function. The ACC serves as a polynomial mask to define the generating polynomial while the RAM register holds the partial result and eventually the calculated check sum. The LINK-bit is used as the serial input. The serial input combines with the MSB of the check-sum register, according to the polynomial defined by the polynomial mask register. When the last input bit has been processed, the check-sum register contains the CRC check bits. The LINK, N, and Z bits are affected and the OVR and C bits of the Status Register are forced to ZERO.

CYCLIC-REDUNDANCY-CHECK FIELD DEFINITIONS:

	15	14	13	12	9	8	5	4	0
CRCF	1	Quad		0110		0011		RAM Address	
CRCR	1	Quad		0110		1001		RAM Address	



PF000330

Figure 11. CRC Forward Function

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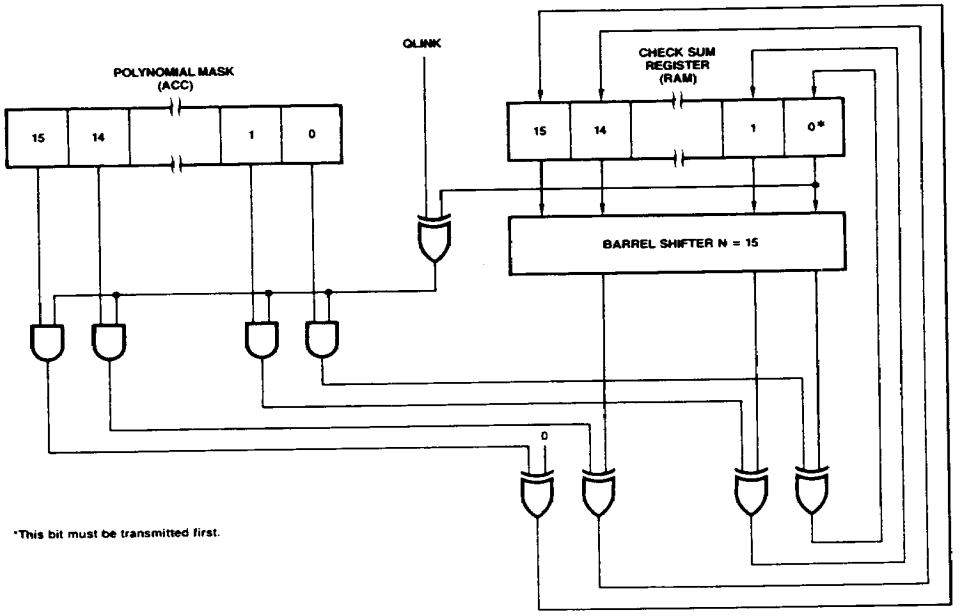

PF000320

Figure 12. CRC Reverse Function

CYCLIC-REDUNDANCY-CHECK INSTRUCTIONS

Instruction	B/W	Quad			RAM Address		
CRCF	1	10	0110	0011	00000 .. 11111	R00 .. R31	RAM Reg 00 .... RAM Reg 31
Instruction	**B/W**	**Quad**			**RAM Address**		
CRCR	1	10	0110	1001	00000 .. 11111	R00 .. R31	RAM Reg 00 .... RAM Reg 31

Y-BUS AND STATUS — CYCLIC-REDUNDANCY-CHECK INSTRUCTIONS

Instruction	Opcode	B/W	Y-Bus	Flag3	Flag2	Flag1	LINK	OVR	N	C	Z
CRCF		1 = W	$Y_i \leftarrow [(QLINK \oplus RAM_{15}) \cdot ACC_i] \oplus RAM_{i-1}$ for i = 15 to 1 $Y_0 \leftarrow [(QLINK \oplus RAM_{15}) \cdot ACC_0] \oplus 0$	NC	NC	NC	RAM_{15}*	0	U	0	U
CRCR		1 = W	$Y_i \leftarrow [(QLINK \oplus RAM_0) \cdot ACC_i] \oplus RAM_{i+1}$ for i = 14 to 0 $Y_{15} \leftarrow [(QLINK \oplus RAM_0) \cdot ACC_{15}] \oplus 0$	NC	NC	NC	RAM_0*	0	U	0	U

*QLINK is loaded with the shifted out bit from the check-sum register.

U = Update
NC = No Change
0 = Reset
1 = Set
i = 0 to 15 when not specified

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Status Instructions

The Set Status Instruction contains a single indicator. This indicator specifies which bit or group of bits, contained in the Status Register (Figure 13), are to be set (forced to a ONE).

7	6	5	4	3	2	1	0
Flag3	Flag2	Flag1	LINK	OVR	N	C	Z

MPR-775

Figure 13. Status Byte

The Reset Status Instruction contains a single indicator. This indicator specifies which bit or group of bits, contained in the Status Register, are to be reset (forced to ZERO).

The Store Status Instruction contains two indicators; Byte/Word and a second indicator that specifies the destination of the Status Register. The Store Status Instruction allows the status of the processor to be saved and restored later, which is an especially useful function for interrupt handling.

The Status Register is always stored in the lower byte of the RAM or the ACC register. Depending upon byte or word mode, the upper byte is unchanged or loaded with all ZEROs, respectively.

The Load Status instructions are included in the single operand and two operand instruction types.

The Test Status Instructions contain a single indicator which specifies which one of the 12 possible test conditions are to be placed on the Conditional-Test (CT) output. Besides the eight bits in the Status Register (QZ, QC, QN, QOVR, QLINK, QFlag1, QFlag2, and QFlag3), four logical functions (QN ⊕ QOVR, (QN ⊕ QOVR) + QZ, QZ + $\overline{QC}$, and LOW may also be selected. These functions are useful in testing results of Two's Complement and unsigned number arithmetic operations. The Status Register may also be tested via the bidirectional T-Bus. The code to test the Status Register via T-Bus is similar to the code used by instruction lines I_1 to I_4 as shown below. Instruction lines I_{0-4} have priority over T-Bus for testing the Status Register on CT output. See the discussion on the Status Register for a full description.

T_4 I_4	T_3 I_3	T_2 I_2	T_1 I_1	CT
0	0	0	0	(N ⊕ OVR) + Z
0	0	0	1	N ⊕ OVR
0	0	1	0	Z
0	0	1	1	OVR
0	1	0	0	LOW
0	1	0	1	C
0	1	1	0	Z + $\overline{C}$
0	1	1	1	N
1	0	0	0	LINK
1	0	0	1	Flag1
1	0	1	0	Flag2
1	0	1	1	Flag3

STATUS FIELD DEFINITIONS:

	15	14 13	12 9	8 5	4 0
SETST	0	Quad	1011	1010	Opcode
RSTST	0	Quad	1010	1010	Opcode
SVSTR	B/W	Quad	0111	1010	RAM Address/Dest
SVSTNR	B/W	Quad	0111	1010	Destination

STATUS INSTRUCTIONS

Instruction	B/W	Quad			Opcode		
SETST	0	11	1011	1010	00011 00101 00110 01001 01010	SONCZ SL SF1 SF2 SF3	Set OVR, N, C, Z Set LINK Set Flag1 Set Flag2 Set Flag3
Instruction	**B/W**	**Quad**			**Opcode**		
RSTST	0	11	1010	1010	00011 00101 00110 01001 01010	RONCZ RL RF1 RF2 RF3	Reset OVR, N, C, Z Reset LINK Reset Flag1 Reset Flag2 Reset Flag3
Instruction	**B/W**	**Quad**			**RAM Address/Dest**		
SVSTR	0 = B 1 = W	10	0111	1010	00000 .. 11111	R00 .. R31	RAM Reg 00 .... RAM Reg 31
Instruction	**B/W**	**Quad**			**Destination**		
SVSTNR	0 = B 1 = W	11	0111	1010	00000 00001	NRY NRA	Y-Bus ACC

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STATUS INSTRUCTIONS (Cont'd.)

Instruction	B/W	Quad			Opcode (CT)		
Test	0	11	1001	1010	00000	TNOZ	Test (N⊕OVR) + Z
					00010	TNO	Test N⊕OVR
					00100	TZ	Test Z
					00110	TOVR	Test OVR
					01000	TLOW	Test LOW
					01010	TC	Test C
					01100	TZC	Test Z + $\overline{C}$
					01110	TN	Test N
					10000	TL	Test LINK
					10010	TF1	Test Flag1
					10100	TF2	Test Flag2
					10110	TF3	Test Flag3

Y-BUS AND STATUS — STATUS INSTRUCTIONS

Instruction	Opcode	Description	B/W	Y-Bus	Flag3	Flag2	Flag1	LINK	OVR	N	C	Z
SETST	SONCZ	Set OVR, N, C, Z	0 = B	$Y_i \leftarrow 1$ for i = 0 to 15	NC	NC	NC	NC	1	1	1	1
	SL	Set LINK			NC	NC	NC	1	NC	NC	NC	NC
	SF1	Set Flag1			NC	NC	1	NC	NC	NC	NC	NC
	SF2	Set Flag2			NC	1	NC	NC	NC	NC	NC	NC
	SF3	Set Flag3			1	NC	NC	NC	NC	NC	NC	NC
RSTST	RONCZ	Reset OVR, N, C, Z	0 = B	$Y_i \leftarrow 0$ for i = 0 to 15	NC	NC	NC	NC	0	0	0	0
	RL	Reset LINK			NC	NC	NC	0	NC	NC	NC	NC
	RF1	Reset Flag1			NC	NC	0	NC	NC	NC	NC	NC
	RF2	Reset Flag2			NC	0	NC	NC	NC	NC	NC	NC
	RF3	Reset Flag3			0	NC	NC	NC	NC	NC	NC	NC
SVSTR SVSTNR		Save Status*	0 = B 1 = W	$Y_i \leftarrow$ Status for i = 0 to 7; $Y_i \leftarrow 0$ for i = 8 to 15	NC	NC	NC	NC	NC	NC	NC	NC
Test	TNOZ	Test (N⊕OVR) + Z	0 = B	**	NC	NC	NC	NC	NC	NC	NC	NC
	TNO	Test N⊕OVR			NC	NC	NC	NC	NC	NC	NC	NC
	TZ	Test Z			NC	NC	NC	NC	NC	NC	NC	NC
	TOVR	Test OVR			NC	NC	NC	NC	NC	NC	NC	NC
	TLOW	Test LOW			NC	NC	NC	NC	NC	NC	NC	NC
	TC	Test C			NC	NC	NC	NC	NC	NC	NC	NC
	TZC	Test Z + $\overline{C}$			NC	NC	NC	NC	NC	NC	NC	NC
	TN	Test N			NC	NC	NC	NC	NC	NC	NC	NC
	TL	Test LINK			NC	NC	NC	NC	NC	NC	NC	NC
	TF1	Test Flag1			NC	NC	NC	NC	NC	NC	NC	NC
	TF2	Test Flag2			NC	NC	NC	NC	NC	NC	NC	NC
	TF3	Test Flag3			NC	NC	NC	NC	NC	NC	NC	NC

U = Update
NC = No Change
0 = Reset
1 = Set
i = 0 to 15 when not specified

*In Byte mode only, the lower byte from the Y-Bus is loaded into the RAM or ACC, and in Word mode, all 16 bits from the Y-Bus are loaded into the RAM or ACC.

**Y-Bus is Undefined.

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No-Operation (NO-OP) Instruction

The NO-OP Instruction has a fixed 16-bit code. This instruction does not change any internal registers in the Am29C117. It preserves the Status Register, RAM register, and the ACC register.

NO-OP FIELD DEFINITION:

	15	14 13	12 9	8 5	4 0
NO-OP	0	11	1000	1010	00000

NO-OP INSTRUCTION

Instruction	B/W	Quad			
NO-OP	0	11	1000	1010	00000

Y-BUS AND STATUS — NO-OP INSTRUCTION

Instruction	Opcode	B/W	Y-Bus	Flag3	Flag2	Flag1	LINK	OVR	N	C	Z
NO-OP		0 = B	*	NC	NC	NC	NC	NC	NC	NC	NC

SRC = Source
U = Update
NC = No Change
0 = Reset
1 = Set
i = 0 to 15 when not specified
*Y-Bus is undefined.

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SUMMARY OF MNEMONICS

INSTRUCTION TYPE

SOR	Single Operand RAM
SONR	Single Operand Non-RAM
TOR1	Two Operand RAM (Quad 0)
TOR2	Two Operand RAM (Quad 2)
TONR	Two Operand Non-RAM
SHFTR	Single Bit Shift RAM
SHFTNR	Single Bit Shift Non-RAM
ROTR1	Rotate n Bits RAM (Quad 0)
ROTR2	Rotate n Bits RAM (Quad 1)
ROTNR	Rotate n Bits Non-RAM
BOR1	Bit Oriented RAM (Quad 3)
BOR2	Bit Oriented RAM (Quad 2)
BONR	Bit Oriented Non-RAM
ROTM	Rotate and Merge
ROTC	Rotate and Compare
PRT1	Prioritize RAM; Type 1
PRT2	Prioritize RAM; Type 2
PRT3	Prioritize RAM; Type 3
PRTNR	Prioritize Non-RAM
CRCF	Cyclic-Redundancy-Check Forward
CRCR	Cyclic-Redundancy-Check Reverse
NOOP	No Operation
SETST	Set Status
RSTST	Reset Status
SVSTR	Save Status RAM
SVSTNR	Save Status Non-RAM
TEST	Test Status

SOURCE AND DESTINATION

Single Operand:

SORA	Single Operand RAM to ACC
SORY	Single Operand RAM to Y-Bus
SORS	Single Operand RAM to Status
SOAR	Single Operand ACC to RAM
SODR	Single Operand D to RAM
SOIR	Single Operand I to RAM
SOZR	Single Operand 0 to RAM
SOZER	Single Operand D(0E) to RAM
SOSER	Single Operand D(SE) to RAM
SORR	Single Operand RAM to RAM
SOA	Single Operand ACC
SOD	Single Operand D
SOI	Single Operand I
SOZ	Single Operand 0
SOZE	Single Operand D(0E)
SOSE	Single Operand D(SE)
NRY	Non-RAM Y-Bus
NRA	Non-RAM ACC
NRS	Non-RAM Status
NRAS	Non-RAM ACC, Status

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Two Operand:

TORAA	Two Operand RAM, ACC to ACC
TORIA	Two Operand RAM, I to ACC
TODRA	Two Operand D, RAM to ACC
TORAY	Two Operand RAM, ACC to Y-Bus
TORIY	Two Operand RAM, I to Y-Bus
TODRY	Two Operand D, RAM to Y-Bus
TORAR	Two Operand RAM, ACC to RAM
TORIR	Two Operand RAM, I to RAM
TODRR	Two Operand D, RAM to RAM
TODAR	Two Operand D, ACC to RAM
TOAIR	Two Operand ACC, I to RAM
TODIR	Two Operand D, I to RAM
TODA	Two Operand D, ACC
TOAI	Two Operand ACC, I
TODI	Two Operand D, I

Single Bit Shift:

SHRR	Shift RAM, Store in RAM
SHDR	Shift D, Store in RAM
SHA	Shift ACC
SHD	Shift D

Rotate By n Bits:

RTRA	Rotate RAM, Store in ACC
RTRY	Rotate RAM, Place on Y-Bus
RTRR	Rotate RAM, Store in RAM
RTAR	Rotate ACC, Store in RAM
RTDR	Rotate D, Store in RAM
RTDY	Rotate D, Place on Y-Bus
RTDA	Rotate D, Store in ACC
RTAY	Rotate ACC, Place on Y-Bus
RTAA	Rotate ACC, Store in ACC

Rotate and Merge:

MDAI	Merge Disjoint Bits of D and ACC Using I as Mask and Store in ACC
MDAR	Merge Disjoint Bits of D and ACC Using RAM as Mask and Store in ACC
MDRI	Merge Disjoint Bits of D and RAM Using I as Mask and Store in RAM
MDRA	Merge Disjoint Bits of D and RAM Using ACC as Mask and Store in RAM
MARI	Merge Disjoint Bits of ACC and RAM Using I as Mask and Store in RAM
MRAI	Merge Disjoint Bits of RAM and ACC Using I as Mask and Store in ACC

Rotate and Compare:

CDAI	Compare Unmasked Bits of D and ACC Using I as Mask

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CDRI	Compare Unmasked Bits of D and RAM Using I as Mask
CDRA	Compare Unmasked Bits of D and RAM Using ACC as Mask
CRAI	Compare Unmasked Bits of RAM and ACC Using I as Mask

Prioritize:

PR1A	ACC as Destination for Prioritize Type 1
PR1Y	Y-Bus as Destination for Prioritize Type 1
PR1R	RAM as Destination for Prioritize Type 1
PRT1A	ACC as Source for Prioritize Type 1
PR1D	D as Source for Prioritize Type 1
PR2A	ACC as Destination for Prioritize Type 2
PR2Y	Y-Bus as Destination for Prioritize Type 2
PR3R	RAM as Source for Prioritize Type 3
PR3A	ACC as Source for Prioritize Type 3
PR3D	D as Source for Prioritize Type 3
PRTA	ACC as source for Prioritize Type Non-RAM
PRTD	D as Source for Prioritize Type Non-RAM
PRA	ACC as Mask for Prioritize Type 2, 3, and Non-RAM
PRZ	Mask Equal to Zero for Prioritize Type 2, 3, and Non-RAM
PRI	I as Mask for Prioritize Type 2, 3, and Non-RAM

OPCODE

Addition:

ADD	Add without Carry
ADDC	Add with Carry
A2NA	Add 2^n to ACC
A2NR	Add 2^n to RAM
A2NDY	Add 2^n to D, Place on Y-Bus

Subtraction:

SUBR	Subtract R from S without Carry
SUBRC	Subtract R from S with Carry
SUBS	Subtract S from R without Carry
SUBSC	Subtract S from R with Carry
S2NR	Subtract 2^n from RAM
S2NA	Subtract 2^n from ACC
S2NDY	Subtract 2^n from D, Place on Y-Bus

Logical Operations:

AND	Boolean AND
NAND	Boolean NAND
EXOR	Boolean EXOR
NOR	Boolean NOR
OR	Boolean OR
EXNOR	Boolean EXNOR

SHIFTS

SHUPZ	Shift Up Towards MSB with 0 Insert
SHUP1	Shift Up Towards MSB with 1 Insert
SHUPL	Shift Up Towards MSB with LINK Insert
SHDNZ	Shift Down Towards LSB with 0 Insert
SHDN1	Shift Down Towards LSB with 1 Insert
SHDNL	Shift Down Towards LSB with LINK Insert
SHDNC	Shift Down Towards LSB with Carry Insert
SHDNOV	Shift Down Towards LSB with Sign EXOR Overflow Insert

Loads:

LD2NR	Load 2^n into RAM
LDC2NR	Load $\overline{2^n}$ into RAM
LD2NA	Load 2^n into ACC
LDC2NA	Load $\overline{2^n}$ into ACC
LD2NY	Place 2^n on Y-Bus
LDC2NY	Place $\overline{2^n}$ on Y-Bus

Bit Oriented:

SETNR	Set RAM, Bit n
SETNA	Set ACC, Bit n
SETND	Set D, Bit n
SONCZ	Set OVR, N, C, Z, in Status Register
SL	Set LINK Bit in Status Register
SF1	Set Flag1 Bit in Status Register
SF2	Set Flag2 Bit in Status Register
SF3	Set Flag3 Bit in Status Register
RSTNR	Reset RAM, Bit n
RSTNA	Reset ACC, Bit n
RSTND	Reset D, Bit n
RONCZ	Reset OVR, N, C, Z, in Status Register
RL	Reset LINK Bit in Status Register
RF1	Reset Flag1 Bit in Status Register
RF2	Reset Flag2 Bit in Status Register
RF3	Reset Flag3 Bit in Status Register
TSTNR	Test RAM, Bit n
TSTNA	Test ACC, Bit n
TSTND	Test D, Bit n

Arithmetic Operations:

MOVE	Move and Update Status
COMP	Complement (1's Complement)
INC	Increment
NEG	Two's Complement

Conditional Test:

TNOZ	Test (N $\oplus$ OVR) + Z
TNO	Test N $\oplus$ OVR
TZ	Test Zero Bit
TOVR	Test Overflow Bit
TLOW	Test for LOW
TC	Test Carry Bit
TZC	Test Z + $\overline{C}$
TN	Test Negative Bit
TL	Test LINK Bit
TF1	Test Flag1 Bit
TF2	Test Flag2 Bit
TF3	Test Flag3 Bit

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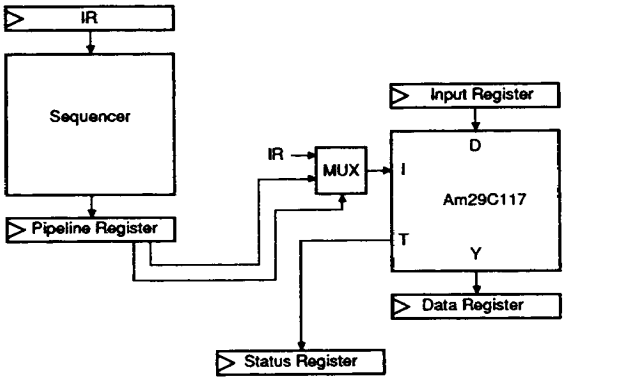
APPLICATIONS



BD008220

Figure 13. System Block Diagram

DATA PATH TIMING ANALYSIS

I. Without any External Logic

		29C117	29C117-1	29C117-2
Pipeline Register	CP-Q	9	9	9
RALU (29C117)	**I-T**	**105**	**60**	**49**
Status Register	D-CP	4	4	4
	Total:	**118**	**73**	**62**
Pipeline Register	CP-Q	9	9	9
RALU (29C117)	**I-Y**	**98**	**60**	**49**
Data Register	D-CP	4	4	4
	Total:	**111**	**73**	**62**
Input Register	CP-Q	9	9	9
RALU (29C117)	**D-Y**	**78**	**49**	**40**
Data Register	D-CP	4	4	4
	Total:	**91**	**62**	**53**

II. With Multiplexers for Two Address

		29C117	29C117-1	29C117-2
Pipeline Register	CP-Q	9	9	9
Multiplexer	Sel-Y	5	5	5
RALU (29C117)	**I-T**	**105**	**60**	**49**
Status Register	D-CP	4	4	4
	Total:	**123**	**78**	**67**
Pipeline Register	CP-Q	9	9	9
Multiplexer	Sel-Y	5	5	5
RALU (29C117)	**I-Y**	**98**	**60**	**49**
Data Register	D-CP	4	4	4
	Total:	**116**	**78**	**67**

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ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
(Case) Temperature Under Bias ..... −55 to +125°C
Supply Voltage to
Ground Potential Continuous ..... −0.3 to +7.0 V
DC Voltage Applied to Outputs For
High Output State ..... −0.3 to +V_{CC} +0.3 V
DC Input Voltage ..... −0.3 to +V_{CC} +0.3 V
DC Output Current, Into LOW Outputs ..... 30 mA
DC Input Current ..... −10 to +10 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Ambient Temperature (T_A) ..... 0 to +70°C
Supply Voltage (V_{CC}) ..... +4.5 to +5.5 V

Military* (M) Devices
Ambient Temperature (T_A) ..... −55 to +125°C
Supply Voltage (V_{CC}) ..... +4.5 to +5.5 V

*Military Products 100% tested at T_A = +25°C, +125°C, and −55°C

Operating ranges define those limits between which the functionality of the device is guaranteed.

Thermal Resistance and I/O Capacitance (Typical)

Symbol	PL 068	CG 068	CL 068	Units
θ_{JA}	35	25	37	°C/W
C*	5	5	10	pF/Pin

*Tested on a sample basis only.

DC CHARACTERISTICS over operating range unless otherwise specified (for APL Products, Group A, Subgroups 1, 2, 3, are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions (Note 1)			Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}		COM'L I_{OH} = −1.6 mA	2.4		V
				MIL I_{OH} = −1.2 mA			
V_{OL}	Output LOW Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}		COM'L I_{OL} = 16 mA		0.5	V
				MIL I_{OL} = 12 mA			
V_{IH}	Guaranteed Input Logical HIGH Voltage (Note 2)				2.0		V
V_{IL}	Guaranteed Input Logical LOW Voltage (Note 2)					0.8	V
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = 0.5 V				−10	μA
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC} − 0.5 V				10	μA
I_{OZH}	Off-State (High Impedance) Output Current	V_{CC} = Max., V_O = 2.4 V				10	μA
I_{OZL}	Off-State (High Impedance) Output Current	V_{CC} = Max., V_O = 0.5 V				−10	μA
I_{CC}	Static Power Supply Current (Note 3)	V_{CC} = Max. (Note 4) I_O = 0 μA	COM'L T_A = 0 to +70°C	CMOS V_{IN} = V_{CC} or GND		120	mA
				TTL V_{IN} = 0.5 or 2.4 V		170	
			MIL T_A = −55 to +125°C	CMOS V_{IN} = V_{CC} or GND		150	
				TTL V_{IN} = 0.5 or 2.4 V		200	
C_{PD}	Power Dissipation Capacitance (Note 4)	V_{CC} = 5.0 V, T_A = 25°C, No Load			850 pF Typical		

Notes:
1. V_{CC} conditions shown as Min. or Max. refer to the (±10%) V_{CC} limits.
2. These input levels provide zero-noise immunity and should only be statically tested in a noise-free environment (not functionally tested).
3. Worst-case I_{CC} is measured at the lowest temperature in the specified operating range.
4. Use CMOS I_{CC} when the device is driven by CMOS circuits, and TTL I_{CC} when the device is driven by TTL circuits.
5. C_{PD} determines the no-load dynamic current consumption:
I_{CC} (Total) = I_{CC} (Static) + (C_{PD} + n C_L) $\frac{f}{2}$ where f is the clock frequency, C_L is the output load capacitance, and n is the number of loads.

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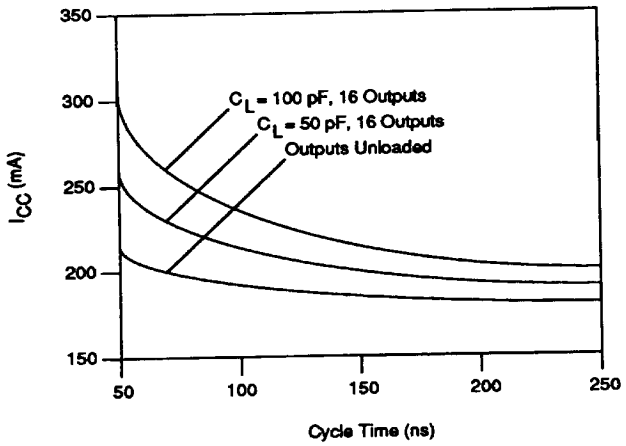
Am29C117 I_{CC} vs Cycle Time



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Note: Values are calculated as typical I_{CC} at V_{CC} = 5.5 V.

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SWITCHING CHARACTERISTICS over COMMERCIAL operating range

(T_A = 0 to +70°C, V_{CC} = 4.50 to 5.50 V, C_L = 50 pF)

Am29C117

A. Combinational Delays (nsec)

		Outputs		
		Y_{0-15}	T_{1-4}	CT
Input	I_{0-4} (ADDR)	98	105	–
	I_{0-15} (DATA)	98	105	–
	I_{0-15} (INSTR)	98	105	58
	DLE	73	75	–
	T_{1-4}	–	–	46
	CP	76	83	48
	D_{0-15}	78	80	–
	$\overline{IEN}$	–	–	53

B. Enable/Disable Times (nsec)

(C_L = 5 pF for disable only)

From Input	To Output	Enable		Disable	
		t_{PZH}	t_{PZL}	t_{PHZ}	t_{PLZ}
$\overline{OE}_Y$	Y_{0-15}	25	25	25	25
OE_T	T_{1-4}	25	25	25	25

C. Clock and Pulse Requirements (nsec)

Input	Min. LOW Time	Min. HIGH Time
CP	21	30
DLE	–	15
$\overline{IEN}$	22	–

D. Setup and Hold Times (nsec)

Input	With Respect to	HIGH-to-LOW Transition		LOW-to-HIGH Transition		Comment	
		Setup	Hold	Setup	Hold		
I_{0-4} (RAM ADDR)	CP	(t_{s1}) 24	(t_{h1}) 0	–	–	Single ADDR (Source)	
I_{0-4} (RAM ADDR)	CP and $\overline{IEN}$ both LOW	(t_{s2}) 10	–	–	(t_{h7}) 2	Two ADDR (Destination)	
I_{0-15} (DATA)	CP	–	–	(t_{s8}) 78	(t_{h8}) 0		
I_{0-15} (INSTR)	CP	(t_{s3}) 38 †	(t_{h3}) 17 †	(t_{s9}) 78	(t_{h9}) 2		
I_{0-15} (INSTR)	$\overline{IEN}$	(t_{s16}) 6	(t_{h16}) 18	–	–	Two ADDR (Immediate)	
$\overline{IEN}$ HIGH	CP	(t_{s4}) 10	–	–	(t_{h10}) 0	Disable	
$\overline{IEN}$ LOW	CP	– –	– –	(t_{s11}) 22 (t_{S5}) 20	(t_{h11}) 0 (t_{h5}) 0	Enable	Immediate first cycle
$\overline{SRE}$	CP	–	–	(t_{s12}) 17	(t_{h12}) 0		
D	CP	–	–	(t_{s13}) 53	(t_{h13}) 0		
D	DLE	(t_{s6}) 10	(t_{h6}) 6	–	–		
DLE	CP	–	–	(t_{s14}) 54	(t_{h14}) 0		

†Timing for immediate instruction for first cycle.

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SWITCHING CHARACTERISTICS over COMMERCIAL operating range (Cont'd.)

Am29C117-1

A. Combinational Delays (nsec)

Input	Outputs		
	Y_{0-15}	T_{1-4}	CT
I_{0-4} (ADDR)	60	60	–
I_{0-15} (DATA)	60	60	–
I_{0-15} (INSTR)	60	60	27
DLE	48	47	–
T_{1-4}	–	–	24
CP	53	57	31
D_{0-15}	49	46	–
$\overline{IEN}$	–	–	24

B. Enable/Disable Times (nsec)
(C_L = 5 pF for disable only)

From Input	To Output	Enable		Disable	
		t_{PZH}	t_{PZL}	t_{PHZ}	t_{PLZ}
$\overline{OE}_Y$	Y_{0-15}	21	21	21	21
OE_T	T_{1-4}	21	21	21	21

C. Clock and Pulse Requirements (nsec)

Input	Min. LOW Time	Min. HIGH Time
CP	21	15
DLE	–	15
$\overline{IEN}$	15	–

D. Setup and Hold Times (nsec)

Input	With Respect to	HIGH-to-LOW Transition		LOW-to-HIGH Transition		Comment	
		Setup	Hold	Setup	Hold		
I_{0-4} (RAM ADDR)	CP	(t_{s1}) 11	(t_{h1}) 0	–	–	Single ADDR (Source)	
I_{0-4} (RAM ADDR)	CP and $\overline{IEN}$ both LOW	(t_{s2}) 2	–	–	(t_{h7}) 0	Two ADDR (Destination)	
I_{0-15} (DATA)	CP	–	–	(t_{s8}) 69	(t_{h8}) 0		
I_{0-15} (INSTR)	CP	(t_{s3}) 19 †	(t_{h3}) 12 †	(t_{s9}) 69	(t_{h9}) 0		
I_{0-15} (INSTR)	$\overline{IEN}$	(t_{s16}) 6	(t_{h16}) 18	–	–	Two ADDR (Immediate)	
$\overline{IEN}$ HIGH	CP	(t_{s4}) 5	–	–	(t_{h10}) 0	Disable	
$\overline{IEN}$ LOW	CP	– –	– –	(t_{s11}) 12 (t_{S5}) 6	(t_{h11}) 0 (t_{h5}) 0	Enable	Immediate first cycle
$\overline{SRE}$	CP	–	–	(t_{s12}) 11	(t_{h12}) 0		
D	CP	–	–	(t_{s13}) 39	(t_{h13}) 0		
D	DLE	(t_{s6}) 5	(t_{h6}) 3	–	–		
DLE	CP	–	–	(t_{s14}) 42	(t_{h14}) 0		

†Timing for immediate instruction for first cycle.

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SWITCHING CHARACTERISTICS over COMMERCIAL operating range (Cont'd.)

Am29C117-2

A. Combinational Delays (nsec)

Input	Outputs		
	Y_{0-15}	T_{1-4}	CT
I_{0-4} (ADDR)	49	49	–
I_{0-15} (DATA)	49	49	–
I_{0-15} (INSTR)	49	49	22
DLE	40	39	–
T_{1-4}	–	–	22
CP	45	45	26
D_{0-15}	40	38	–
$\overline{IEN}$	–	–	22

B. Enable/Disable Times (nsec)
(C_L = 5 pF for disable only)

From Input	To Output	Enable		Disable	
		t_{PZH}	t_{PZL}	t_{PHZ}	t_{PLZ}
$\overline{OE}_Y$	Y_{0-15}	19	19	19	19
OE_T	T_{1-4}	19	19	19	19

C. Clock and Pulse Requirements (nsec)

Input	Min. LOW Time	Min. HIGH Time
CP	20	15
DLE	–	15
$\overline{IEN}$	15	–

D. Setup and Hold Times (nsec)

Input	With Respect to	HIGH-to-LOW Transition		LOW-to-HIGH Transition		Comment	
		Setup	Hold	Setup	Hold		
I_{0-4} (RAM ADDR)	CP	(t_{s1}) 10	(t_{h1}) 0	–	–	Single ADDR (Source)	
I_{0-4} (RAM ADDR)	CP and $\overline{IEN}$ both LOW	(t_{s2}) 2	–	–	(t_{h7}) 0	Two ADDR (Destination)	
I_{0-15} (DATA)	CP	–	–	(t_{s8}) 61	(t_{h8}) 0		
I_{0-15} (INSTR)	CP	(t_{s3}) 17 †	(t_{h3}) 10 †	(t_{s9}) 61	(t_{h9}) 0		
I_{0-15} (INSTR)	$\overline{IEN}$	(t_{s16}) 6	(t_{h16}) 18	–	–	Two ADDR (Immediate)	
$\overline{IEN}$ HIGH	CP	(t_{s4}) 5	–	–	(t_{h10}) 0	Disable	
$\overline{IEN}$ LOW	CP	– –	– –	(t_{s11}) 11 (t_{S5}) 6	(t_{h11}) 0 (t_{h5}) 0	Enable	Immediate first cycle
$\overline{SRE}$	CP	–	–	(t_{s12}) 10	(t_{h12}) 0		
D	CP	–	–	(t_{s13}) 34	(t_{h13}) 0		
D	DLE	(t_{s6}) 5	(t_{h6}) 3	–	–		
DLE	CP	–	–	(t_{s14}) 36	(t_{h14}) 0		

†Timing for immediate instruction for first cycle.

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SWITCHING CHARACTERISTICS over **MILITARY** operating range (for APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted)

Am29C117-1

A. Combinational Delays (nsec)

Input	Outputs		
	Y_{0-15}	T_{1-4}	CT
I_{0-4} (ADDR)	65	64	–
I_{0-15} (DATA)	65	64	–
I_{0-15} (INSTR)	65	64	27
DLE	53	52	–
T_{1-4}	–	–	27
CP	58	61	34
D_{0-15}	53	50	–
$\overline{IEN}$	–	–	26

B. Enable/Disable Times (nsec)
(C_L = 5 pF for disable only)

From Input	To Output	Enable		Disable	
		t_{PZH}	t_{PZL}	t_{PHZ}	t_{PLZ}
$\overline{OE}_Y$	Y_{0-15}	22	22	22	22
OE_T	T_{1-4}	22	22	22	22

C. Clock and Pulse Requirements (nsec)

Input	Min. LOW Time	Min. HIGH Time
CP	22	15
DLE	–	15
$\overline{IEN}$	15	–

D. Setup and Hold Times (nsec)

Input	With Respect to	HIGH-to-LOW Transition		LOW-to-HIGH Transition		Comment	
		Setup	Hold	Setup	Hold		
I_{0-4} (RAM ADDR)	CP	(t_{s1}) 12	(t_{h1}) 1	–	–	Single ADDR (Source)	
I_{0-4} (RAM ADDR)	CP and $\overline{IEN}$ both LOW	(t_{s2}) 2	–	–	(t_{h7}) 0	Two ADDR (Destination)	
I_{0-15} (DATA)	CP	–	–	(t_{s8}) 72	(t_{h8}) 0		
I_{0-15} (INSTR)	CP	(t_{s3}) 21 †	(t_{h3}) 12 †	(t_{s9}) 72	(t_{h9}) 0		
I_{0-15} (INSTR)	$\overline{IEN}$	(t_{s16}) 6	(t_{h16}) 18	–	–	Two ADDR (Immediate)	
$\overline{IEN}$ HIGH	CP	(t_{s4}) 5	–	–	(t_{h10}) 0	Disable	
$\overline{IEN}$ LOW	CP	– –	– –	(t_{s11}) 13 (t_{S5}) 7	(t_{h11}) 0 (t_{h5}) 0	Enable	Immediate first cycle
$\overline{SRE}$	CP	–	–	(t_{s12}) 11	(t_{h12}) 1		
D	CP	–	–	(t_{s13}) 44	(t_{h13}) 0		
D	DLE	(t_{s6}) 6	(t_{h6}) 4	–	–		
DLE	CP	–	–	(t_{s14}) 47	(t_{h14}) 0		

†Timing for immediate instruction for first cycle.

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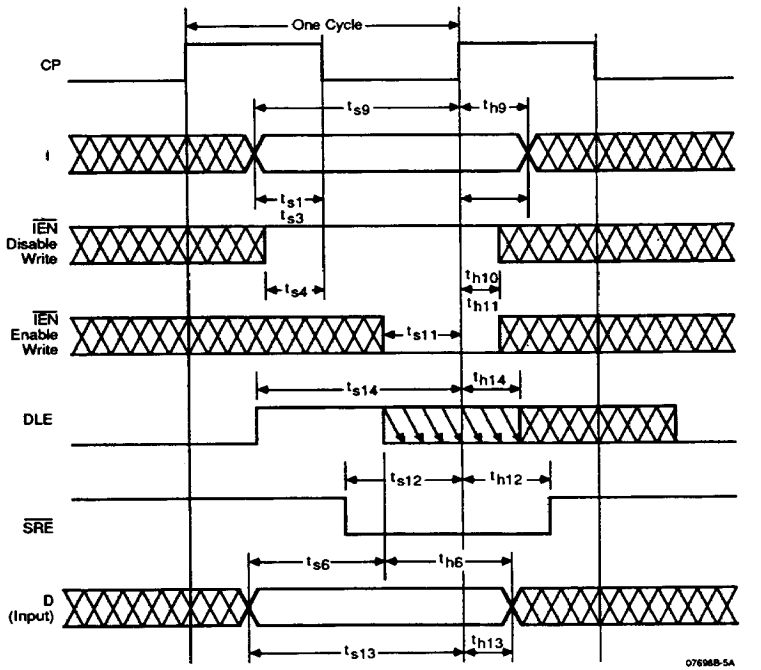
SWITCHING WAVEFORMS

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
———	MUST BE STEADY	WILL BE STEADY
▨	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
▨	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
▨	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN
⋈	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

KS000010



WF025870

Single-Address Access Timing

If t_{h6} is satisfied, t_{h13} need not be satisfied.

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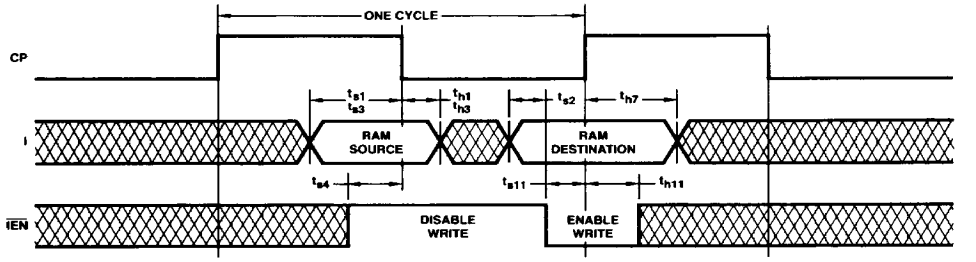
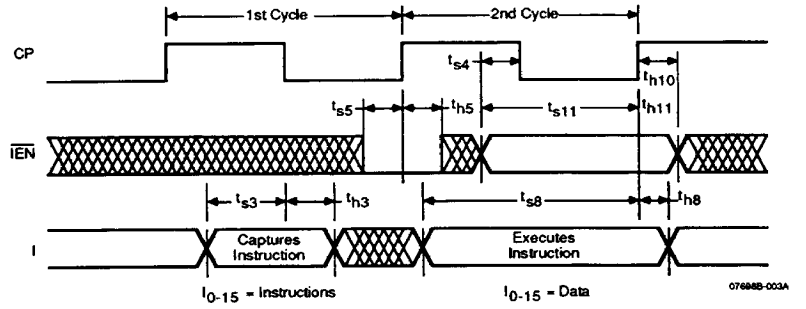
SWITCHING WAVEFORMS (Cont'd)



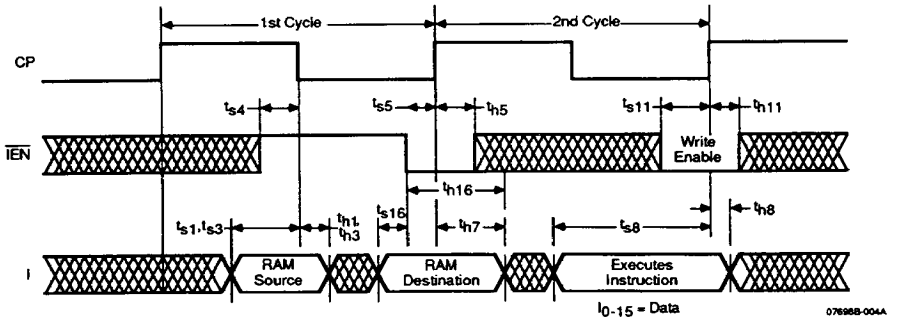
WF002546

Double-Address Access Timing



WF025900

One-Address Immediate Instruction Cycle Timing



WF025890

Two-Address Immediate Instruction Timing

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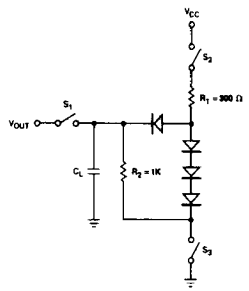
Test Philosophy and Methods

The following points give the general philosophy which we apply to tests that must be properly engineered if they are to be implemented in an automatic environment. The specifics of what philosophies applied to which test are shown in the data sheet.

1. Ensure the part is adequately decoupled at the test head. Large changes in V_{CC} current when the device switches may cause function failures due to V_{CC} changes.
2. Do not leave inputs floating during any tests, as they may start to oscillate at high frequency.
3. Do not attempt to perform threshold tests at high speed. Following an input transition, ground current may change by as much as 400 mA in 5–8 ns. Inductance in the ground cable may allow the ground pin at the device to rise by hundreds of millivolts momentarily.
4. Use extreme care in defining input levels for AC tests. Many inputs may be changed at once, so there will be significant noise at the device pins which may not actually reach V_{IL} or V_{IH} until the noise has settled. AMD recommends using $V_{IL} \leqslant 0$ V and $V_{IH} \geqslant 3.0$ V for AC tests.
5. To simplify failure analysis, programs should be designed to perform DC, Function, and AC tests as three distinct groups of tests.
6. Capacitive Loading for AC Testing
   Automatic testers and their associated hardware have stray capacitance that varies from one type of tester to another, but is generally around 50 pF. This makes it impossible to make direct measurements of parameters that call for a smaller capacitive load than the associated stray capacitance. Typical examples of this are the so-called "float delays," which measure the propagation delays into the high-impedance state and are usually specified at a load capacitance of 5.0 pF. In these cases, the test is peformed at the higher load capacitance (typically 50 pF), and engineering correlations based on data taken with a bench setup are used to predict the result at the lower capacitance.
   Similarly, a product may be specified at more than one capacitive load. Since the typical automatic tester is not capable of switching loads in mid-test, it is impossible to make measurements at <u>both</u> capacitances even though they may both be greater than the stray capacitance. In these cases, a measurement is made at one of the two capacitances. The result at the other capacitance is predicted from engineering correlations based on data taken with a bench setup and the knowledge that certain DC measurements (I_{OH}, I_{OL}, for example) have already been taken and are within specification. In some cases, special DC tests are performed in order to facilitate this correlation.
7. Threshold Testing
   the noise associated with automatic testing (due to the long, inductive cables) and the high gain of the tested device when in the vicinity of the actual device threshold, frequently give rise to oscillations when testing high-speed circuits. These oscillations are not indicative of a reject device, but instead, of an overtaxed test system. To minimize this problem, thresholds are tested at least once for <u>each</u> input pin. Thereafter, "hard" HIGH and LOW levels are used for other tests. Generally this means that function and AC testing are performed at "hard" input levels rather than at V_{IL} Max. and V_{IH} Min.
8. AC Testing
   Occasionally parameters are specified that cannot be measured directly on automatic testers because of tester limitations. Data input hold times often fall into this category. In these cases, the parameter in question is guaranteed by correlating these tests with other AC tests that have been performed. These correlations are arrived at by the cognizant engineer using data from precise bench measurements in conjunction with the knowledge that certain DC parameters have already been measured and are within specification.

   In some cases, certain AC tests are redundant since they can be shown to be predicted by other tests that have already been performed. In these cases, the redundant tests are not performed.

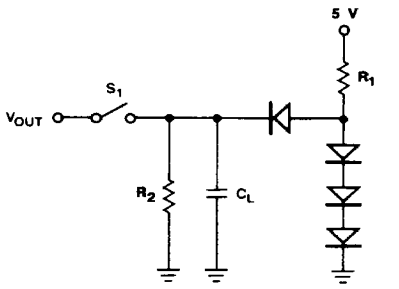
SWITCHING TEST CIRCUITS



TCR01331

A. Three-State Outputs

$R_1 = 300\ \Omega$



TCR01341

B. Normal Outputs

$R_1 = 300\ \Omega$
$R_2 = 3.0\ k\Omega$

Notes:
1. C_L = 50 pF includes scope probe, wiring and stray capacitances without device in test fixture.
2. S_1, S_2, S_3 are closed during function tests and all AC tests except output enable tests.
3. S_1 and S_3 are closed while S_2 is open for t_{PZH} test.
   S_1 and S_2 are closed while S_3 is open for t_{PZL} test.
4. C_L = 5.0 pF for output disable tests.

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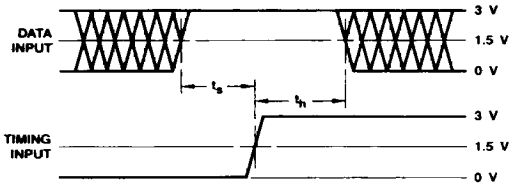
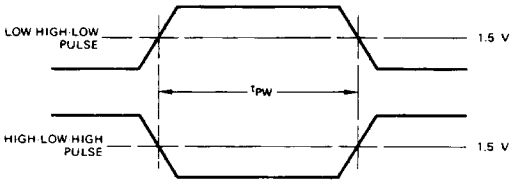
SWITCHING TEST WAVEFORMS



WFR02970

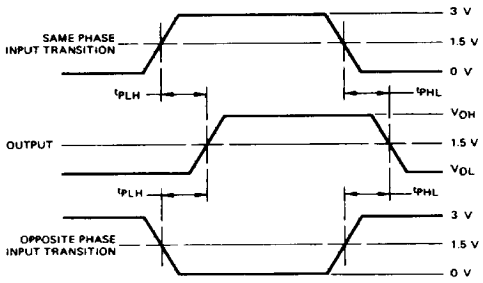
Notes: 1. Diagram shown for HIGH data only. Output transition may be opposite sense.
2. Cross hatched area is don't care condition.

A. Set-up, Hold, and Release Times



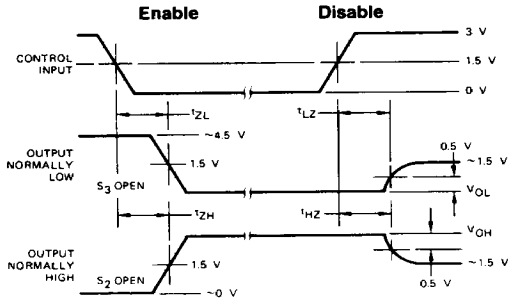
WFR02790

B. Pulse Width



WFR02980

C. Propagation Delay

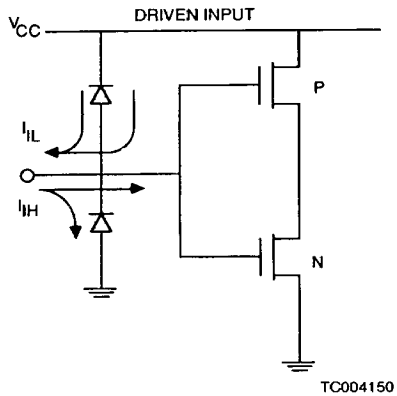


WFR02660

Notes: 1. Diagram shown for Input Control Enable-LOW and Input Control Disable-HIGH.
2. S_1, S_2 and S_3 of Load Circuit are closed except where shown.

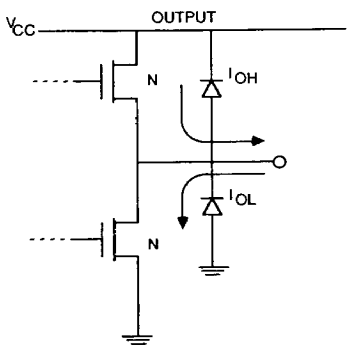
D. Enable and Disable Times

INPUT/OUTPUT CIRCUIT DIAGRAMS



TC004150

$C_I \approx 5.0$ pF, all inputs



TC004160

$C_O \approx 5.0$ pF, all outputs

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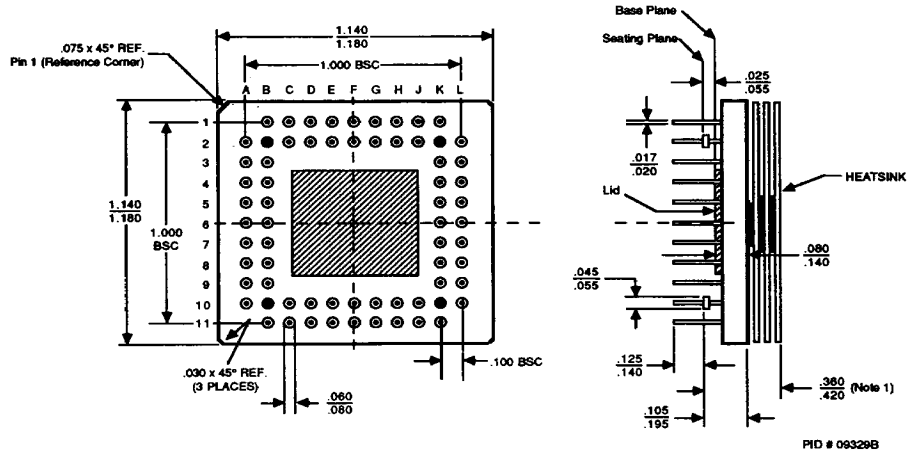
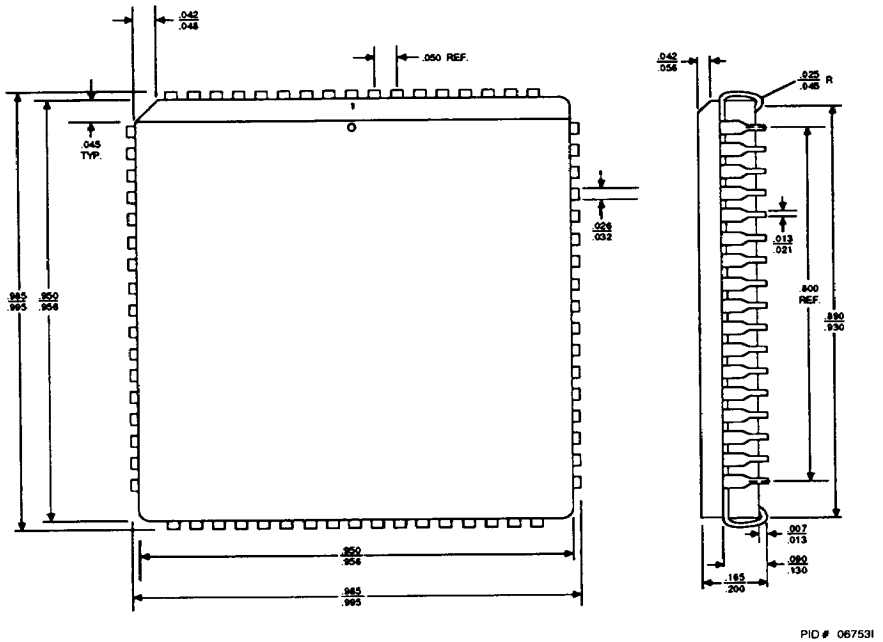
PHYSICAL DIMENSIONS*

CG 068



Note: 1. This dimension refers to a heatsink with only 3 fins. For heatsinks with more than 3 fins, the following dimensions apply: 4 fins = .450/.510
6 fins = .540/.600
7 fins = .690/.750

PL 068



*For reference only. All measurements are in inches. BSC is the ANSI standard for Basic Space Centering.

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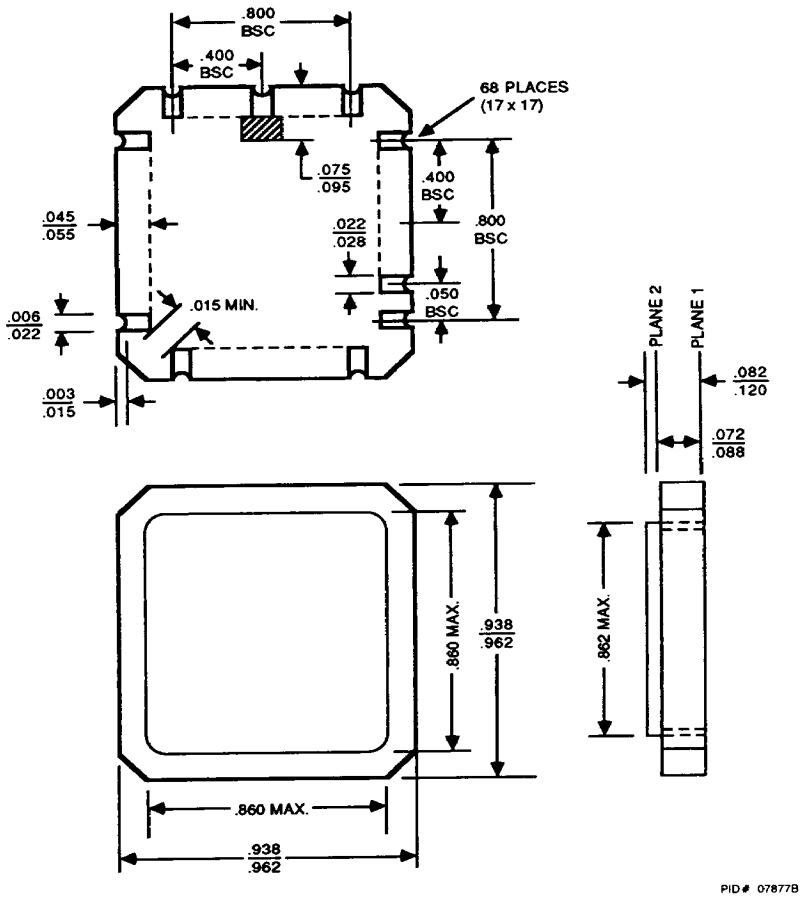
PHYSICAL DIMENSIONS (Cont'd.)

CL 068



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