

Am29C983/Am29C983A

9-Bit x 4-Port Multiple Bus Exchange



DISTINCTIVE CHARACTERISTICS

- Four bidirectional I/O ports with latches
 - Replaces several bidirectional latches and transceivers
 - Permits multiple bus communication
 - Allows two independent communication channels
 - TTL compatibility
- 9 bit-wide ports to handle byte parity
- Two selection inputs per port
 - Independent port interconnect control
 - Increased flexibility in data routing
- Matched port decoding
 - Simplifies external decode logic
 - Easily cascadable for wider buses
- Latches for incoming and outgoing data
 - Independent controls permit selective data capture
 - Ideal for stored operation
 - Readback feature for system diagnostics
- Glitch-free outputs during power-up/down
 - No power-up sequencing needed
 - Ideal for card-edge interface
- 48 mA output drive
 - High-capacitance bus driving
- High-performance CMOS
 - Low stand-by power consumption
- Two speeds available
Am29C983
 - 9 ns (typ) port-to-port delay
 - 10 ns (typ) select-to-port delayAm29C983A
 - 6 ns (typ) port-to-port delay
 - 7 ns (typ) select-to-port delay
- Available in 68-pin PLCC package and 80-pin PQFP package for commercial applications
- Available in 68-pin PGA package for military applications (Am29C983 only)

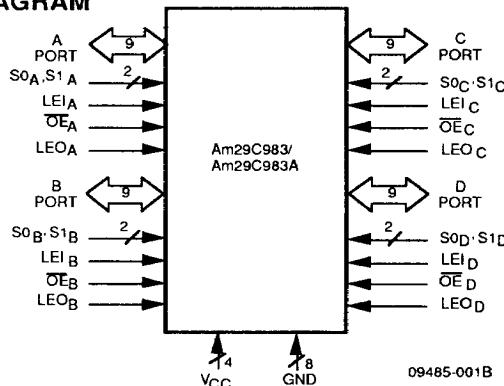
GENERAL DESCRIPTION

The Am29C983/A is a high-speed Multiple Bus Exchange device. It is organized as four 9-bit wide TTL-compatible I/O ports with Output Enable control for each port. Any port can serve either as a source (Input) port or as a destination (Output) port. When the output drivers of a port are disabled (high-impedance state), the port serves as a source port. When the drivers are enabled, the port serves as a destination port. Source port selection is made by two independent Select inputs at each port. This organization offers flexibility in implementing the Am29C983/A as a digital cross-point switch for multiple bus communication in a multiprocessing environment.

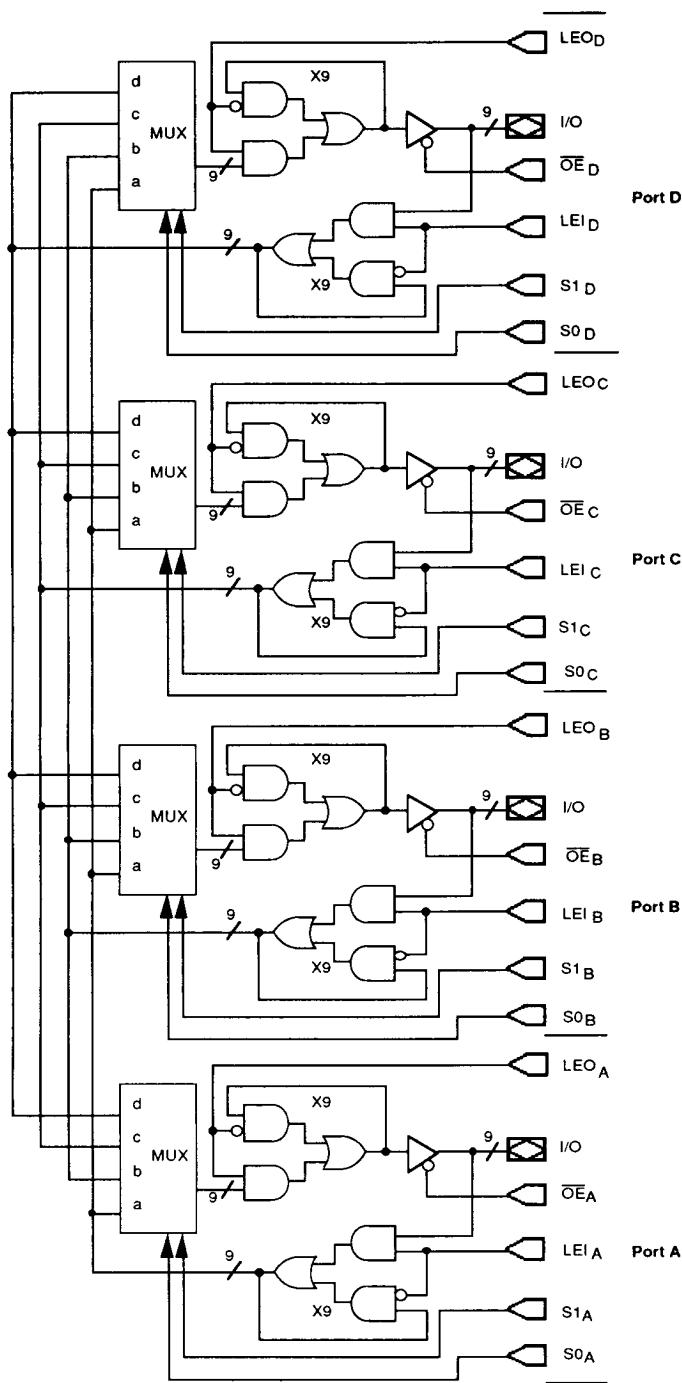
Each I/O port has an input latch to capture incoming data and an output latch to capture outgoing data. All input and output latches are independently controlled by active-HIGH Latch Enable inputs. This feature can be used to perform stored operation for byte-word compression and expansion to communicate between buses of different widths.

Independent port control permits cascading of Am29C983/As for wider buses. All I/O ports go into high-impedance state upon power-down. This feature makes the device ideally suited for card-edge applications.

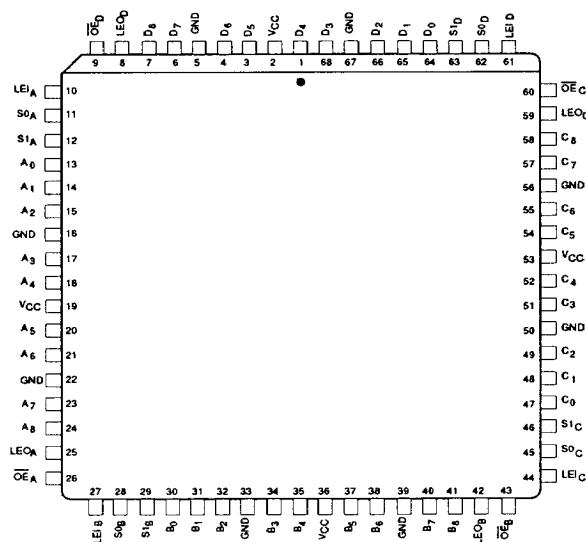
SIMPLIFIED BLOCK DIAGRAM



DETAILED BLOCK DIAGRAM

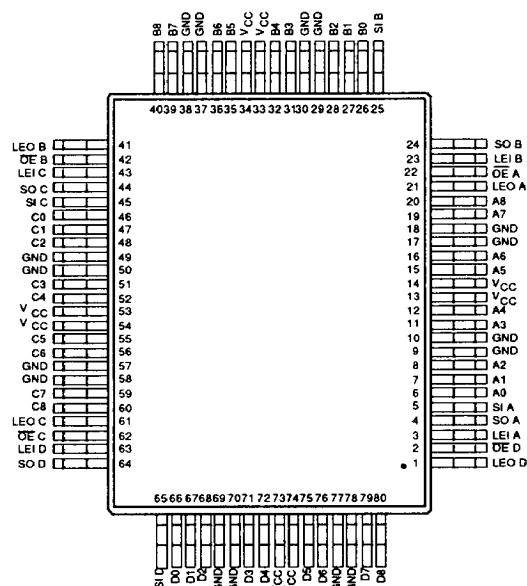


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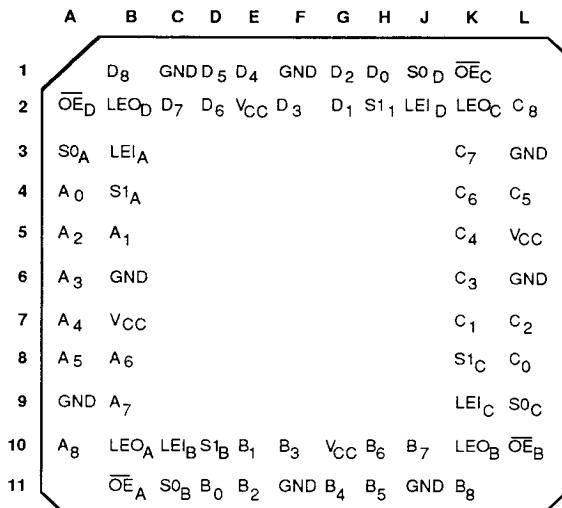
CONNECTION DIAGRAMS**PLCC****(Top View)****Note:**

Pin 1 is marked for orientation.

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PQFP
(Top View)

09485-013A

PGA
(Bottom View)


Note: Notch indicates orientation.

09485-013A

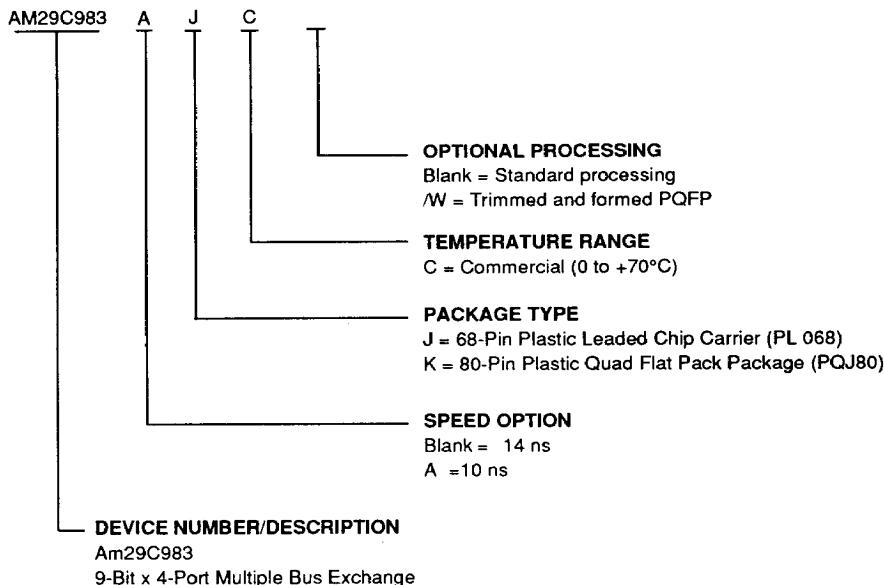
PIN DESIGNATIONS
(Sorted by Pin Number)

| PIN NO. | PIN NAME |
|---------|------------------|---------|------------------|---------|------------------|---------|------------------|
| A-2 | OE _D | B-9 | A ₇ | F-10 | B ₃ | K-4 | C ₆ |
| A-3 | S _{0A} | B-10 | LEO _A | F-11 | GND | K-5 | C ₄ |
| A-4 | A ₀ | B-11 | OE _A | G-1 | D ₂ | K-6 | C ₃ |
| A-5 | A ₂ | C-1 | GND | G-2 | D ₁ | K-7 | C ₁ |
| A-6 | A ₃ | C-2 | D ₇ | G-10 | V _{CC} | K-8 | S _{1C} |
| A-7 | A ₄ | C-10 | LEI _B | G-11 | B ₄ | K-9 | LEI _C |
| A-8 | A ₅ | C-11 | S _{0B} | H-1 | D ₀ | K-10 | LEO _B |
| A-9 | GND | D-1 | D ₅ | H-2 | S _{1D} | K-11 | B ₈ |
| A-10 | A ₈ | D-2 | D ₆ | H-10 | B ₆ | L-2 | C ₈ |
| B-1 | D ₈ | D-10 | S _{1B} | H-11 | B ₅ | L-3 | GND |
| B-2 | LEO _D | D-11 | B ₀ | J-1 | S _{0D} | L-4 | C ₅ |
| B-3 | LEI _A | E-1 | D ₄ | J-2 | LEI _D | L-5 | V _{CC} |
| B-4 | S _{1A} | E-2 | V _{CC} | J-10 | B ₇ | L-6 | GND |
| B-5 | A ₁ | E-10 | B ₁ | J-11 | GND | L-7 | C ₂ |
| B-6 | GND | E-11 | B ₂ | K-1 | OE _C | L-8 | C ₀ |
| B-7 | V _{CC} | F-1 | GND | K-2 | LEO _C | L-9 | S _{0C} |
| B-8 | A ₆ | F-2 | D ₃ | K-3 | C ₇ | L-10 | OE _B |

ORDERING INFORMATION**Standard Products**

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

Device Number
Speed Option (If applicable)
Package Type
Temperature Range
Optional Processing



| Valid Combinations | |
|--------------------|----------|
| AM29C983 | JC |
| AM29C983A | JC, KC/W |

Valid Combinations

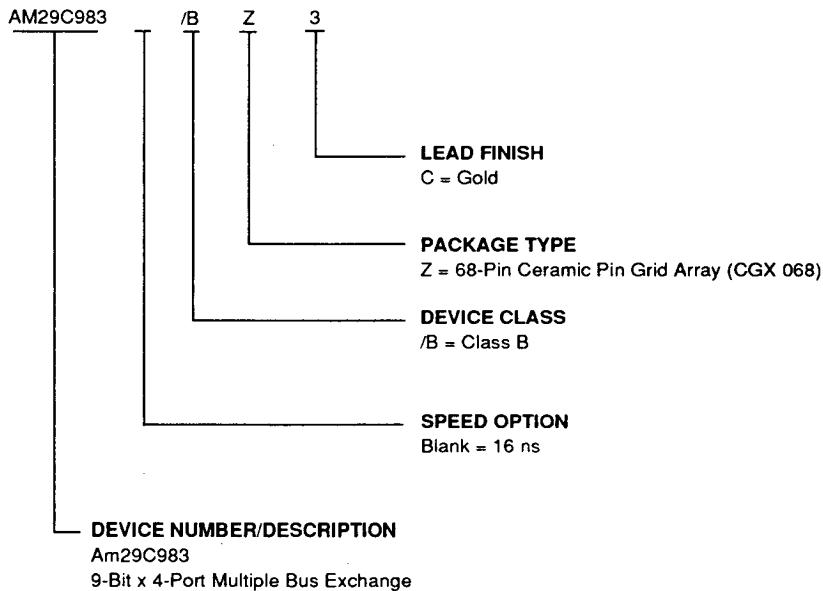
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) is formed by a combination of:

- Device Number**
- Speed Option (if applicable)**
- Package Type**
- Temperature Range**
- Optional Processing**



| Valid Combinations | |
|--------------------|-----|
| AM29C983 | BZC |

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

Group A Tests

Group A tests consists of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

ABSOLUTE MAXIMUM RATINGS

| | |
|---|------------------|
| Supply Voltage (V_{CC}) | -0.5 to 7.0 V |
| DC Input Diode Current (I_{IN}) ($V_{IN} < 0$ V) ($V_{IN} > V_{CC}$ if applicable) | -20 mA +20 mA |
| DC Input Voltage (V_{IN}) | -0.5 to 7 V |
| DC Output Diode Current (I_{OK}) ($V_{OUT} < 0$ V) ($V_{OUT} > V_{CC}$ if applicable) | -50 mA +50 mA |
| DC Output Current per Output Pin: I_{SINK} | +70 mA -30 mA |
| I_{SOURCE} | |
| DC Output Voltage (V_{OUT}) | -0.5 to 7 V |
| Total DC Ground Current (I_{GND}) | 1750 mA |
| Total DC V_{CC} Current (I_{CC}) | 575 mA |
| Storage Temperature | -65 to +150°C |

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES**Commercial (C) Devices**

| | |
|-----------------------------|----------------|
| Temperature (T_A) | 0 to +70°C |
| Supply Voltage (V_{CC}) | +4.5 to +5.5 V |

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

| Am29C983 | | | | | | |
|------------------|---|--|-------------------|-----|------|---------|
| Parameter Symbol | Parameter Description | Test Conditions | | Min | Max | Unit |
| V_{OH} | Output HIGH Voltage | $V_{CC} = 4.5$ V $V_{IN} = V_{IL}$ or V_{IH} | $I_{OH} = -15$ mA | 2.4 | | V |
| V_{OL} | Output LOW Voltage | $V_{CC} = 4.5$ V $V_{IN} = V_{IL}$ or V_{IH} | $I_{OL} = 48$ mA | | 0.5 | V |
| V_{IH} | Input HIGH Voltage | (Note 1) | | 2.0 | | V |
| V_{IL} | Input LOW Voltage | (Note 1) | | | 0.8 | V |
| V_{IC} | Input Clamp Voltage | $V_{CC} = 4.5$ V, $I_{IN} = -18$ mA | | | -1.2 | V |
| I_{IL} | Input LOW Current (Select Inputs) | $V_{CC} = 5.5$ V, $V_{IN} = 0$ V | | | -10 | μ A |
| I_{IH} | Input HIGH Current (Select Inputs) | $V_{CC} = 5.5$ V, $V_{IN} = 5.5$ V | | | 10 | μ A |
| I_{OZL} | Off-State Leakage Current (I/O Ports) | $V_{CC} = 5.5$ V, $V_{OUT} = 0$ V | | | -20 | μ A |
| I_{OZH} | Off-State Leakage Current (I/O Ports) | $V_{CC} = 5.5$ V, $V_{OUT} = 5.5$ V | | | 20 | μ A |
| I_{SC} | Output Short-Circuit Current | $V_{CC} = 5.5$ V, $V_{OUT} = 0$ V (Note 2) | | -60 | | mA |
| I_{CC0} | Quiescent Power Supply Current (Note 4) | $V_{CC} = 5.5$ V, $V_{IN} = 5.5$ V or GND Outputs Open | | | 1.5 | mA |

DC CHARACTERISTICS (Continued)

| Parameter Symbol | Parameter Description | Test Conditions | Min. | Max. | Unit |
|------------------|--|--|------|------|---------------------------|
| I_{CCT} | Power Supply Current TTL Input HIGH (Note 4) | $V_{CC} = 5.5 \text{ V}$, $V_{IN} = 2.4 \text{ V}$ Other Inputs at V_{CC} or GND | | 3.0 | mA/ Input |
| I_{CCD} | Dynamic Power Supply Current (Note 4) | $V_{CC} = 5.5 \text{ V}$, Outputs Open One Output Toggling (Note 3) | | 500 | $\mu\text{A}/$ MHz/Bit |

Am29C983A

| Parameter Symbol | Parameter Description | Test Conditions | Min. | Max. | Unit |
|------------------|--|--|---------------------------|------|---------------------------|
| V_{OH} | Output HIGH Voltage | $V_{CC} = 4.5 \text{ V}$ $V_{IN} = V_{IL}$ or V_{IH} | $I_{OH} = -15 \text{ mA}$ | 2.4 | V |
| V_{OL} | Output LOW Voltage | $V_{CC} = 4.5 \text{ V}$ $V_{IN} = V_{IL}$ or V_{IH} | $I_{OL} = 48 \text{ mA}$ | | 0.5 V |
| V_{IH} | Input HIGH Voltage | (Note 1) | | 2.0 | V |
| V_{IL} | Input LOW Voltage | (Note 1) | | 0.8 | V |
| V_{IC} | Input Clamp Voltage | $V_{CC} = 4.5 \text{ V}$, $I_{IN} = -18 \text{ mA}$ | | -1.2 | V |
| I_{IL} | Input LOW Current (Select Inputs) | $V_{CC} = 5.5 \text{ V}$, $V_{IN} = 0 \text{ V}$ | | -10 | μA |
| I_{IH} | Input HIGH Current (Select Inputs) | $V_{CC} = 5.5 \text{ V}$, $V_{IN} = 5.5 \text{ V}$ | | 10 | μA |
| I_{OZL} | Off-State Leakage Current (I/O Ports) | $V_{CC} = 5.5 \text{ V}$, $V_{OUT} = 0 \text{ V}$ | | -20 | μA |
| I_{OZH} | Off-State Leakage Current (I/O Ports) | $V_{CC} = 5.5 \text{ V}$, $V_{OUT} = 5.5 \text{ V}$ | | 20 | μA |
| I_{SC} | Output Short-Circuit Current | $V_{CC} = 5.5 \text{ V}$, $V_{OUT} = 0 \text{ V}$ (Note 2) | -60 | | mA |
| I_{CCD} | Quiescent Power Supply Current (Note 4) | $V_{CC} = 5.5 \text{ V}$, $V_{IN} = 5.5 \text{ V}$ or GND Outputs Open | | 1.5 | mA |
| I_{CCT} | Power Supply Current TTL Input HIGH (Note 4) | $V_{CC} = 5.5 \text{ V}$, $V_{IN} = 2.4 \text{ V}$ Other Inputs at V_{CC} or GND | | 3.0 | mA/ Input |
| I_{CCD} | Dynamic Power Supply Current (Note 4) | $V_{CC} = 5.5 \text{ V}$, Outputs Open One Output Toggling (Note 3) | | 500 | $\mu\text{A}/$ MHz/Bit |

Notes:

1. Input thresholds are tested in combination with other DC parameters or by correlation.
2. Not more than one output shorted at a time. Duration of short-circuit test not to exceed 100 milliseconds.
3. Measured at a frequency of < 10 MHz with 50% duty cycle. Unused inputs are at V_{CC} or GND.
4. Calculation of total device I_{CC} : $I_{CC} = I_{CCD} + I_{CCT} \times M_t \times D_H + I_{CCD} \times ((C_L + 91) + 91) \times f \times N$

Where C_L = Load Capacitance in pF per output

f = Frequency in MHz

N = Average number of outputs switching

M_t = Number of inputs at logic HIGH

D_H = Duty cycle for each input HIGH

SWITCHING CHARACTERISTICS over COMMERCIAL operating range unless otherwise specified

| Am29C983 | | Parameter Description | Test Conditions | Commercial | | |
|----------|------------------|---|---|------------|-----|------|
| No. | Parameter Symbol | | | Min | Max | Unit |
| 1 | t_{PLH} | Propagation Delay Port to Port LEI = HIGH, LEO = HIGH Propagation Delay Select Input to Port LEO = HIGH Propagation Delay LEI to Port LEO = HIGH Propagation Delay LEO to Port Output Enable Time OE to Port Output Disable Time OE to Port Port to LEI Setup Port to LEI Hold Port to LEO Setup Port to LEO Hold Select to LEI Setup Select to LEI Hold LEI to LEO Setup LEI to LEO Hold LEI, LEO Pulse Width HIGH | $C_L = 50 \text{ pF}$ $R_1 = 500 \text{ Ohms}$ $R_2 = 500 \text{ Ohms}$ | 1.5 | 14 | ns |
| 2 | t_{PHL} | | | 1.5 | 14 | ns |
| 3 | t_{PLH} | | | 1.5 | 18 | ns |
| 4 | t_{PHL} | | | 1.5 | 18 | ns |
| 5 | t_{PLH} | | | 1.5 | 18 | ns |
| 6 | t_{PHL} | | | 1.5 | 18 | ns |
| 7 | t_{PLH} | | | 1.5 | 14 | ns |
| 8 | t_{PHL} | | | 1.5 | 14 | ns |
| 9 | t_{PZH} | | | 1 | 14 | ns |
| 10 | t_{PZL} | | | 1 | 14 | ns |
| 11 | t_{PHZ} | | | 0 | 12 | ns |
| 12 | t_{PLZ} | | | 0 | 12 | ns |
| 13 | t_s | | | 2 | | ns |
| 14 | t_h | | | 3 | | ns |
| 15 | t_s | | | 4.5 | | ns |
| 16 | t_h | | | 1.5 | | ns |
| 17 | t_s | | | 6 | | ns |
| 18 | t_h | | | 0 | | ns |
| 19 | t_s | | | 6 | | ns |
| 20 | t_h | | | 0 | | ns |
| 21 | t_{PWH} | | | 6 | | ns |

SWITCHING CHARACTERISTICS over MILITARY operating range unless otherwise specified (for APL products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted)

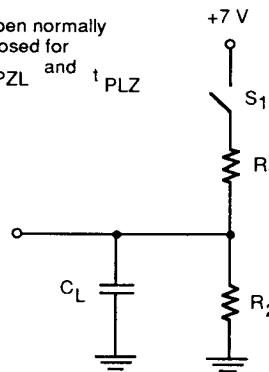
| Am29C983 | | | Military | | | |
|----------|------------------|---|---|-----|-----|------|
| No. | Parameter Symbol | Parameter Description | Test Conditions | Min | Max | Unit |
| 1 | t_{PLH} | Propagation Delay Port to Port | $C_L = 50 \text{ pF}$ $R_1 = 500 \text{ Ohms}$ $R_2 = 500 \text{ Ohms}$ | 1.0 | 16 | ns |
| 2 | t_{PHL} | LEI = HIGH, LEO = HIGH | | 1.0 | 16 | ns |
| 3 | t_{PLH} | Propagation Delay Select Input to Port | | 1.0 | 20 | ns |
| 4 | t_{PHL} | LEO = HIGH | | 1.0 | 20 | ns |
| 5 | t_{PLH} | Propagation Delay LEI to Port | | 1.0 | 20 | ns |
| 6 | t_{PHL} | LEO = HIGH | | 1.0 | 20 | ns |
| 7 | t_{PLH} | Propagation Delay LEO to Port | | 1.0 | 16 | ns |
| 8 | t_{PHL} | Output Enable Time \bar{OE} to Port | | 1.0 | 16 | ns |
| 9 | t_{PZH} | | | 1.5 | 16 | ns |
| 10 | t_{PZL} | | | 1.0 | 16 | ns |
| 11 | t_{PHZ} | Output Disable Time \bar{OE} to Port | | 0 | 14 | ns |
| 12 | t_{PLZ} | | | 0 | 14 | ns |
| 13 | t_s | Port to LEI Setup | | 3 | | ns |
| 14 | t_h | Port to LEI Hold | | 4 | | ns |
| 15 | t_s | Port to LEO Setup | | 5.5 | | ns |
| 16 | t_h | Port to LEO Hold | | 2.5 | | ns |
| 17 | t_s | Select to LEO Setup | | 7 | | ns |
| 18 | t_h | Select to LEO Hold | | 1 | | ns |
| 19 | t_s | LEI to LEO Setup | | 7 | | ns |
| 20 | t_h | LEI to LEO Hold | | 1 | | ns |
| 21 | t_{PWH} | LEI, LEO Pulse Width HIGH | | 7 | | ns |

SWITCHING CHARACTERISTICS over COMMERCIAL operating range unless otherwise specified

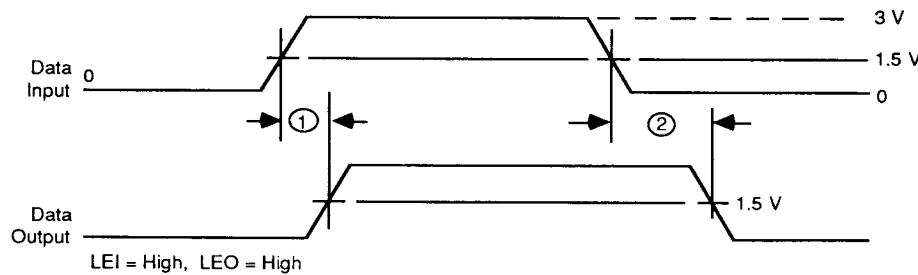
| Am29C983A | | | | Commercial | | |
|-----------|------------------|---|---|------------|-----|------|
| No. | Parameter Symbol | Parameter Description | Test Conditions | Min | Max | Unit |
| 1 | t_{PLH} | Propagation Delay Port to Port LEI = HIGH, LEO = HIGH | $C_L = 50 \text{ pF}$ $R_1 = 500 \text{ Ohms}$ $R_2 = 500 \text{ Ohms}$ | 1.5 | 10 | ns |
| 2 | t_{PHL} | Propagation Delay Select Input to Port LEO = HIGH | | 1.5 | 10 | ns |
| 3 | t_{PLH} | Propagation Delay Select Input to Port LEO = HIGH | | 1.5 | 11 | ns |
| 4 | t_{PHL} | Propagation Delay LEI to Port LEO = HIGH | | 1.5 | 11 | ns |
| 5 | t_{PLH} | Propagation Delay LEI to Port LEO = HIGH | | 1.5 | 12 | ns |
| 6 | t_{PHL} | Propagation Delay LEO to Port | | 1.5 | 12 | ns |
| 7 | t_{PLH} | Propagation Delay LEO to Port | | 1.5 | 10 | ns |
| 8 | t_{PHL} | Output Enable Time \overline{OE} to Port | | 1.5 | 10 | ns |
| 9 | t_{PZH} | Output Enable Time \overline{OE} to Port | | 1 | 10 | ns |
| 10 | t_{PZL} | Output Disable Time \overline{OE} to Port | | 1 | 10 | ns |
| 11 | t_{PHZ} | Output Disable Time \overline{OE} to Port | | 0 | 9 | ns |
| 12 | t_{PLZ} | Port to LEI Setup | | 0 | 9 | ns |
| 13 | t_s | Port to LEI Hold | | 2 | | ns |
| 14 | t_h | Port to LEO Setup | | 3 | | ns |
| 15 | t_s | Port to LEO Hold | | 4.5 | | ns |
| 16 | t_h | Select to LEO Setup | | 1.5 | | ns |
| 17 | t_s | Select to LEO Hold | | 6 | | ns |
| 18 | t_h | LEI to LEO Setup | | 0 | | ns |
| 19 | t_s | LEI to LEO Hold | | 6 | | ns |
| 20 | t_h | LEI, LEO Pulse Width HIGH | | 0 | | ns |
| 21 | t_{PWH} | LEI, LEO Pulse Width HIGH | | 6 | | ns |

SWITCHING TEST CIRCUIT

S_1 = Open normally
 S_1 = Closed for
 t_{PZL} and t_{PLZ}

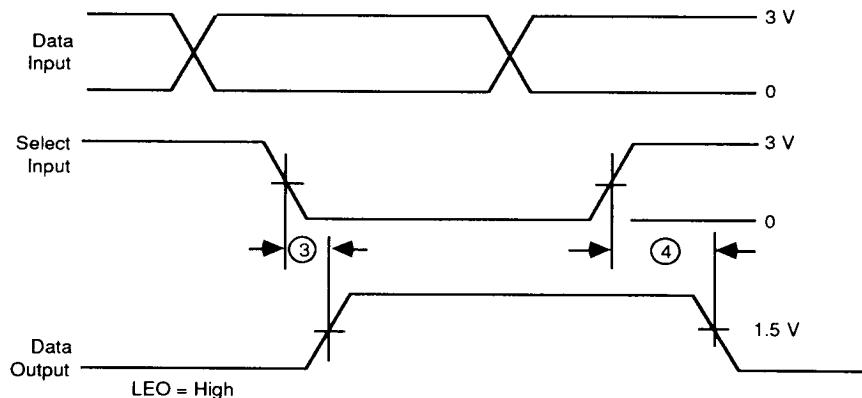


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SWITCHING TEST WAVEFORMS

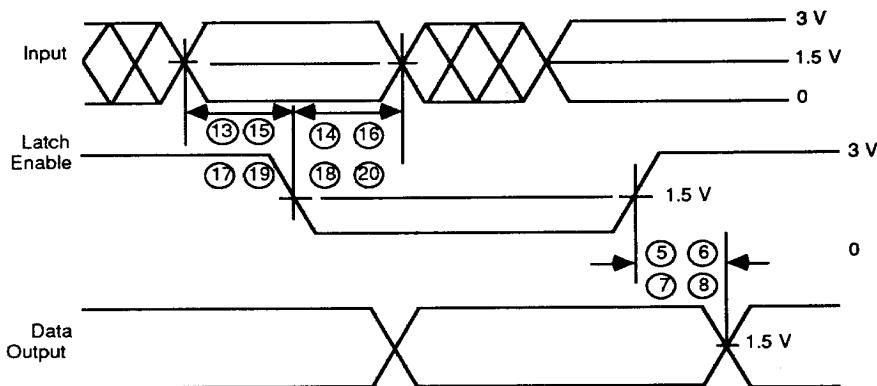
Propagation Delay—Port-to-Port

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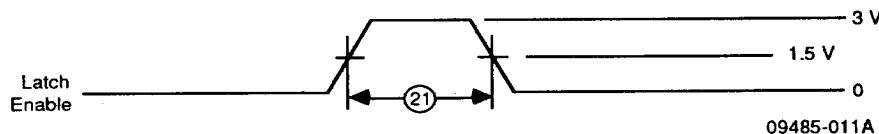


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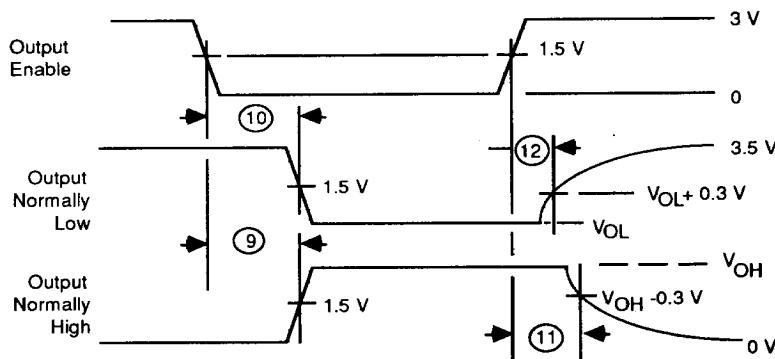
Propagation Delay—Select-to-Port

SWITCHING TEST WAVEFORMS

09485-010B

Input and Output Latch Propagation Delay, Setup and Hold Times

09485-011A

Minimum Latch Enable Pulse Width

09485-012B

Enable and Disable Times