Am29F040

4 Megabit (524,288 x 8-Bit) CMOS 5.0 Volt-only, Sector Erase Flash Memory

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **5.0 V ± 10% read, write, and erase**
  - Minimizes system level power requirements
- **Compatible with JEDEC-standard commands**
  - Uses same software commands as E²PROMs
- **Compatible with JEDEC-standard byte-wide pinouts**
  - 32-pin PLCC/LCC
  - 32-pin TSOP
  - 32-pin DIP
- **Minimum 100,000 write/erase cycles**
- **High performance**
  - 70 ns maximum access time
- **Sector erase architecture**
  - 8 equal size sectors of 64K bytes each
  - Any combination of sectors can be concurrently erased. Also supports full chip erase.
- **Embedded Erase Algorithms**
  - Automatically pre-programs and erases the chip or any sector

- **Embedded Program Algorithms**
  - Automatically writes and verifies data at specified address
- **Data Polling and Toggle Bit feature for detection of program or erase cycle completion**
- **Low power consumption**
  - 20 mA typical active read current
  - 30 mA typical write/erase current
  - 25 µA typical standby current
- **Low V_{CC} write inhibit ≤ 3.2 V**
- **Sector protection**
  - Hardware method disables any combination of sectors from write or erase operations
- **Suspend Erase/Resume**
  - Suspend the erase operation to allow a read data in another sector within the same device

GENERAL DESCRIPTION

The Am29F040 is a 4 Mbit, 5.0 V-only Flash memory organized as 512K bytes of 8 bits each. The Am29F040 is offered in a 32-pin package. This device is designed to be programmed in-system with the standard system 5.0 V V_{CC} supply. A 12.0 V V_{PP} is not required for write or erase operations. The device can also be reprogrammed in standard EPROM programmers.

The standard Am29F040 offers access times between 70 ns and 150 ns, allowing operation of high-speed microprocessors without wait states. To eliminate bus contention the device has separate chip enable ($\overline{CE}$), write enable ($\overline{WE}$) and output enable ($\overline{OE}$) controls.

The Am29F040 is entirely pin and command set compatible with JEDEC standard 4 Mbit E²PROMs.

Commands are written to the command register using standard microprocessor write timings. Register contents serve as input to an internal state-machine which controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the device is similar to reading from 12.0 V Flash or EPROM devices.

The Am29F040 is programmed by executing the program command sequence. This will invoke the Embedded Program Algorithm which is an internal algorithm that automatically times the program pulse widths and verifies proper cell margin. Typically, each sector can be programmed and verified in less than one

PRODUCT SELECTOR GUIDE

Family Part No:		Am29F040			
Ordering Part No: $\quad V_{CC}$ = 5.0 V ± 5%	**-75**				
$\qquad\qquad\qquad\quad V_{CC}$ = 5.0 V ± 10%			**-90**	**-120**	**-150**
Max Access Time (ns)	70		90	120	150
$\overline{CE}$ ($\overline{E}$) Access (ns)	70		90	120	150
$\overline{OE}$ ($\overline{G}$) Access (ns)	30		35	50	55

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second. Erase is accomplished by executing the erase command sequence. This will invoke the Embedded Erase Algorithm which is an internal algorithm that automatically preprograms the array if it is not already programmed before executing the erase operation. During erase, the device automatically times the erase pulse widths and verifies proper cell margin.

The entire chip or any individual sector is typically erased and verified in 1.5 seconds (if already completely preprogrammed).

This device also features a sector erase architecture. The sector mode allows for 64K byte blocks of memory to be erased and reprogrammed without affecting other blocks. The Am29F040 is erased when shipped from the factory.
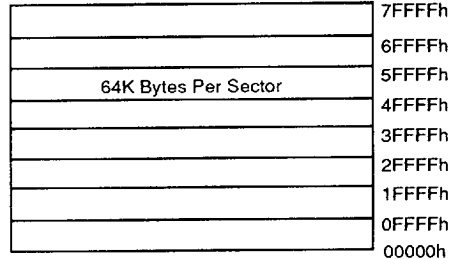
The device features single 5.0 V power supply operation for both read and write functions. Internally generated and regulated voltages are provided for the program and erase operations. A low V_{CC} detector automatically inhibits write operations on the loss of power. The end of program or erase is detected by Data Polling of DQ7 or by the Toggle Bit feature on DQ6. Once the end of a program or erase cycle has been completed, the device internally resets to the read mode.

AMD's Flash technology combines years of EPROM and E²PROM experience to produce the highest levels of quality, reliability and cost effectiveness. The Am29F040 memory electrically erases the entire chip or all bits within a sector simultaneously via Fowler-Nordhiem tunneling. The bytes are programmed one byte at a time using the EPROM programming mechanism of hot electron injection.
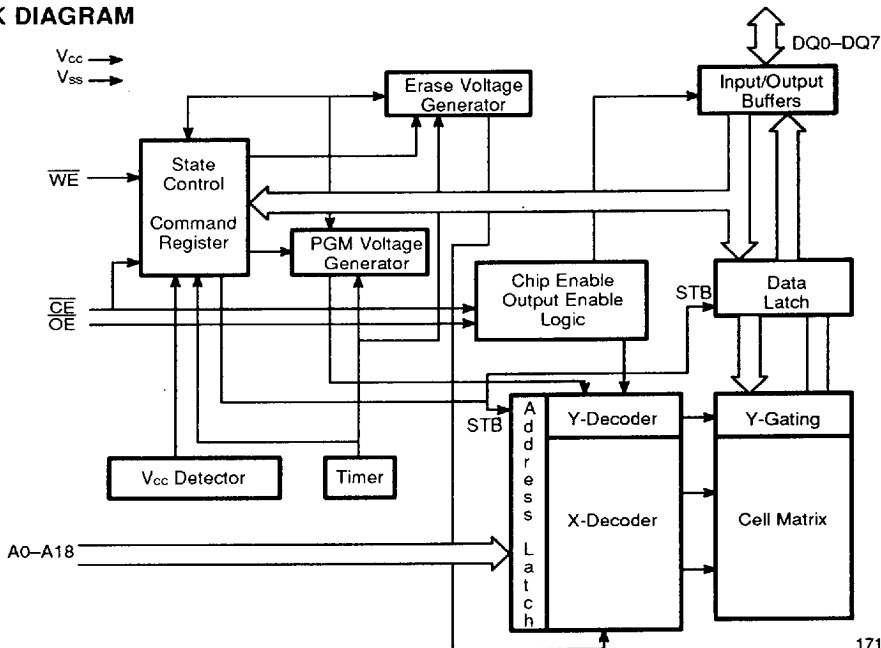
Flexible Sector-Erase Architecture

- 64K Bytes per sector
- Individual-sector, multiple-sector, or bulk-erase capability
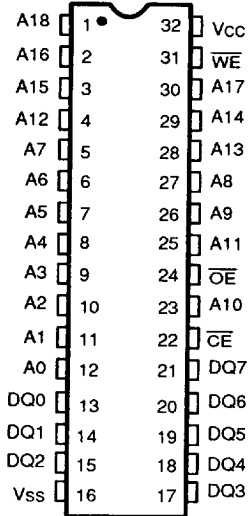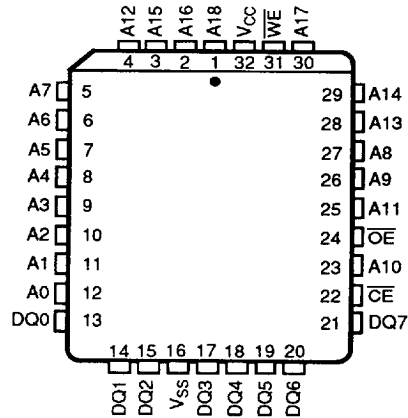- Individual or multiple-sector protection is user definable

	7FFFFh
	6FFFFh
	5FFFFh
64K Bytes Per Sector	4FFFFh
	3FFFFh
	2FFFFh
	1FFFFh
	0FFFFh
	00000h

17113C-1

BLOCK DIAGRAM

17113C-2

CONNECTION DIAGRAMS

CERDIP/PDIP

Left	Pin	Pin	Right
A18	1	32	Vcc
A16	2	31	WE
A15	3	30	A17
A12	4	29	A14
A7	5	28	A13
A6	6	27	A8
A5	7	26	A9
A4	8	25	A11
A3	9	24	OE
A2	10	23	A10
A1	11	22	CE
A0	12	21	DQ7
DQ0	13	20	DQ6
DQ1	14	19	DQ5
DQ2	15	18	DQ4
Vss	16	17	DQ3

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PLCC/LCC

Top pins (4, 3, 2, 1, 32, 31, 30): A12, A15, A16, A18, Vcc, WE, A17

Left	Pin	Pin	Right
A7	5	29	A14
A6	6	28	A13
A5	7	27	A8
A4	8	26	A9
A3	9	25	A11
A2	10	24	OE
A1	11	23	A10
A0	12	22	CE
DQ0	13	21	DQ7

Bottom pins (14, 15, 16, 17, 18, 19, 20): DQ1, DQ2, Vss, DQ3, DQ4, DQ5, DQ6

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TSOP

29F040 Standard Pinout

Left	Pin	Pin	Right
A11	1	32	OE
A9	2	31	A10
A8	3	30	CE
A13	4	29	DQ7
A14	5	28	DQ6
A17	6	27	DQ5
WE	7	26	DQ4
Vcc	8	25	DQ3
A18	9	24	Vss
A16	10	23	DQ2
A15	11	22	DQ1
A12	12	21	DQ0
A7	13	20	A0
A6	14	19	A1
A5	15	18	A2
A4	16	17	A3

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29F040 Reverse Pinout

Left	Pin	Pin	Right
OE	1	32	A11
A10	2	31	A9
CE	3	30	A8
DQ7	4	29	A13
DQ6	5	28	A14
DQ5	6	27	A17
DQ4	7	26	WE
DQ3	8	25	Vcc
Vss	9	24	A18
DQ2	10	23	A16
DQ1	11	22	A15
DQ0	12	21	A12
A0	13	20	A7
A1	14	19	A6
A2	15	18	A5
A3	16	17	A4
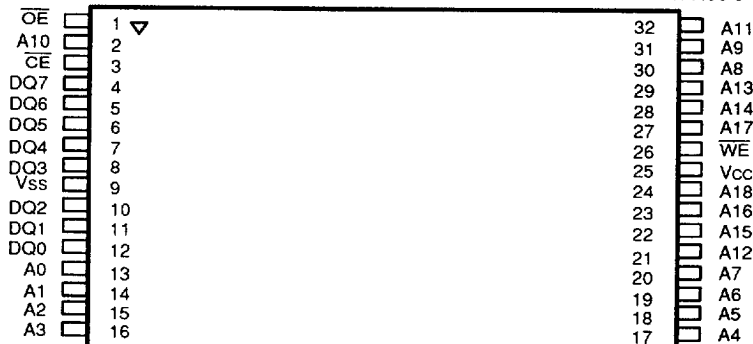
17113C-6

LOGIC SYMBOL
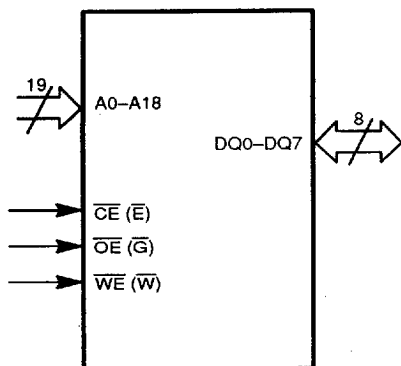
17113C-7

Table 1. Am29F040 Pin Configuration

Pin	Function
A0–A18	Address Inputs
DQ0–DQ7	Data Input/Output
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
Vss	Device Ground
Vcc	Device Power Supply (5.0 V ± 10% or ± 5%)

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ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

AM29F040   -75   J   C   B

OPTIONAL PROCESSING
Blank = Standard Processing
B = Burn-In

TEMPERATURE RANGE
C = Commercial (0°C to +70°C)
I = Industrial (–40°C to +85°C)
E = Extended (–55°C to +125°C)

PACKAGE TYPE
P = 32-Pin Plastic DIP (PD 032)
J = 32-Pin Rectangular Plastic Leaded Chip Carrier (PL 032)
E = 32-Pin Thin Small Outline Package (TSOP) Standard Pinout (TS 032)
F = 32-Pin Thin Small Outline Package (TSOP) Reverse Pinout (TSR 032)

SPEED OPTION
See Product Selector Guide and Valid Combinations

DEVICE NUMBER/DESCRIPTION
Am29F040
4 Megabit (512K x 8-Bit) CMOS Flash Memory
5.0 V Program and Erase
64K Byte Sectors

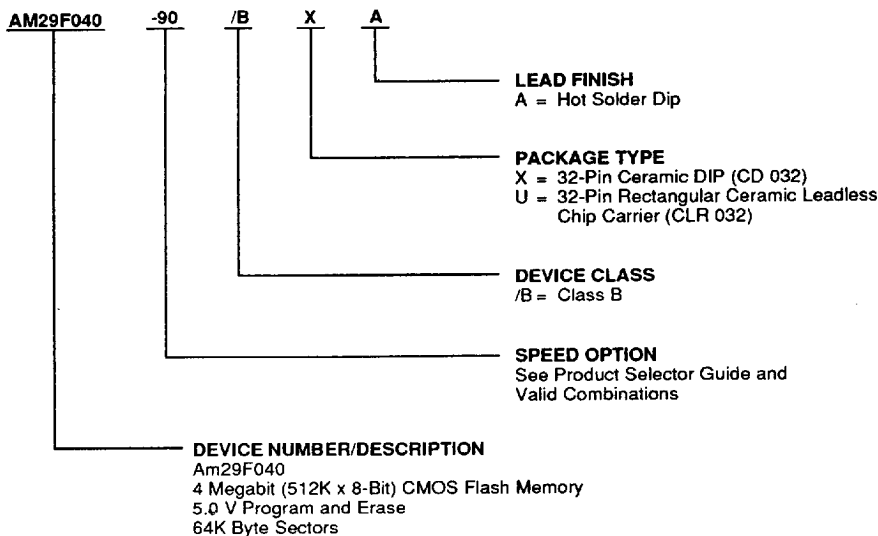| Valid Combinations	
AM29F040-75	JC, EC, FC
AM29F040-90 AM29F040-120 AM29F040-150	DE, DEB, LE, LEB, PC, PI, JC, JI, PCB, PIB, JCB, JIB, PE, PEB, JE, JEB, EC, EI, FC, FI, EE, EEB, FE, FEB

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

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MILITARY ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883 requirements. The order number (Valid Combination) is formed by a combination of:

AM29F040   -90   /B   X   A

LEAD FINISH
A = Hot Solder Dip

PACKAGE TYPE
X = 32-Pin Ceramic DIP (CD 032)
U = 32-Pin Rectangular Ceramic Leadless
    Chip Carrier (CLR 032)

DEVICE CLASS
/B = Class B

SPEED OPTION
See Product Selector Guide and
Valid Combinations

DEVICE NUMBER/DESCRIPTION
Am29F040
4 Megabit (512K x 8-Bit) CMOS Flash Memory
5.0 V Program and Erase
64K Byte Sectors

Valid Combinations	
AM29F040-90	
AM29F040-120	/BXA, /BUA
AM29F040-150	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and or to check on newly released combinations.

Group A Tests
Group A tests consist of Subgroups
1, 2, 3, 7, 8, 9, 10, 11.

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Table 2. Am29F040 User Bus Operations

Operation	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	A0	A1	A6	A9	I/O
Auto-Select Manufacturer Code (1)	L	L	H	L	L	L	V_{ID}	Code
Auto-Select Device Code (1)	L	L	H	H	L	L	V_{ID}	Code
Read (4)	L	L	H	A0	A1	A6	A9	D_{OUT}
Standby	H	X	X	X	X	X	X	HIGH Z
Output Disable	L	H	H	X	X	X	X	HIGH Z
Write	L	H	L	A0	A1	A6	A9	D_{IN} (2)
Enable Sector Protect	L	V_{ID}	L	X	X	X	V_{ID}	X
Verify Sector Protect (3)	L	L	H	L	H	L	V_{ID}	Code

Legend:

$L = V_{IL}$, $H = V_{IH}$, X = Don't Care. See DC Characteristics for voltage levels.

Notes:

1. Manufacturer and device codes may also be accessed via a command register write sequence. Refer to Tables 3 and 4.

2. Refer to Table 4 for valid D_{IN} during a write operation.

3. Refer to the section on Sector Protection

4. $\overline{WE}$ can be V_{IL} if $\overline{OE}$ is V_{IL}, $\overline{OE}$ at V_{IH} initiates the write operations.

Read Mode

The Am29F040 has two control functions which must be satisfied in order to obtain data at the outputs. $\overline{CE}$ is the power control and should be used for device selection. $\overline{OE}$ is the output control and should be used to gate data to the output pins if a device is selected.

Address access time (t_{ACC}) is equal to the delay from stable addresses to valid output data. The chip enable access time (t_{CE}) is the delay from stable addresses and stable $\overline{CE}$ to valid data at the output pins. The output enable access time is the delay from the falling edge of $\overline{OE}$ to valid data at the output pins (assuming the addresses have been stable for at least $t_{ACC}-t_{OE}$ time).

Standby Mode

The Am29F040 has two standby modes, a CMOS standby mode ($\overline{CE}$ input held at Vcc $\pm$ 0.5 V), when the current consumed is less than 100 µA; and a TTL standby mode ($\overline{CE}$ is held at V_{IH}) when the current required is reduced to approximately 1 mA. In the standby mode the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

If the device is deselected during erasure or programming, the device will draw active current until the operation is completed.

Output Disable

With the $\overline{OE}$ input at a logic high level (V_{IH}), output from the device is disabled. This will cause the output pins to be in a high impedance state.

Autoselect

The autoselect mode allows the reading out of a binary code from the device and will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional over the entire temperature range of the device.

To activate this mode, the programming equipment must force V_{ID} (11.5 V to 12.5 V) on address pin A9. Two identifier bytes may then be sequenced from the device outputs by toggling address A0 from V_{IL} to V_{IH}. All addresses are don't cares except A0, A1, and A6.

The manufacturer and device codes may also be read via the command register, for instances when the AM29F040 is erased or programmed in a system without access to high voltage on the A9 pin. The command sequence is illustrated in Table 5 (refer to Autoselect Command section).

Byte 0 (A0 = V_{IL}) represents the manufacture's code (AMD=01H) and byte 1 (A0 = V_{IH}) the device identifier code (Am29F040=A4H). These two bytes are given in the table below. All identifiers for manufactures and device will exhibit odd parity with the MSB (DQ7) defined as the parity bit. In order to read the proper device codes when executing the autoselect, A1 must be V_{IL} (see Table 3).

Table 3. Am29F040 Sector Protection Verify Autoselect Codes

Type	A18	A17	A16	A6	A1	A0	Code (HEX)	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
Manufacture Code	X	X	X	V_{IL}	V_{IL}	V_{IL}	01H	0	0	0	0	0	0	0	1
Am29F040 Device Code	X	X	X	V_{IL}	V_{IL}	V_{IH}	A4H	1	0	1	0	0	1	0	0
Sector Protection	Sector Addresses			V_{IL}	V_{IH}	V_{IL}	01H*	0	0	0	0	0	0	0	1

*Outputs 01H at protected sector addresses

Table 4. Sector Address Tables

	A18	A17	A16	Address Range
SA0	0	0	0	00000h–0FFFFh
SA1	0	0	1	10000h–1FFFFh
SA2	0	1	0	20000h–2FFFFh
SA3	0	1	1	30000h–3FFFFh
SA4	1	0	0	40000h–4FFFFh
SA5	1	0	1	50000h–5FFFFh
SA6	1	1	0	60000h–6FFFFh
SA7	1	1	1	70000h–7FFFFh

Write

Device erasure and programming are accomplished via the command register. The contents of the register serve as inputs to the internal state machine. The state machine outputs dictate the function of the device.

The command register itself does not occupy any addressable memory location. The register is a latch used to store the commands, along with the address and data information needed to execute the command. The command register is written by bringing $\overline{WE}$ to V_{IL}, while $\overline{CE}$ is at V_{IL} and $\overline{OE}$ is at V_{IH}. Addresses are latched on the falling edge of $\overline{WE}$ or $\overline{CE}$, whichever happens later; while data is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$, whichever happens first. Standard microprocessor write timings are used.

Refer to AC Write Characteristics and the Erase/Programming Waveforms for specific timing parameters.

Sector Protection

The Am29F040 features hardware sector protection. This feature will disable both program and erase operations in any number of sectors (0 through 8). The sector protect feature is enabled using programming equipment at the user's site. The device is shipped with all sectors unprotected. Alternatively, AMD may program and protect sectors in the factory prior to shipping the device (AMD's ExpressFlash™ Service).

To activate this mode, the programming equipment must force V_{ID} on address pin A9 and control pin $\overline{OE}$, (suggest V_{ID} = 11 V) and $\overline{CE}$ = V_{IH}. The sector addresses (A18, A17, and A16) should be set to the sector to be protected. Table 4 defines the sector address for each of the eight (8) individual sectors. Programming of the protection circuitry begins on the falling edge of the $\overline{WE}$ pulse and is terminated with the rising edge of the same. Sector addresses must be held constant during the $\overline{WE}$ pulse.

To verify programming of the protection circuitry, the programming equipment must force V_{ID} on address pin A9 with $\overline{CE}$ and $\overline{OE}$ at V_{IL} and $\overline{WE}$ at V_{IH}. Scanning the sector addresses (A16, A17, and A18) while (A6, A1, A0) = (0, 1, 0) will produce a logical "1" code at device output DQ0 for a protected sector. Otherwise the device will read 00H for unprotected sector. In this mode, the lower order addresses, except for A0, A1, and A6 are don't care. Address locations with A1 = V_{IL} are reserved for Autoselect manufacturer and device codes.

It is also possible to determine if a sector is protected in the system by writing an Autoselect command. Performing a read operation at the address location XX02H, where the higher order addresses (A16, A17, and A18) are the sector address will produce a logical "1" at DQ0 for a protected sector. See Table 3 for Autoselect codes.

Command Definitions

Device operations are selected by writing specific address and data sequences into the command register. Writing incorrect address and data values or writing them in the improper sequence will reset the device to read mode. Table 5 defines the valid register command sequences. Note that the Erase Suspend (B0) and Erase Resume (30) commands are valid only while the Sector Erase operation is in progress. Either of the two reset commands will reset the device (when applicable).

Table 5. Am29F040 Command Definitions

Command Sequence Read/Reset	Bus Write Cycles Req'd	First Bus Write Cycle		Second Bus Write Cycle		Third Bus Write Cycle		Fourth Bus Read/Write Cycle		Fifth Bus Write Cycle		Sixth Bus Write Cycle	
		Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read/Reset	1	XXXH	F0H										
Read/Reset	4	5555H	AAH	2AAAH	55H	5555H	F0H	RA	RD				
Autoselect	4	5555H	AAH	2AAAH	55H	5555H	90H						
Byte Program	4	5555H	AAH	2AAAH	55H	5555H	A0H	PA	Data				
Chip Erase	6	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	5555H	10H
Sector Erase	6	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	SA	30H
Sector Erase Suspend	Erase can be suspended during sector erase with Addr (don't care), Data (B0H)												
Sector Erase Resume	Erase can be resumed after suspend with Addr (don't care), Data (30H)												

Notes:

1. Address bits A15, A16, A17, and A18 = X = Don't Care. Write Sequences may be initiated with A15 in either state.
2. Address bits A15, A16, A17, and A18 = X = Don't Care for all address commands except for Program Address (PA) and Sector Address (SA).
3. Bus operations are defined in Table 2.
4. RA = Address of the memory location to be read.
   PA = Address of the memory location to be programmed. Addresses are latched on the falling edge of the $\overline{WE}$ pulse.
   SA = Address of the sector to be erased. The combination of A18, A17, A16 will uniquely select any sector.
5. RD = Data read from location RA during read operation.
   PD = Data to be programmed at location PA. Data is latched on the falling edge of $\overline{WE}$.

Read/Reset Command

The read or reset operation is initiated by writing the read/reset command sequence into the command register. Microprocessor read cycles retrieve array data from the memory. The device remains enabled for reads until the command register contents are altered.

The device will automatically power-up in the read/reset state. In this case, a command sequence is not required to read data. Standard microprocessor read cycles will retrieve array data. This default value ensures that no spurious alteration of the memory content occurs during the power transition. Refer to the AC Read Characteristics and Waveforms for the specific timing parameters.

Autoselect Command

Flash memories are intended for use in applications where the local CPU alters memory contents. As such, manufacture and device codes must be accessible while the device resides in the target system. PROM programmers typically access the signature codes by raising A9 to a high voltage. However, multiplexing high voltage onto the address lines is not generally desired system design practice.

The device contains a command autoselect operation to supplement traditional PROM programming methodology. The operation is initiated by writing the autoselect command sequence into the command register. Following the command write, a read cycle from address XX00H retrieves the manufacture code of 01H. A read cycle from address XX01H returns the device code A4H (see Table 3). All manufacturer and device codes will exhibit odd parity with the MSB (DQ7) defined as the parity bit.

Scanning the sector addresses (A16, A17, A18) while (A6, A1, A0) = (0, 1, 0) will produce a logical "1" at device output DQ0 for a protected sector.

To terminate the operation, it is necessary to write the read/reset command sequence into the register.

Byte Programming

The device is programmed on a byte-by-byte basis. Programming is a four bus cycle operation. There are two "unlock" write cycles. These are followed by the program set-up command and data write cycles. Addresses are latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever happens later and the data is latched on the rising edge of $\overline{CE}$ or $\overline{WE}$, whichever happens first. The rising edge of $\overline{CE}$ or $\overline{WE}$ (whichever happens first) begins programming. Upon executing the Embedded Program Algorithm command sequence the system is not required to provide further controls or timings. The device will automatically provide adequate internally generated program pulses and verify the programmed cell margin.

The automatic programming operation is completed when the data on DQ7 is equivalent to data written to this bit (see Write Operation Status section) at which time the device returns to the read mode and addresses are no longer latched. Therefore, the device requires that a valid address to the device be supplied by the system at this particular instance of time. Hence, Data Polling must be performed at the memory location which is being programmed.

Any commands written to the chip during this period will be ignored.

Programming is allowed in any sequence and across sector boundaries. Beware that a data "0" cannot be programmed back to a "1". Attempting to do so will probably hang up the device (exceed timing limits), or perhaps result in an apparent success according to the data polling algorithm but a read from reset/read mode will show that the data is still "0". Only erase operations can convert "0"s to "1"s.

Figure 1 illustrates the Embedded Programming Algorithm using typical command strings and bus operations.

Chip Erase

Chip erase is a six bus cycle operation. There are two "unlock" write cycles. These are followed by writing the "set-up" command. Two more "unlock" write cycles are then followed by the chip erase command.

Chip erase does *not* require the user to program the device prior to erase. Upon executing the Embedded Erase™ Algorithm command sequence the device automatically will program and verify the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations.

The automatic erase begins on the rising edge of the last $\overline{WE}$ pulse in the command sequence and terminates when the data on DQ7 is "1" (see Write Operation Status section) at which time the device returns to read the mode.

Figure 2 illustrates the Embedded Erase Algorithm using typical command strings and bus operations.

Sector Erase

Sector erase is a six bus cycle operation. There are two "unlock" write cycles. These are followed by writing the "set-up" command. Two more "unlock" write cycles are then followed by the sector erase command. The sector address (any address location within the desired sector) is latched on the falling edge of $\overline{WE}$, while the command (data) is latched on the rising edge of $\overline{WE}$. A time-out of 80 µs from the rising edge of the last sector erase command will initiate the sector erase command(s). *Please note: Do not attempt to write an invalid command sequence during the sector erase operation. Otherwise, it will terminate the sector erase operation and the device will reset back into the read mode.*

Multiple sectors may be erased concurrently by writing the six bus cycle operations as described above. This sequence is followed with writes of the Sector Erase command to addresses in other sectors desired to be concurrently erased. The time between writes must be less than 80 µs, otherwise that command will not be accepted. It is recommended that processor interrupts be disabled during this time to guarantee this condition. The interrupts can be re-enabled after the last Sector Erase command is written. A time-out of 80 µs from the rising edge of the last $\overline{WE}$ will initiate the execution of the Sector Erase command(s). If another falling edge of the $\overline{WE}$ occurs within the 80 µs time-out window the timer is

reset. (Monitor DQ3 to determine if the sector erase window is still open, see section DQ3, Sector Erase Timer.) Any command other than Sector Erase or Erase Suspend during this period and afterwards will reset the device to read mode, ignoring the previous command string. Resetting the device after it has begun execution will result in the data of the operated sectors being undefined (messed up). In that case, restart the erase on those sectors and allow them to complete. (Refer to the Write Operation Status section for Sector Erase Timer operation.) Loading the sector erase buffer may be done in any sequence and with any number of sectors (1 to 8).

Sector erase does *not* require the user to program the device prior to erase. The device automatically programs all memory locations in the sector(s) to be erased prior to electrical erase. When erasing a sector or sectors the remaining unselected sectors are not affected. The system is *not* required to provide any controls or timings during these operations.

The automatic sector erase begins after the 100 µs time out from the rising edge of the $\overline{WE}$ pulse for the last sector erase command pulse and terminates when the data on DQ7 is "1" (see Write Operation Status section) at which time the device returns to read mode. *During the execution of the Sector Erase command, only the Erase Suspend and Erase Resume commands are allowed. All other commands will reset the device to read mode.* Data polling must be performed at an address within any of the sectors being erased.

Figure 2 illustrates the Embedded Erase Algorithm using typical command strings and bus operations.

Erase Suspend

Erase Suspend command allows the user to interrupt the chip and then do data reads (not program) from a non-busy sector while it is in the middle of a Sector Erase operation (which may take up to several seconds). This command is applicable ONLY during the Sector Erase operation and will be ignored if written during the chip Erase or Programming operation. The Erase Suspend command (B0) will be allowed only during the Sector Erase Operation that will include the sector erase time-out period after the Sector Erase commands (30). Writing this command during the time-out will result in immediate termination of the time-out period. Any subsequent writes of the Sector Erase command will be taken as the Erase Resume command. Note that any other commands during the time out will reset the device to read mode. The addresses are don't-cares in writing the erase Suspend or Erase Resume commands.

When the Erase Suspend command is written during a Sector Erase operation, the chip will take between 0.1 µs to 15 µs to suspend the erase operation and go into erase suspended read mode (pseudo-read mode), during which the user can read from a sector that is NOT being erased. A read from a sector being erased may result in invalid data. The user must monitor the toggle bit to determine if the chip has entered the pseudo-read

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mode, at which time the toggle bit stops toggling. An address of a sector NOT being erased must be used to read the toggle bit, otherwise the user may encounter intermittent problems. Note that the user must keep track of what state the chip is in since there is no external indication of whether the chip is in pseudo-read mode or actual read mode. After the user writes the Erase Suspend command and waits until the toggle bit stops toggling, data reads from the device may then be performed. Any further writes of the Erase Suspend command at this time will be ignored.

Every time an Erase Suspend command followed by an Erase Resume command is written, the internal (pulse)

counters are reset. These counters are used to count the number of high voltage pulses the memory cell requires to program or erase. If the count exceeds a certain limit, then the DQ5 bit will be set (Exceeded Time Limit flag). This resetting of the counters is necessary since the Erase Suspend command can potentially interrupt or disrupt the high voltage pulses.

To resume the operation of Sector Erase, the Resume command (30) should be written. Any further writes of the Resume command at this point will be ignore. Another Erase Suspend command can be written after the chip has resumed.

Write Operation Status

Table 6. Hardware Sequence Flags

	Status	DQ7	DQ6	DQ5	DQ3	DQ2–DQ0
In Progress	Auto-Programming	$\overline{DQ7}$	Toggle	0	0	$(\overline{D})$
	Program/Erase in Auto Erase	0	Toggle	0	1	
Exceeded Time Limits	Auto-Programming	$\overline{DQ7}$	Toggle	1	1	$(\overline{D})$
	Program/Erase in Auto-Erase	0	Toggle	1	1	

Note: DQ0, DQ1, and DQ2 are reserve pins for future use. DQ4 is for AMD internal use only.

DQ7
Data Polling

The Am29F040 device features $\overline{Data}$ Polling as a method to indicate to the host that the Embedded Algorithms are in progress or completed. During the Embedded Program Algorithm an attempt to read the device will produce the compliment of the data last written to DQ7. Upon completion of the Embedded Program Algorithm, an attempt to read the device will produce the true data last written to DQ7. During the Embedded Erase Algorithm, an attempt to read the device will produce a "0" at the DQ7 output. Upon completion of the Embedded Erase Algorithm an attempt to read the device will produce a "1" at the DQ7 output. The flowchart for $\overline{Data}$ Polling (DQ7) is shown in Figure 3.

For chip erase, the $\overline{Data}$ Polling is valid after the rising edge of the sixth $\overline{WE}$ pulse in the six write pulse sequence. For sector erase, the $\overline{Data}$ Polling is valid after the last rising edge of the sector erase $\overline{WE}$ pulse. Data Polling must be performed at sector address within any of the sectors being erased and **not** a protected sector. Otherwise, the status may not be valid. Once the Embedded Algorithm operation is close to being completed, the Am29F040 data pins (DQ7) may change asynchronously while the output enable ($\overline{OE}$) is asserted low. This means that the device is driving status information on DQ7 at one instant of time and then that byte's valid data at the next instant of time. Depending on when the system samples the DQ7 output, it may read the status or valid data. Even if the device has completed the Embedded Algorithm operation and DQ7 has a valid data, the data outputs on DQ0–DQ6 may be still

invalid. The valid data on DQ0–DQ7 will be read on the successive read attempts.

The $\overline{Data}$ Polling feature is only active during the Embedded Programming Algorithm, Embedded Erase Algorithm, or sector erase time-out (see Table 6).

See Figure 11 for the $\overline{Data}$ Polling timing specifications and diagrams.

DQ6
Toggle Bit

The Am29F040 also features the "Toggle Bit" as a method to indicate to the host system that the Embedded Algorithms are in progress or completed.

During an Embedded Program or Erase Algorithm cycle, successive attempts to read ($\overline{OE}$ toggling) data from the device will result in DQ6 toggling between one and zero. Once the Embedded Program or Erase Algorithm cycle is completed, DQ6 will stop toggling and valid data will be read on *the next* successive attempts. During programming, the Toggle Bit is valid after the rising edge of the fourth $\overline{WE}$ pulse in the four write pulse sequence. For chip erase, the Toggle Bit is valid after the rising edge of the sixth $\overline{WE}$ pulse in the six write pulse sequence. For Sector erase, the Toggle Bit is valid after the last rising edge of the sector erase $\overline{WE}$ pulse. The Toggle Bit is active during the sector time out.

In programming, if the sector being written to is protected, the toggle bit will toggle for about 2 μs and then stop toggling without the data having changed. In erase, the device will erase all the selected sectors except for the ones that are protected. If all selected sectors are

protected, the chip will toggle the toggle bit for about 100 μs and then drop back into read mode, having changed none of the data.

Either $\overline{CE}$ or $\overline{OE}$ toggling will cause the DQ6 to toggle.

See Figure 12 for the Toggle Bit timing specifications and diagrams.

DQ5
Exceeded Timing Limits

DQ5 will indicate if the program or erase time has exceeded the specified limits (internal pulse count). Under these conditions DQ5 will produce a "1". This is a failure condition which indicates that the program or erase cycle was not successfully completed. Data Polling is the only operating function of the device under this condition. The $\overline{CE}$ circuit will partially power down the device under these conditions (to approximately 2 mA). The $\overline{OE}$ and $\overline{WE}$ pins will control the output disable functions as described in Table 2.

If this failure condition occurs during sector erase operation, it specifies that a particular sector is bad and it may not be reused, however, other sectors are still functional and may be used for the program or erase operation. The device must be reset to use other sectors. Write the Reset command sequence to the device, and then execute program or erase command sequence. This allows the system to continue to use the other active sectors in the device.

If this failure condition occurs during the chip erase operation, it specifies that the entire chip is bad or combination of sectors are bad.

If this failure condition occurs during the byte programming operation, it specifies that the entire sector containing that byte is bad and this sector may not be reused, (other sectors are still functional and can be reused).

The DQ5 failure condition may also appear if a user tries to program a non blank location without erasing. In this case the device locks out and never completes the Embedded Algorithm operation. Hence, the system never reads a valid data on DQ7 bit and DQ6 never stops toggling. Once the device has exceeded timing limits, the DQ5 bit will indicate a "1." Please note that this is not a device failure condition since the device was incorrectly used.

DQ3
Sector Erase Timer

After the completion of the initial sector erase command sequence the sector erase time-out will begin. DQ3 will remain low until the time-out is complete. Data Polling and Toggle Bit are valid after the initial sector erase command sequence.

If Data Polling or the Toggle Bit indicates the device has been written with a valid erase command, DQ3 may be used to determine if the sector erase timer window is still

open. If DQ3 is high ("1") the internally controlled erase cycle has begun; attempts to write subsequent commands to the device will be ignored until the erase operation is completed as indicated by Data Polling or Toggle Bit. If DQ3 is low ("0"), the device will accept additional sector erase commands. To insure the command has been accepted, the system software should check the status of DQ3 prior to and following each subsequent sector erase command. If DQ3 were high on the second status check, the command may not have been accepted.

Refer to Table 6: Hardware Sequence Flags.

Data Protection

The Am29F040 is designed to offer protection against accidental erasure or programming caused by spurious system level signals that may exist during power transitions. During power up the device automatically resets the internal state machine in the Read mode. Also, with its control register architecture, alteration of the memory contents only occurs after successful completion of specific multi-bus cycle command sequences.

The device also incorporates several features to prevent inadvertent write cycles resulting form Vcc power-up and power-down transitions or system noise.

Low Vcc Write Inhibit

To avoid initiation of a write cycle during Vcc power-up and power-down, a write cycle is locked out for Vcc less than 3.2 V (typically 3.7 V). If $V_{CC} < V_{LKO}$, the command register is disabled and all internal program/erase circuits are disabled. Under this condition the device will reset to the read mode. Subsequent writes will be ignored until the Vcc level is greater than V_{LKO}.

Write Pulse "Glitch" Protection

Noise pulses of less than 5 ns (typical) on $\overline{OE}$, $\overline{CE}$ or $\overline{WE}$ will not initiate a write cycle.

Logical Inhibit

Writing is inhibited by holding any one of $\overline{OE} = V_{IL}$, $\overline{CE} = V_{IH}$ or $\overline{WE} = V_{IH}$. To initiate a write cycle $\overline{CE}$ and $\overline{WE}$ must be a logical zero while $\overline{OE}$ is a logical one.

Power-Up Write Inhibit

Power-up of the device with $\overline{WE} = \overline{CE} = V_{IL}$ and $\overline{OE} = V_{IH}$ will not accept commands on the rising edge of $\overline{WE}$. The internal state machine is automatically reset to the read mode on power-up.

Sector Protect

Sectors of the Am29F040 may be hardware protected at the users factory. The protection circuitry will disable both program and erase functions for the protected sector(s). Requests to program or erase a protected sector will be ignored by the device.

0257528 0032507 922

EMBEDDED ALGORITHMS

```
                        ┌─────────────┐
                        │    Start    │
                        └─────────────┘
                               │
          ┌────────────────────▼────────────────────┐
          │      Write Program Command Sequence      │
          │              (see below)                 │
          └────────────────────┬────────────────────┘
          │                     │
          │      ┌──────────────▼──────────────┐
          │      │      Data Poll Device        │
          │      └──────────────┬──────────────┘
          │                     │
 ┌────────┴────────┐    No      ▼
 │Increment Address│◄──────◄ Last Address ►
 └─────────────────┘         ?
                              │
                             Yes
                              ▼
                    ┌──────────────────────┐
                    │ Programming Completed │
                    └──────────────────────┘
```

Program Command Sequence (Address/Command):
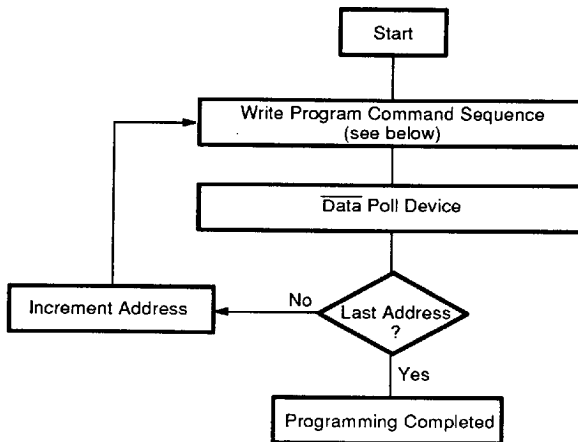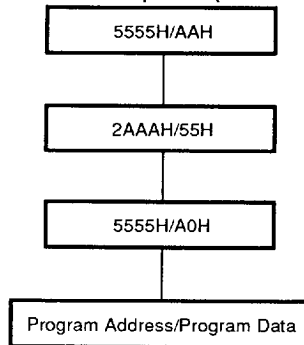
```
        ┌─────────────────────┐
        │      5555H/AAH      │
        └──────────┬──────────┘
                   │
        ┌──────────▼──────────┐
        │      2AAAH/55H      │
        └──────────┬──────────┘
                   │
        ┌──────────▼──────────┐
        │      5555H/A0H      │
        └──────────┬──────────┘
                   │
┌──────────────────▼──────────────────┐
│   Program Address/Program Data       │          17113C-8
└─────────────────────────────────────┘
```

Figure 1. Embedded Programming Algorithm

Table 7. Embedded Programming Algorithm

Bus Operations	Command Sequence	Comments
Standby (Note 1)		
Write	Program	Valid Address/Data Sequence
Read		Data Polling to Verify Programming
Standby (Note 1)		Compare Data Output to Data Expected

Note: Device is either powered-down, erase inhibit or program inhibit.

EMBEDDED ALGORITHMS

```
                          ┌──────────────┐
                          │    Start     │
                          └──────┬───────┘
                   ┌─────────────┴─────────────┐
                   │ Write Erase Command Sequence │
                   │        (see below)         │
                   └─────────────┬─────────────┘
                   ┌─────────────┴─────────────┐
                   │ Data Polling or Toggle Bit │
                   │   Successfully Completed   │
                   └─────────────┬─────────────┘
                          ┌───────┴───────┐
                          │ Erasure Completed │
                          └───────────────┘
```

Chip Erase Command Sequence (Address/Command):	Individual Sector/Multiple Sector Erase Command Sequence (Address/Command):
5555H/AAH	5555H/AAH
2AAAH/55H	2AAAH/55H
5555H/80H	5555H/80H
5555H/AAH	5555H/AAH
2AAAH/55H	2AAAH/55H
5555H/10H	Sector Address/30H
	Sector Address/30H
	⋮
	Sector Address/30H

Additional sector erase commands are optional

17113C-9

Figure 2. Embedded Erase Algorithm

Table 8. Embedded Programming Algorithm

Bus Operations	Command Sequence	Comments
Standby		
Write	Erase	
Read		Data Polling to Verify Erasure
Standby		Compare Output to FFH

■ 0257528 0032509 7T5 ■

VA = Byte address for programming
= Any of the sector addresses within the sector being erased during sector erase operation
= XXXXH during chip erase
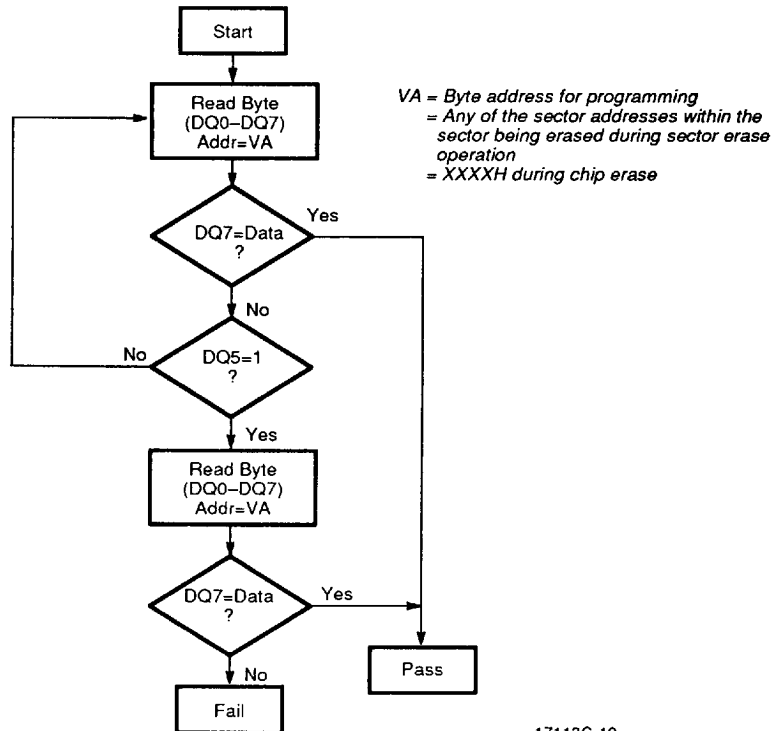
17113C-10

Note: *DQ7 is rechecked even if DQ5 = "1" because DQ7 may change simultaneously with DQ5.*

Figure 3. Data Polling Algorithm

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VA = Byte address for programming
  = any of the sector addresses within the sector being erased during sector erase operation
  = XXXXH during chip erase
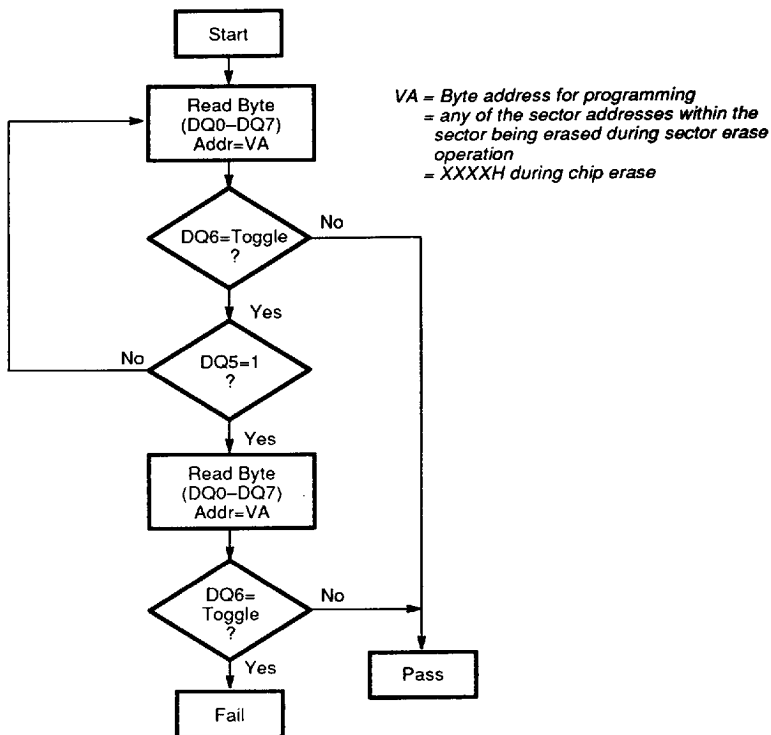
17113C-11

Note:

DQ6 is rechecked even if DQ5 = "1" because DQ6 may stop toggling at the same time as DQ5 changing to "1".

Figure 4. Toggle Bit Algorithm

17113C-12
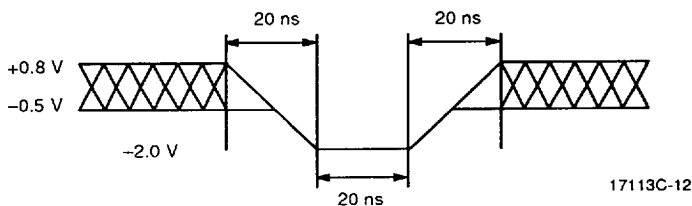
Figure 5. Maximum Negative Overshoot Waveform

17113C-13
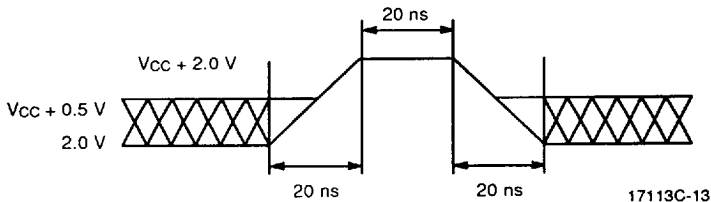
Figure 6. Maximum Positive Overshoot Waveform

0257528 0032511 353

ABSOLUTE MAXIMUM RATINGS

Storage Temperature
Ceramic Packages . . . . −65°C to +150°C
Plastic Packages . . . . −65°C to +125°C

Ambient Temperature
with Power Applied . . . . −55°C to +125°C

Voltage with Respect to Ground
All pins except A9 (Note 1) . . . . −2.0 V to +7.0 V

V_{CC} (Note 1) . . . . −2.0 V to +7.0 V

A9 (Note 2) . . . . −2.0 V to +14.0 V

Output Short Circuit Current (Note 3) . . . . . . 200 mA

Notes:

1. *Minimum DC voltage on input or I/O pins is −0.5 V. During voltage transitions, inputs may undershoot V_{SS} to −2.0 V for periods of up to 20 ns. Maximum DC voltage on output and I/O pins is V_{CC} + 0.5 V. During voltage transitions, outputs may overshoot to V_{CC} + 2.0 V for periods up to 20 ns.*

2. *Minimum DC input voltage on A9 pin is −0.5 V. During voltage transitions, A9 may undershoot V to −2.0 V for periods of up to 20 ns. Maximum DC input voltage on A9 is +13.5 V which may overshoot to 14.0 V_{SS} for periods up to 20 ns.*

3. *No more than one output shorted at a time. Duration of the short circuit should not be greater than one second.*

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.*

OPERATING RANGES

Commercial (C) Devices
Case Temperature (T_C) . . . . 0°C to +70°C

Industrial (I) Devices
Case Temperature (T_C) . . . . −40°C to +85°C

Extended (E) Devices
Case Temperature (T_C) . . . . −55°C to +125°C

Military (M) Devices
Case Temperature (T_C) . . . . −55°C to +125°C

V_{CC} Supply Voltages
V_{CC} for Am29F040-75 . . . . +4.75 V to +5.25 V

V_{CC} for Am29F040
90, 120, 150 . . . . +4.50 V to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS

TTL/NMOS Compatible

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
I_{LI}	Input Load Current	$V_{IN} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC}$ Max		±1.0	µA
I_{LIT}	A9 Input Load Current	$V_{CC} = V_{CC}$ Max, A9 = 12.5 V		50	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC}$ Max		±1.0	µA
I_{CC1}	V_{CC} Active Current (Note 1)	$\overline{CE} = V_{IL}, \overline{OE} = V_{IH}$		40	mA
I_{CC2}	V_{CC} Active Current (Notes 2, 3)	$\overline{CE} = V_{IL}, \overline{OE} = V_{IH}$		60	mA
I_{CC3}	V_{CC} Standby Current	$V_{CC} = V_{CC}$ Max, $\overline{CE} = V_{IH}, \overline{OE} = V_{IH}$		1.0	mA
V_{IL}	Input Low Level		−0.5	0.8	V
V_{IH}	Input High Level		2.0	V_{CC} + 0.5	V
V_{ID}	Voltage for Autoselect and Sector Protect	$V_{CC} = 5.0$ V	11.5	12.5	V
V_{OL}	Output Low Voltage	$I_{OL} = 12$ mA, $V_{CC} = V_{CC}$ Min		0.45	V
V_{OH}	Output High Level	$I_{OH} = −2.5$ mA $V_{CC} = V_{CC}$ Min	2.4		V
V_{LKO}	Low V_{CC} Lock-Out Voltage		3.2	4.2	V

Notes:

1. The I_{CC} current listed includes both the DC operating current and the frequency dependent component (at 6 MHz). The frequency component typically is less than 2 mA/MHz, with $\overline{OE}$ at V_{IH}.

2. I_{CC} active while Embedded Algorithm (program or erase) is in progress.

3. Not 100% tested.

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DC CHARACTERISTICS (continued)
CMOS Compatible

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
I_{LI}	Input Load Current	V_{IN} = Vss to Vcc, Vcc = Vcc Max		±1.0	μA
I_{LIT}	A9 Input Load Current	Vcc = Vcc Max, A9 = 12.5 V		50	μA
I_{LO}	Output Leakage Current	V_{OUT} = Vss to Vcc, Vcc = Vcc Max		±1.0	μA
I_{CC1}	Vcc Active Current (Note 1)	$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}		40	mA
I_{CC2}	Vcc Active Current (Notes 2, 3)	$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}		60	mA
I_{CC3}	Vcc Standby Current	Vcc = Vcc Max, $\overline{CE}$ = Vcc ± 0.5 V, $\overline{OE}$ = V_{IL}		100	μA
V_{IL}	Input Low Level		−0.5	0.8	V
V_{IH}	Input High Level		0.7x Vcc	Vcc +0.3	V
V_{ID}	Voltage for Autoselect and Sector Protect	Vcc = 5.0 V	11.5	12.5	V
V_{OL}	Output Low Voltage	I_{OL} = 12.0 mA, Vcc = Vcc Min		0.45	V
V_{OH1}	Output High Voltage	I_{OH} = −2.5 mA, Vcc = Vcc Min	0.85 Vcc		V
V_{OH2}		I_{OH} = −100 μA, Vcc = Vcc Min	Vcc −0.4		V
V_{LKO}	Low Vcc Lock-out Voltage		3.2	4.2	V

Notes:

1. The Icc current listed includes both the DC operating current and the frequency dependent component (at 6 MHz). The frequency component typically is less than 2 mA/MHz, with $\overline{OE}$ at V_{IH}.

2. Icc active while Embedded Algorithm (program or erase) is in progress.

3. Not 100% tested.

AC CHARACTERISTICS

Read Only Operations Characteristics

Parameter Symbols JEDEC	Parameter Symbols Standard	Description	Test Setup		-75 (Note 1)	-90 (Note 2)	-120 (Note 2)	-150 (Note 2)	Unit
t_{AVAV}	t_{RC}	Read Cycle Time (Note 4)		Min	70	90	120	150	ns
t_{AVQV}	t_{ACC}	Address to Output Delay	$\overline{CE} = V_{IL}$ $\overline{OE} = V_{IL}$	Max	70	90	120	150	ns
t_{ELQV}	t_{CE}	Chip Enable to Output Delay	$\overline{OE} = V_{IL}$	Max	70	90	120	150	ns
t_{GLQV}	t_{OE}	Output Enable to Output Delay		Max	30	35	50	55	ns
t_{EHQZ}	t_{DF}	Chip Enable to Output High Z (Notes 3, 4)		Max	20	20	30	35	ns
t_{GHQZ}	t_{DF}	Output Enable to Output High Z (Notes 3, 4)			20	20	30	35	ns
t_{AXQX}	t_{OH}	Output Hold Time From Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurs First		Min	0	0	0	0	ns

Notes:

1. *Test Conditions:*
   Output Load: 1 TTL gate and 30 pF
   Input rise and fall times: 5 ns
   Input pulse levels: 0.0 V to 3.0 V
   Timing measurement reference level
      Input: 1.5 V
      Output: 1.5 V

2. *Test Conditions:*
   Output Load: 1 TTL gate and 100 pF
   Input rise and fall times: 20 ns
   Input pulse levels: 0.45 V to 2.4 V
   Timing measurement reference level
      Input: 0.8 and 2.0 V
      Output: 0.8 and 2.0 V

3. *Output driver disable time.*
4. *Not 100% tested.*
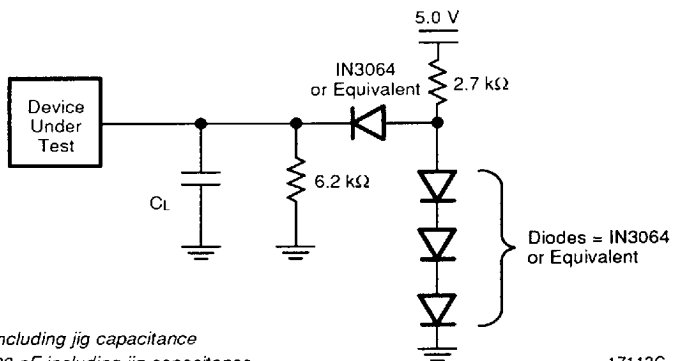
Notes:

For −75: C_L = 30 pF including jig capacitance
For all others: C_L = 100 pF including jig capacitance

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Figure 7. Test Conditions

0257528 0032515 TT9
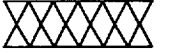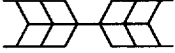
AC CHARACTERISTICS

Write/Erase/Program Operations

Parameter Symbols					-75	-90	-120	-150	Unit
JEDEC	Standard	Description							
tAVAV	twc	Write Cycle Time (Note 4)		Min	70	90	120	150	ns
tAVWL	tAS	Address Setup Time		Min	0	0	0	0	ns
tWLAX	tAH	Address Hold Time		Min	45	45	50	50	ns
tDVWH	tDS	Data Setup Time		Min	30	45	50	50	ns
tWHDX	tDH	Data Hold Time		Min	0	0	0	0	ns
	tOES	Output Enable Setup Time		Min	0	0	0	0	ns
	tOEH	Output Enable Hold Time	Read (Note 4)	Min	0	0	0	0	ns
			Toggle and Data Polling (Note 4)	Min	10	10	10	10	ns
tGHWL	tGHWL	Read Recover Time Before Write		Min	0	0	0	0	ns
tELWL	tCS	CE Setup Time		Min	0	0	0	0	ns
tWHEH	tCH	CE Hold Time		Min	0	0	0	0	ns
tWLWH	tWP	Write Pulse Width		Min	35	45	50	50	ns
tWHWL	tWPH	Write Pulse Width High		Min	20	20	20	20	ns
tWHWH1	tWHWH1	Byte Programming Operation		Min	16	16	16	16	µs
tWHWH2	tWHWH2	Erase Operation (Note 1)		Min	1.5	1.5	1.5	1.5	sec
				Max	30	30	30	30	sec
	tVCS	Vcc Set Up Time (Note 4)		Min	50	50	50	50	µs
	tVLHT	Voltage Transition Time (Notes 2, 4)		Min	4	4	4	4	µs
	tWPP	Write Pulse Width (Note 2)		Min	100	100	100	100	µs
	tOESP	OE Setup Time to WE Active (Notes 2, 4)		Min	4	4	4	4	µs
	tCSP	CE Setup Time to WE Active (Notes 3, 4)		Min	4	4	4	4	µs

Notes:

1. This does not include the preprogramming time.
2. These timings are for Sector Protect/Unprotect operations.
3. This timing is only for Sector Unprotect.
4. Not 100% tested.

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must Be Steady	Will Be Steady
	May Change from H to L	Will Be Changing from H to L
	May Change from L to H	Will Be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010

SWITCHING WAVEFORMS
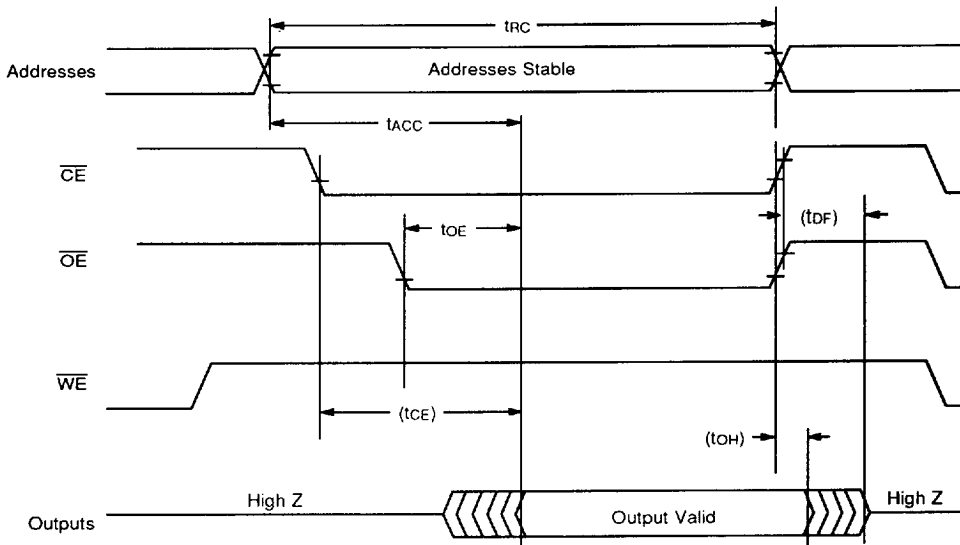
Figure 8. AC Waveforms for Read Operations

17113C-15
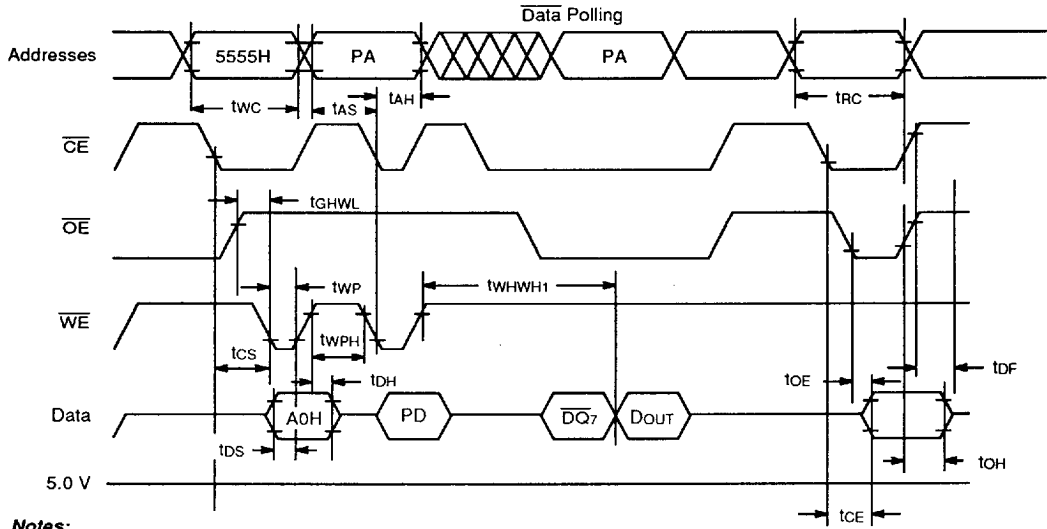
0257528 0032517 871

SWITCHING WAVEFORMS

Notes:

1. PA is address of the memory location to be programmed.

2. PD is data to be programmed at byte address.

3. $\overline{DQ7}$ is the output of the complement of the data written to the device.

4. D_{OUT} is the output of the data written to the device.

5. Figure indicates last two bus cycles of four bus cycle sequence.

Figure 9. Program Operation Timings
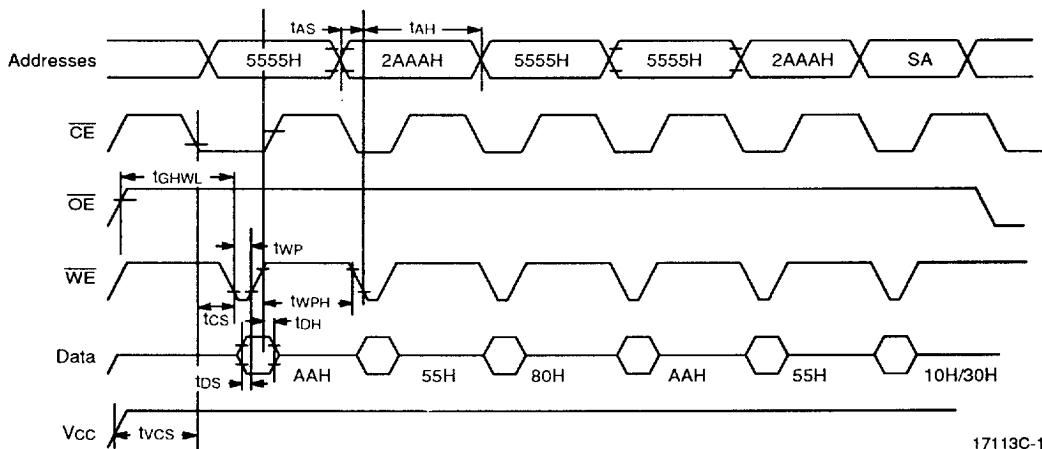
Note: SA is the sector address for Sector Erase. Addresses = don't care for Chip Erase.

Figure 10. AC Waveforms Chip/Sector Erase Operations

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SWITCHING WAVEFORMS

*DQ7=Valid Data (The device has completed the Embedded operation).

17113C-18
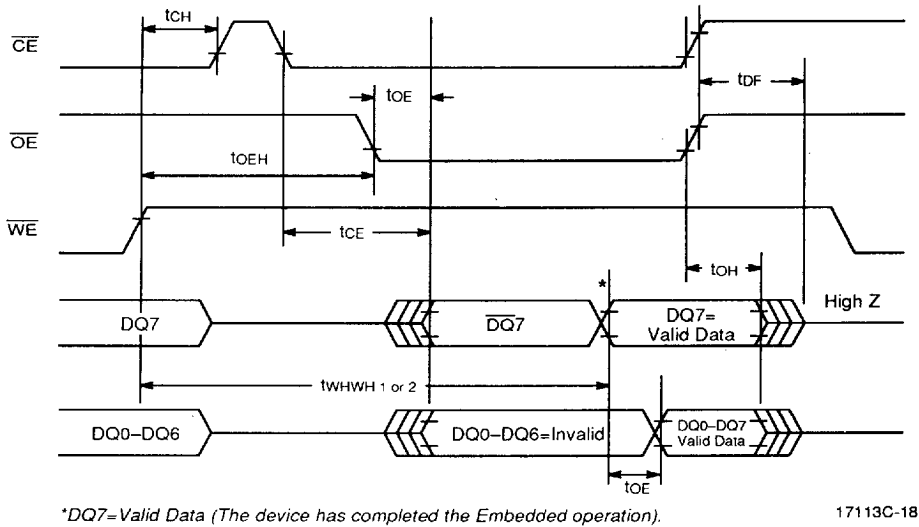
Figure 11. AC Waveforms for Data Polling during Embedded Algorithm Operations

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Note: *DQ6 stops toggling (The device has completed the Embedded operation).
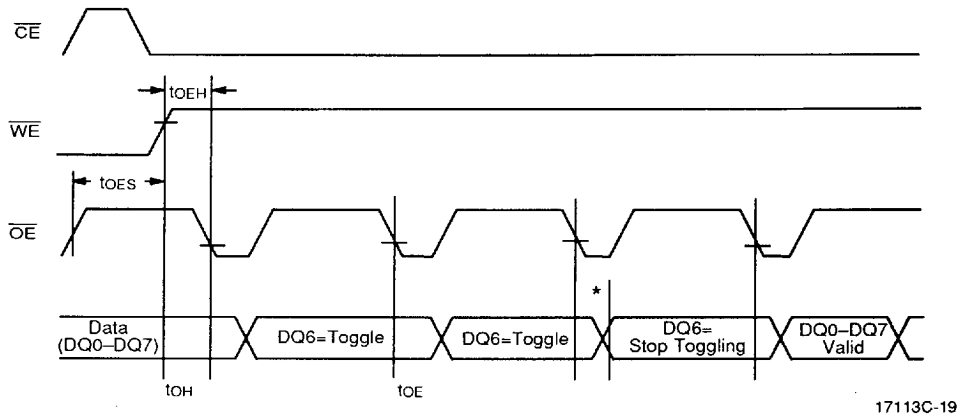
Figure 12. AC Waveforms for Toggle Bit during Embedded Algorithm Operations

SECTOR PROTECTION ALGORITHMS

Sector Protection

The Am29F040 features hardware sector protection which will disable both program and erase operations to an individual sector or any group of sectors. To activate this mode, the programming equipment must force V_{ID} on control pin $\overline{OE}$ and address pin A9. The sector addresses should be set using higher address lines A18, A17, and A16. The protection mechanism begins on the falling edge of the $\overline{WE}$ pulse and is terminated with the rising edge of the same.

It is also possible to verify if a sector is protected during the sector protection operation. This is done by setting A6 = $\overline{CE}$ = $\overline{OE}$ = V_{IL} and $\overline{WE}$ = V_{IH} (A9 remains high at V_{ID}). Reading the device at address location XXX2H, where the higher order addresses (A18, A17, and A16) define a particular sector, will produce 01H at data outputs (DQ0–DQ7) for a protected sector.

Sector Unprotect

The Am29F040 also features a sector unprotect mode, so that a protected sector may be unprotected to incorporate any changes in the code. All sectors should be protected prior to unprotecting any sector.

To activate this mode, the programming equipment must force V_{ID} on control pins $\overline{OE}$, $\overline{CE}$, and address pin A9. The address pins A6, A16, and A12 should be set to V_{IH}. The unprotection mechanism begins on the falling edge of the $\overline{WE}$ pulse and is terminated with the rising edge of the same.

It is also possible to determine if a sector is unprotected in the system by writing the autoselect command and A6 is set at V_{IH}. Performing a read operation at address location XXX2H, where the higher order addresses (A18, A17, and A16) define a particular sector address, will produce 00H at data outputs (DQ0–DQ7) for an unprotected sector.

```
                    ┌─────────────┐
                    │    Start    │
                    └──────┬──────┘
                           │
                    ┌──────▼──────────┐
                    │ Set Up Sector Addr │◄────┐
                    │ (A18, A17, A16)  │      │
                    └──────┬──────────┘       │
                           │                  │
                    ┌──────▼──────┐           │
                    │  PLSCNT = 1 │           │
                    └──────┬──────┘           │
                           │                  │
                    ┌──────▼──────────┐       │
                    │   OE = VID      │       │
                    │ A9 = VID, CE = VIL │    │
                    └──────┬──────────┘       │
                           │                  │
                    ┌──────▼──────────┐       │
                    │ Activate WE Pulse │     │
                    └──────┬──────────┘       │
                           │                  │
                    ┌──────▼──────────┐       │
                    │ Time Out 100 µs │       │
                    └──────┬──────────┘       │
    ┌──────────┐          │                  │
    │ Increment │   ┌──────▼──────────┐       │
    │  PLSCNT   │   │ Power Down OE   │       │
    └──────────┘   │    WE = VIH     │        │
                   │   CE = OE = VIL │        │
                   │ A9 should remain VID │   │
                   └──────┬──────────┘        │
                          │                   │
                   ┌──────▼──────────┐        │
                   │ Read from Sector │       │
                   │Addr = SA, A0 = 0, A1 = 1,│
                   │     A6 = 0      │        │
                   └──────┬──────────┘        │
```

PLSCNT = 25 ? — No

Data = 01H ? — No

Yes / Yes

Device Failed

Protect Another Sector? — Yes

No

Remove VID from A9 Write Reset Command

Sector Protection Complete
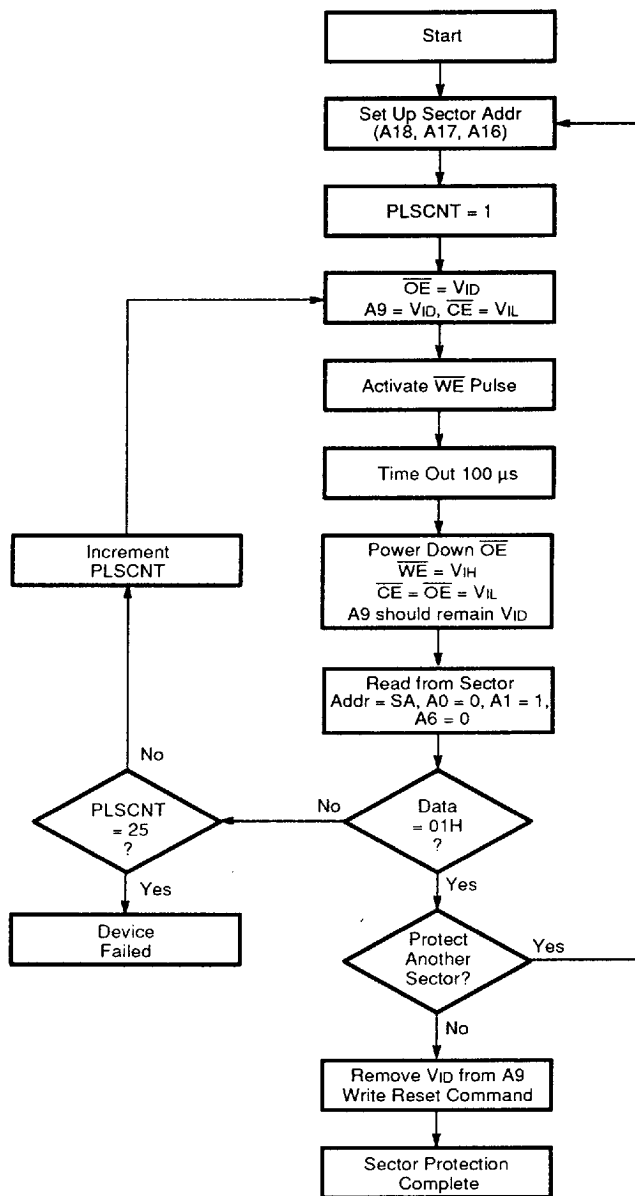
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Figure 13. Sector Protection Algorithm

SWITCHING WAVEFORMS
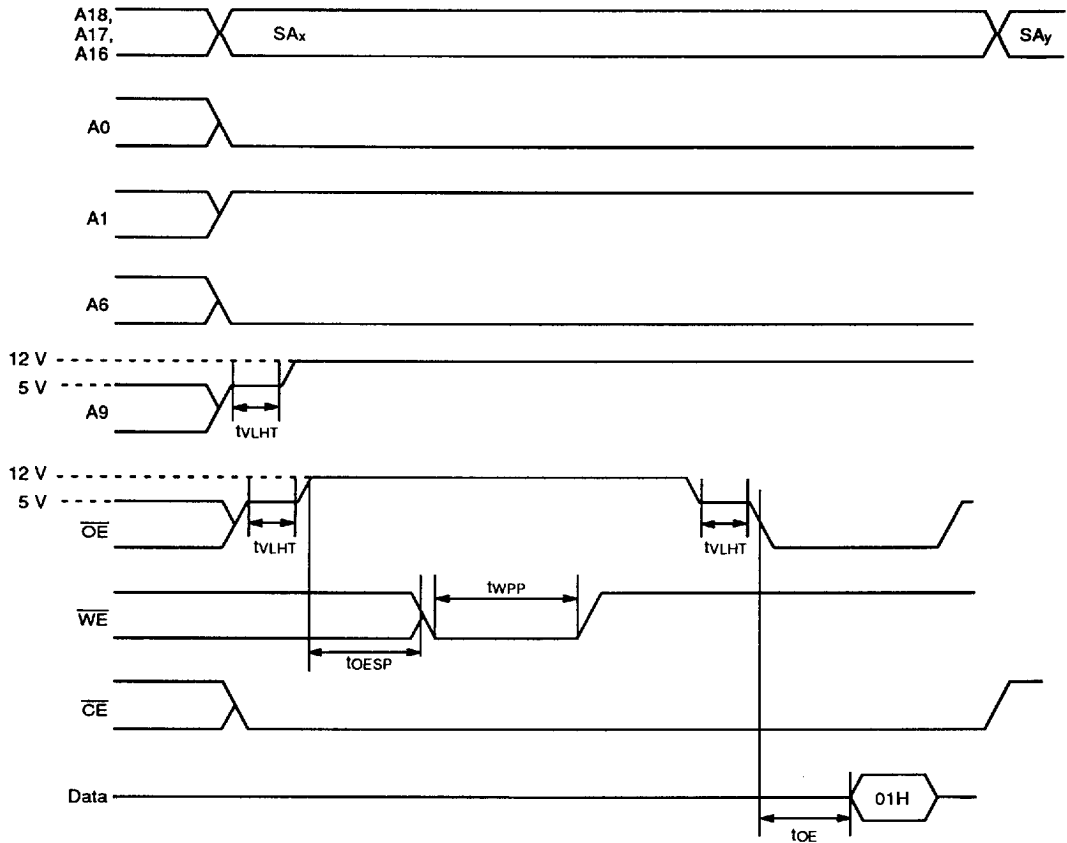
SAx = Sector Address for initial sector
SAy = Sector Address for next sector

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Figure 14. AC Waveforms for Sector Protection

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```
                      ┌──────────────────┐
                      │      Start       │
                      └──────────────────┘
                               │
                      ┌──────────────────┐
                      │ Protect All Sectors │
                      └──────────────────┘
                               │
                      ┌──────────────────┐
                      │    PLSCNT = 1    │
                      └──────────────────┘
                               │
                      ┌──────────────────┐
                      │  Set Up Sector   │◄───────────────────────────┐
                      │  Unprotect Mode  │                            │
                      │  A12 = A16 = VIH │                            │
                      └──────────────────┘                            │
                               │                                      │
                      ┌──────────────────┐                            │
                      │       Set        │                            │
                      │  OE = CE = A9 = VID │                         │
                      └──────────────────┘                            │
                               │                                      │
                      ┌──────────────────┐            ┌──────────────────┐
                      │ Activate WE Pulse │           │    Increment     │
                      └──────────────────┘            │     PLSCNT       │
                               │                      └──────────────────┘
                      ┌──────────────────┐                     ▲
                      │   Time Out 10 ms │                     │
                      └──────────────────┘                     │
                               │                               │
                      ┌──────────────────┐                     │
                      │ Set OE = CE = VIL │                    │
                      │     A9 = VID     │                     │
                      └──────────────────┘                     │
                               │                               │
                      ┌──────────────────────┐                 │
                      │ Set Up Sector Addr SA0 │               │
                      │ Set A1A0 = 10, A6 = 1  │               │
                      └──────────────────────┘                 │
                               │                         No    │
                      ┌──────────────────┐◄──────┐             │
                      │    Read Data     │       │             │
                      │   from Device    │       │             │
                      └──────────────────┘       │             │
                               │                 │             │
                           ◇ Data ◇       ┌──────────────┐  ◇ PLSCNT ◇
                           ◇ = 00H ◇──No──│  Increment   │  ◇ = 1000 ◇
                           ◇   ?   ◇      │ Sector Addr  │  ◇   ?    ◇
                               │Yes       └──────────────┘      │Yes
                          ◇ Sector ◇                      ┌──────────────┐
                          ◇ Addr = SA7 ◇──No──────────────│   Device     │
                          ◇    ?   ◇                      │   Failed     │
                               │Yes                       └──────────────┘
                      ┌──────────────────┐
                      │   Remove VID     │
                      │    from A9       │
                      └──────────────────┘
                               │
                      ┌──────────────────┐
                      │ Sector Unprotect │
                      │   Completed      │
                      └──────────────────┘
```
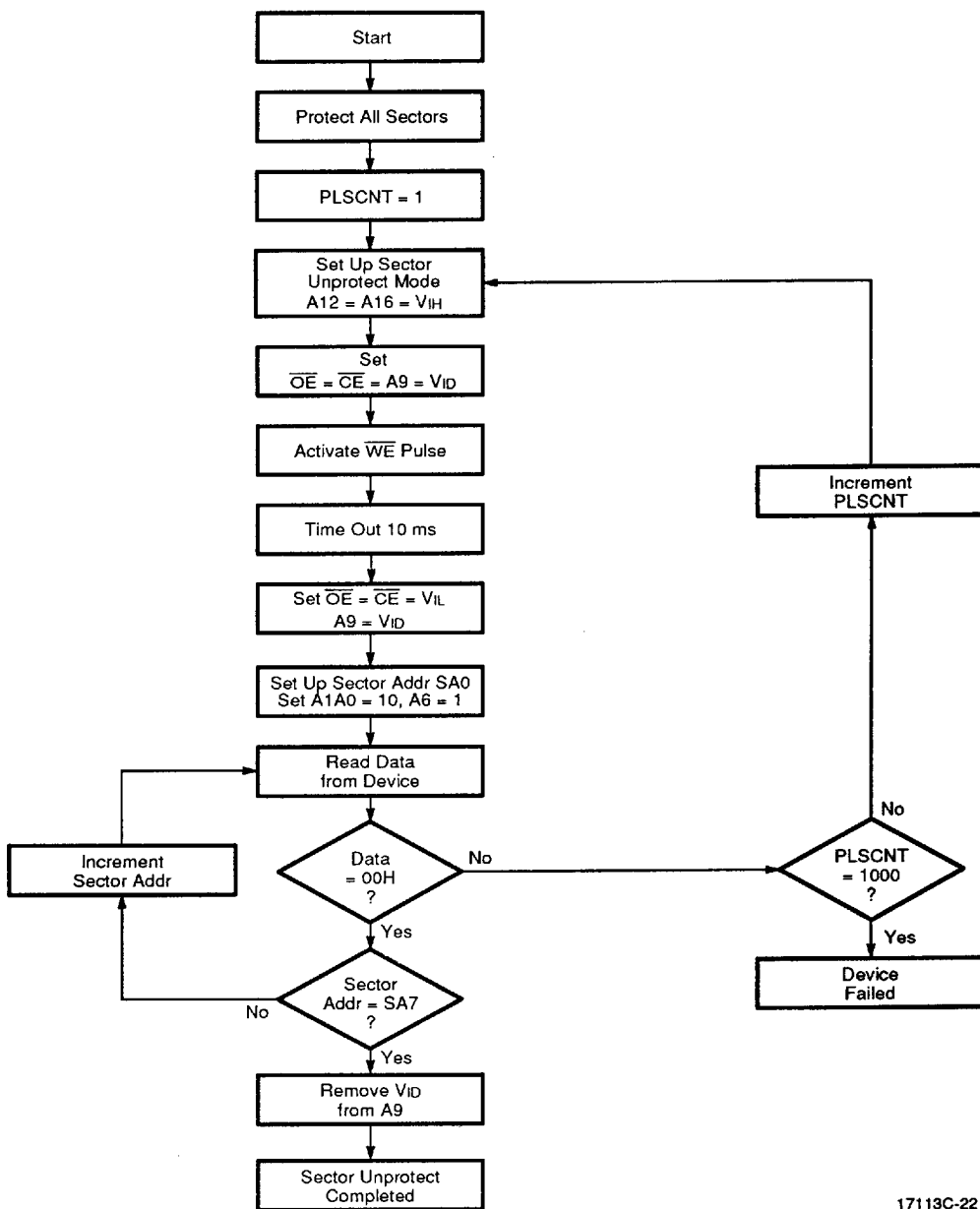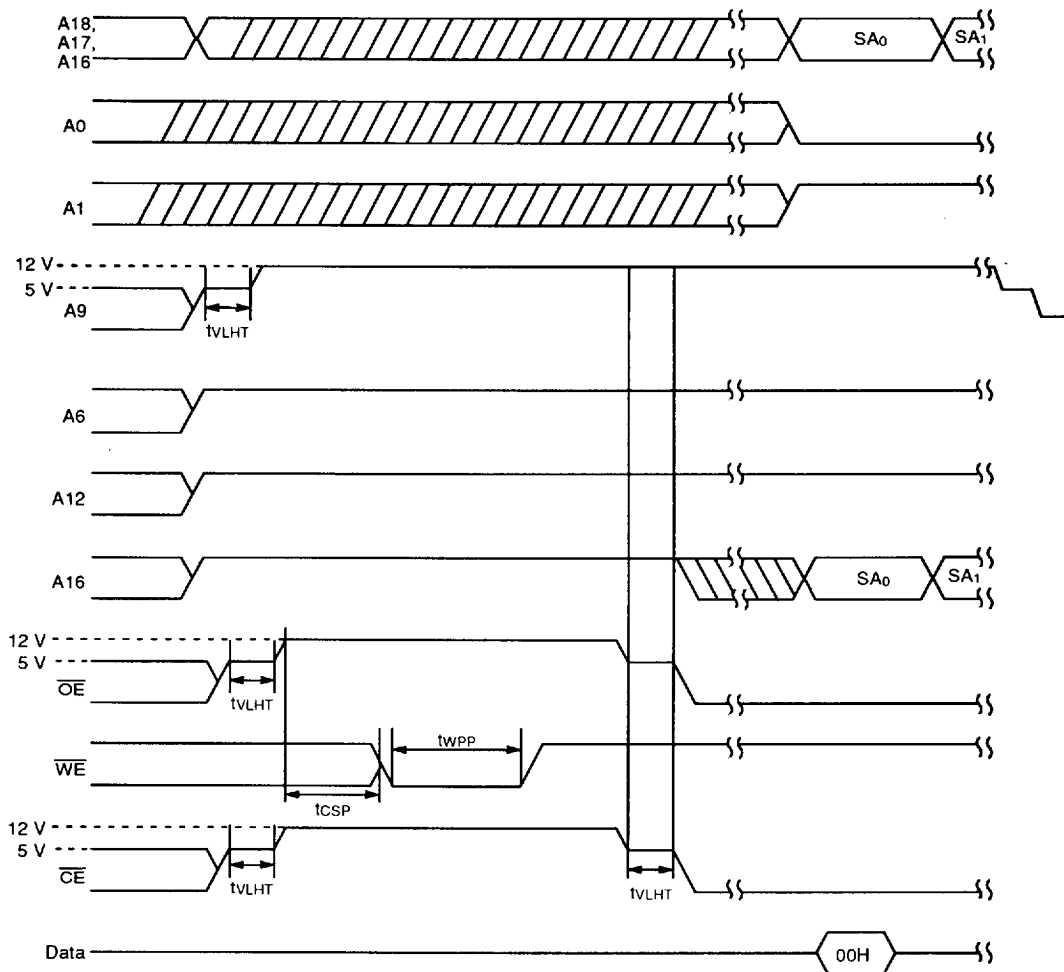
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Notes:

SA0 = Sector Address for initial sector
SA7 = Sector Address for last sector
Please refer to Table 4 for details.

Figure 15. Sector Unprotect Algorithm

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SWITCHING WAVEFORMS

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Figure 16. AC Waveforms for Sector Unprotect

AC CHARACTERISTICS
Write/Erase/Program Operations
Alternate CE Controlled Writes

Parameter Symbols					-75	-90	-120	-150	Unit
JEDEC	Standard	Description							
tAVAV	tWC	Write Cycle Time (Note 4)		Min	70	90	120	150	ns
tAVEL	tAS	Address Setup Time		Min	0	0	0	0	ns
tELAX	tAH	Address Hold Time		Min	45	45	50	50	ns
tDVEH	tDS	Data Setup Time		Min	30	45	50	50	ns
tEHDX	tDH	Data Hold Time		Min	0	0	0	0	ns
	tOES	Output Enable Setup Time		Min	0	0	0	0	ns
	tOEH	Output Enable Hold Time	Read (Note 4)	Min	0	0	0	0	ns
			Toggle and Data Polling (Note 4)	Min	10	10	10	10	ns
tGHEL	tGHEL	Read Recover Time Before Write		Min	0	0	0	0	ns
tWLEL	tWS	WE Setup Time		Min	0	0	0	0	ns
tEHWH	tWH	WE Hold Time		Min	0	0	0	0	ns
tELEH	tCP	CE Pulse Width		Min	35	45	50	50	ns
tEHEL	tCPH	CE Pulse Width High		Min	20	20	20	20	ns
tWHWH1	tWHWH1	Byte Programming Operation		Min	16	16	16	16	μs
tWHWH2	tWHWH2	Erase Operation (Note 1)		Min	1.5	1.5	1.5	1.5	sec
				Max	30	30	30	30	sec
	tVCS	Vcc Set Up Time (Note 4)		Min	50	50	50	50	μs

Notes:

1. This does not include the preprogramming time.
2. These timings are for Sector Protect/Unprotect operations.
3. This timing is only for Sector Unprotect.
4. Not 100% tested.

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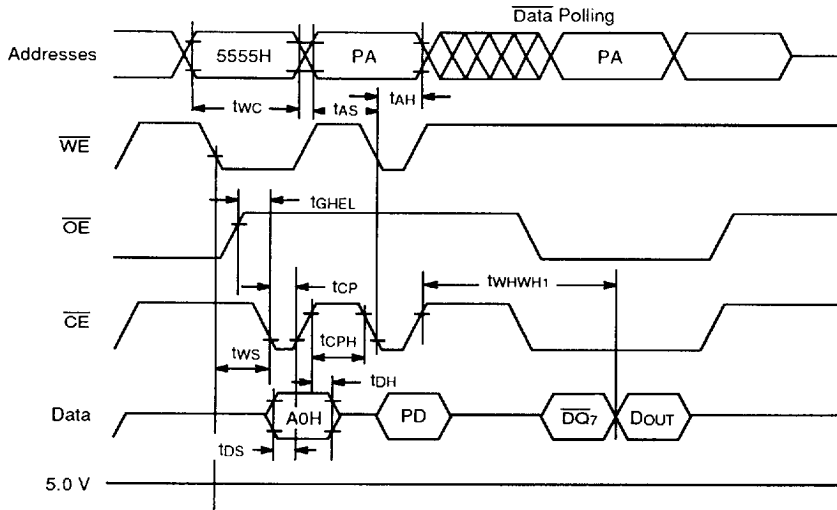
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Notes:

1. PA is address of the memory location to be programmed.

2. PD is data to be programmed at byte address.

3. $\overline{DQ_7}$ is the output of the complement of the data written to the device.

4. D$_{OUT}$ is the output of the data written to the device.

5. Figure indicates last two bus cycles of four bus cycle sequence.

Figure 17. Alternate $\overline{CE}$ Controlled Program Operation Timings

ERASE AND PROGRAMMING PERFORMANCE

Parameter	Min	Limits Typ	Max	Unit	Comments
Chip and Sector Erase Time		1.5 (Note 1)	30	sec	Excludes 00H programming prior to erasure
Byte Programming Time		16	1000 (Note 2)	µs	Excludes system-level overhead
Chip Programming Time		8.5 (Note 1)	50	sec	Excludes system-level overhead
Erase/Program Cycles	100,000	1,000,000		Cycles	

Notes:

1. 25°C, 5 V Vcc, 100,000 cycles
2. When programming a "1" over a "0", the Embedded Algorithms allow for 48 ms byte program time.

LATCHUP CHARACTERISTICS

	Min	Max
Input Voltage with respect to Vss on all I/O pins	−1.0 V	Vcc + 1.0 V
Vcc Current	−100 mA	+100 mA

Includes all pins except Vcc. Test conditions: Vcc = 5.0 V, one pin at a time.

LCC PIN CAPACITANCE

Parameter Symbol	Parameter Description	Test Setup	Typ	Max	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0$	6	7.5	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0$	8.5	12	pF
C_{IN2}	Control Pin Capacitance	$V_{IN} = 0$	7.5	9	pF

Notes:

1. Sampled, not 100% tested.
2. Test conditions $T_A = 25°C$, f = 1.0 MHz

TSOP PIN CAPACITANCE

Parameter Symbol	Parameter Description	Test Setup	Typ	Max	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0$	6	7.5	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0$	8.5	12	pF
C_{IN2}	Control Pin Capacitance	$V_{IN} = 0$	7.5	9	pF

Notes:

1. Sampled, not 100% tested.
2. Test conditions $T_A = 25°C$, f = 1.0 MHz

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PLCC PIN CAPACITANCE

Parameter Symbol	Parameter Description	Test Setup	Typ	Max	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0$	4	6	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0$	8	12	pF
C_{IN2}	Control Pin Capacitance	$V_{PP} = 0$	8	12	pF

Notes:

1. *Sampled, not 100% tested.*
2. *Test conditions $T_A = 25°C$, $f = 1.0$ MHz*

PDIP PIN CAPACITANCE

Parameter Symbol	Parameter Description	Test Setup	Typ	Max	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0$	4	6	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0$	8	12	pF
C_{IN2}	Control Pin Capacitance	$V_{PP} = 0$	8	12	pF

Notes:

1. *Sampled, not 100% tested.*
2. *Test conditions $T_A = 25°C$, $f = 1.0$ MHz*

DATA RETENTION

Parameter	Test Conditions	Min	Unit
Minimum Pattern Data Retention Time	150°C	10	Years
	125°C	20	Years

DATA SHEET REVISION SUMMARY FOR Am29F040

Title

Specify "4 Megabit" density.

Distinctive Characteristics

Include "Read" under first bullet.

General Description

Include statement "Am29F040 is erased when shipped from factory."

Autoselect

Correction in text (V_{ID}) from 13 V to 12.5 V.

Table 5. Am29F040 Command Definition

Clarify Note 1, remove A16, A17, and A18 in second sentence.

Byte Programming

Clarify the statement "hang up the device" by including "exceed timing limits."

DC Characteristics CMOS Compatible Table

Add parameters I_{LI}: "Input Load Current" and I_{LIT}: "A9 Input Load Current" to be consistent with TTL/NMOS compatible table.

Figure 12. AC Waveforms for Toggle Bit during Embedded Algorithm Operations

Identify parameter "t_{OES}"

Figure 15. AC Waveforms for Sector Protection

$\overline{CE}$ Waveform is altered to show preferred method; this change is also reflected in Figure 13. Sector Protection Algorithm flow chart.

Data Retention Table

Added to be consistent with all other data sheets.

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