ADVANCED INFORMATION

1K	Commercial Industrial	X24LC01 X24LC01I	128 x 8 Bit

Electrically Erasable PROM

T-46-13-27

TYPICAL FEATURES

- 3V–6V V_{CC} Operation
- Low Power CMOS
  - —2 mA Active Current Typical
  - —60 μA Standby Current Typical
- Internally Organized 128 x 8
- 2 Wire Serial Interface
  - —Provides Bidirectional Data Transfer Protocol
- Four Byte Page Write Mode
- Self Timed Write Cycle
  - —Typical Write Cycle Time of 5 ms
- Inherent 100+ Years Data Retention
- 8-Pin Mini-DIP Package
- 8-Pin SOIC Package

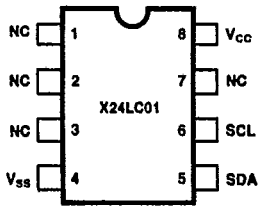
DESCRIPTION

The X24LC01 is a CMOS 1024 bit serial E²PROM, internally organized as 128 x 8. The X24LC01 features a serial interface and software protocol allowing operation on a two wire bus.

Xicor E²PROMs are designed and tested for applications requiring extended endurance.

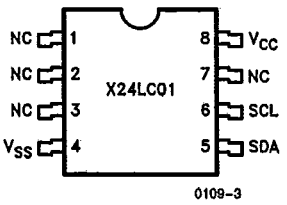
PIN CONFIGURATIONS

PLASTIC



0109-2

SOIC



0109-3

PIN NAMES

1 to 3	No Connect
4	V_{SS}
5	SDA Serial Data
6	SCL Serial Clock
7	No Connect
8	V_{CC} +3V to +6V

X24LC01, X24LC01I

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias
X24LC01 ..... −10°C to +85°C
X24LC01I ..... −65°C to +135°C
Storage Temperature ..... −65°C to +150°C
Voltage on any Pin with
Respect to V_{SS} ..... −1.0V to +7V
D.C. Output Current ..... 5 mA
Lead Temperature
(Soldering, 10 Seconds) ..... 300°C

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. OPERATING CHARACTERISTICS

X24LC01 T_A = 0°C to +70°C, V_{CC} = +3V to +6V, unless otherwise specified.
X24LC01I T_A = −40°C to +85°C, V_{CC} = +3V to +6V, unless otherwise specified.

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.(1)	Max.		
I_{CC}	Power Supply Current		2.0	3.0	mA	f_{SCL} = 100 KHz
I_{SB}(2)	Standby Current V_{CC} = 6V			150	µA	V_{IN} = GND or V_{CC}
I_{SB}(2)	Standby Current V_{CC} = 3V			50	µA	V_{IN} = GND or V_{CC}
I_{LI}	Input Leakage Current		0.1	10	µA	V_{IN} = GND to V_{CC}
I_{LO}	Output Leakage Current		0.1	10	µA	V_{OUT} = GND to V_{CC}
V_{IL}(3)	Input Low Voltage	−1.0		V_{CC} ×0.3	V	
V_{IH}(3)	Input High Voltage	V_{CC} ×0.7		V_{CC} +0.5	V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 2.1 mA

CAPACITANCE T_A = 25°C, f = 1.0 MHz, V_{CC} = 5V

Symbol	Test	Max.	Units	Conditions
$C_{I/O}$(4)	Input/Output Capacitance (SDA)	8	pF	$V_{I/O}$ = 0V
C_{IN}(4)	Input Capacitance (SCL)	6	pF	V_{IN} = 0V

A.C. CONDITIONS OF TEST

Input Pulse Levels	V_{CC} ×0.1 to V_{CC} ×0.9
Input Rise and Fall Times	10 ns
Input and Output Timing Levels	V_{CC} ×0.5
Output Load	1 TTL Gate and C_L = 100 pF

Notes: (1) Typical values are for T_A = 25°C and nominal supply voltage (5V).
(2) SDA and SCL require pull-up resistor.
(3) V_{IL} min. and V_{IH} max. are for reference only and are not tested.
(4) This parameter is periodically sampled and not 100% tested.

SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from Low to High	Will change from Low to High
	May change from High to Low	Will change from High to Low
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

X24LC01, X24LC01I

A.C. CHARACTERISTICS LIMITS

X24LC01 T_A = 0°C to +70°C, V_{CC} = +3V to +6V, unless otherwise specified.
X24LC01I T_A = −40°C to +85°C, V_{CC} = +3V to +6V, unless otherwise specified.

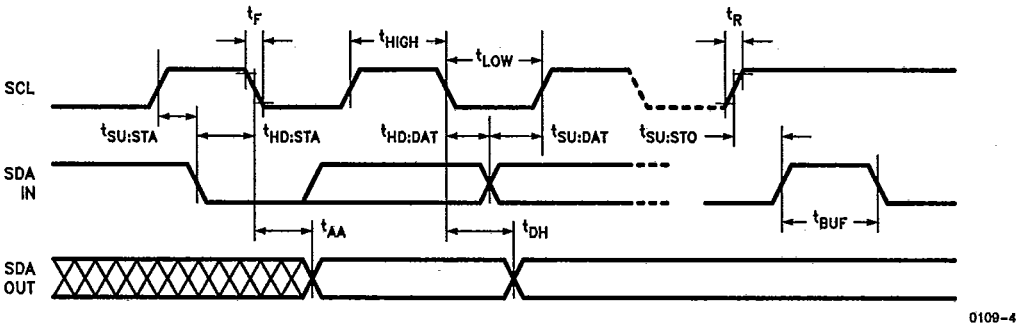
Read & Write Cycle Limits

Symbol	Parameter	Min.	Max.	Units
f_{SCL}	SCL Clock Frequency	0	100	KHz
T_I	Noise Suppression Time Constant at SCL, SDA Inputs		100	ns
t_{AA}	SCL Low to SDA Data Out Valid	0.3	3.5	μs
t_{BUF}	Time the Bus Must Be Free Before a New Transmission Can Start	4.7		μs
$t_{HD:STA}$	Start Condition Hold Time	4.0		μs
t_{LOW}	Clock Low Period	4.7		μs
t_{HIGH}	Clock High Period	4.0		μs
$t_{SU:STA}$	Start Condition Setup Time	4.7		μs
$t_{HD:DAT}$	Data In Hold Time	0		μs
$t_{SU:DAT}$	Data In Setup Time	250		ns
t_R	SDA and SCL Rise Time		1	μs
t_F	SDA and SCL Fall Time		300	ns
$t_{SU:STO}$	Stop Condition Setup Time	4.7		μs
t_{DH}	Data Out Hold Time	300		ns

Typical Power-Up Timing

Symbol	Parameter	Typ.(5)	Units
t_{PUR}(6)	Power-Up to Read Operation	2.0	ms
t_{PUW}(6)	Power-Up to Write Operation	2.0	ms

Bus Timing



Notes: (5) Typical values are for T_A = 25°C and nominal supply voltage (5V).
(6) This parameter is periodically sampled and not 100% tested.

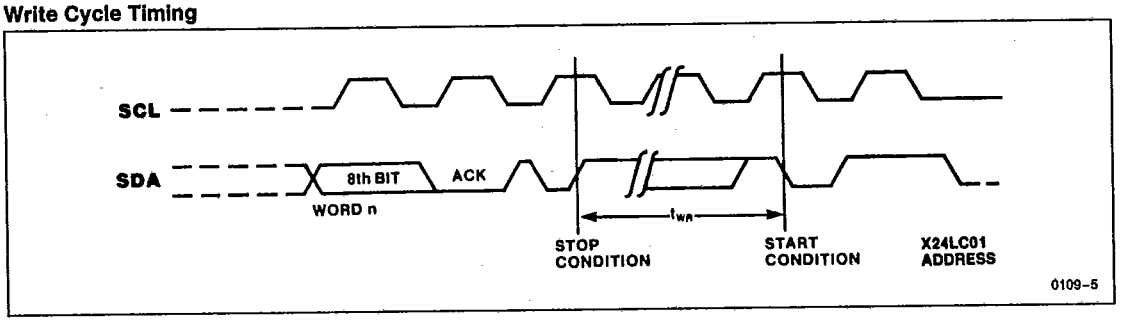
X24LC01, X24LC01I

Write Cycle Limits

Symbol	Parameter	Min.	Typ.(7)	Max.	Units
t_{WR}(8)	Write Cycle Time		5	10	ms

The write cycle time is the time from a valid stop condition of a write sequence to the end of the internal erase/program cycle. During the write cycle, the X24LC01 bus interface circuits are disabled, SDA is allowed to remain high, and the device does not respond to its word address.

Write Cycle Timing



PIN DESCRIPTIONS

Serial Clock (SCL)

The SCL input is used to clock all data into and out of the device.

Serial Data (SDA)

SDA is a bidirectional pin used to transfer data into and out of the device. It is an open drain output and may be wire-ORed with any number of open drain or open collector outputs.

An open collector output requires the use of a pull-up resistor. For selecting typical values, refer to the Guidelines for Calculating Typical Values of Bus Pull-Up Resistors graph.

DEVICE OPERATION

The X24LC01 supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter, and the receiving device as the receiver. A controller initiates data transfers, and provides the clock for both transmit and receive operations.

Clock and Data Conventions

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions. Refer to Figures 1 and 2.

Start Condition

All commands are preceded by the start condition, which is a HIGH to LOW transition of SDA when SCL is HIGH. The X24LC01 continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met. This is true only if the previous sequence was correctly terminated with a stop condition.

Notes: (7) Typical values are for T_A = 25°C and nominal supply voltage (5V).

(8) t_{WR} is the minimum cycle time to be allowed from the system perspective unless polling techniques are used. It is the maximum time the device requires to automatically complete the internal write operation.

Figure 1: Data Validity

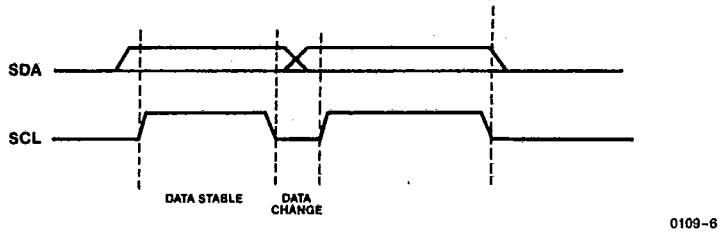
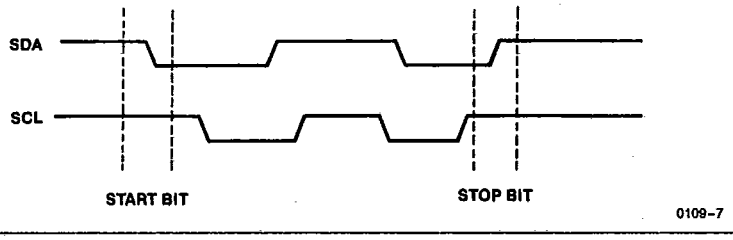


Figure 2: Definition of Start and Stop



Stop Condition

All communications are terminated by a stop condition, which is a LOW to HIGH transition of SDA when SCL is HIGH. The stop condition is also used by the X24LC01 to place the device in the standby power mode after a read sequence. A stop condition can only be issued after the transmitting device has released the bus.

Acknowledge

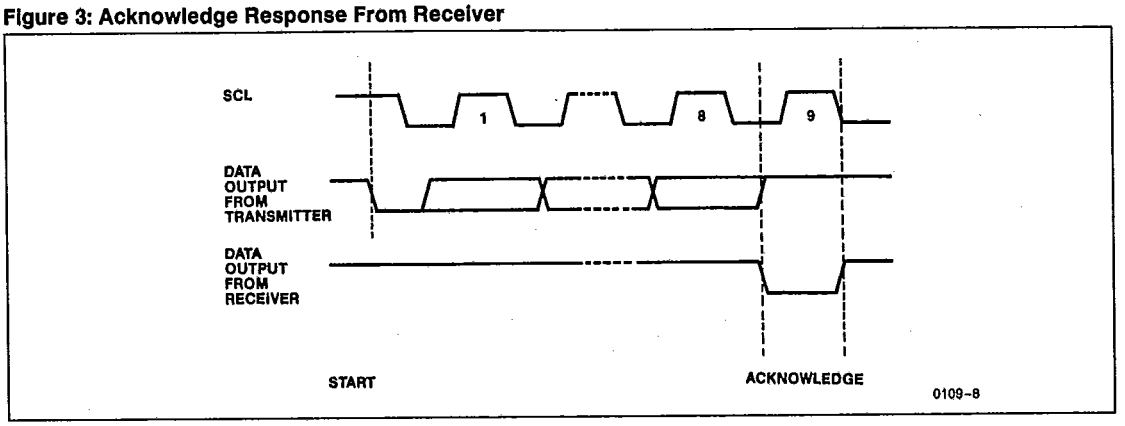
Acknowledge is a software convention used to indicate successful data transfers. The transmitting device will release the bus after transmitting eight bits. During the ninth clock cycle the receiver will pull the SDA line LOW to acknowledge that it received the eight bits of data. Refer to Figure 3.

The X24LC01 will always respond with an acknowledge after recognition of a start condition, a seven bit word address and a R/$\overline{W}$ bit. If a write operation has been selected, the X24LC01 will respond with an acknowledge after each byte of data is received.

In the read mode the X24LC01 will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the controller, the X24LC01 will continue to transmit data. If an acknowledge is not detected, the X24LC01 will terminate further data transmissions and await the stop condition to return to the standby power mode.

X24LC01, X24LC01I

Figure 3: Acknowledge Response From Receiver

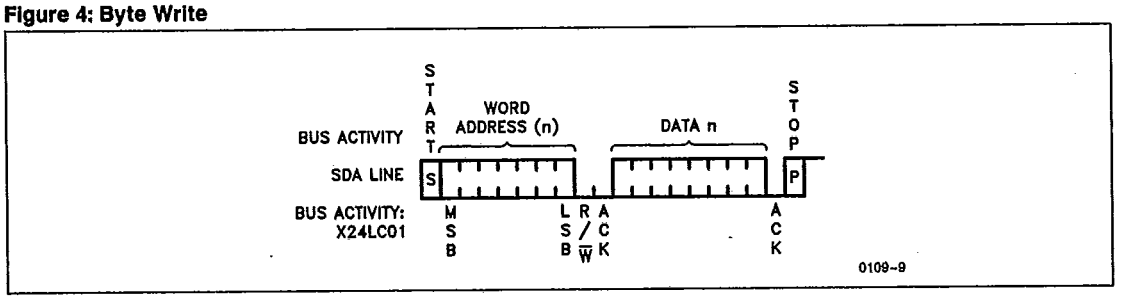


WRITE OPERATIONS

Byte Write

To initiate a write operation, the controller sends a start condition followed by a seven bit word address and a write bit. The X24LC01 responds with an acknowledge, then waits for eight bits of data and then responds with an acknowledge. The controller then terminates the transfer by generating a stop condition, at which time the X24LC01 begins the internal write cycle to the nonvolatile memory. While the internal write cycle is in progress, the X24LC01 inputs are disabled, and the device will not respond to any requests from the controller. Refer to Figure 4 for the address, acknowledge and data transfer sequence.

Figure 4: Byte Write



Page Write

The most significant five bits of the word address define the page address. The X24LC01 is capable of a four byte page write operation. It is initiated in the same manner as the byte write operation, but instead of terminating the transfer of data after the first data byte, the controller can transmit up to three more bytes. After the receipt of each data byte, the X24LC01 will respond with an acknowledge.

After the receipt of each data byte, the two low order address bits are internally incremented by one. The high order five bits of the address remain constant. If the controller should transmit more than four data bytes prior to generating the stop condition, the address counter will "roll over" and the previously transmitted data will be overwritten. As with the byte write operation, all inputs are disabled until completion of the internal write cycle. Refer to Figure 5 for the address, acknowledge and data transfer sequence.

Acknowledge Polling

The disabling of the inputs can be used to take advantage of the typical 5 ms write cycle time. Once the stop condition is issued to indicate the end of the host's write operation the X24LC01 initiates the internal write cycle. ACK polling can be initiated immediately. This involves issuing the start condition followed by the word address for a read or write operation. If the X24LC01 is still busy with the write operation no ACK will be returned. If the X24LC01 has completed the write operation an ACK will be returned and the controller can then proceed with the next read or write operation.

READ OPERATIONS

To terminate a read operation, the controller must **either** issue a stop condition during the ninth cycle **or** hold SDA high during the ninth clock cycle (i.e. not issue an acknowledge) and then issue a stop condition later.

Byte Read

To initiate a read operation, the controller sends a start condition followed by a seven bit word address and a read bit. The X24LC01 responds with an acknowledge and then transmits the eight bits of data. If the controller does not acknowledge the transfer and generates a stop condition, the X24LC01 will discontinue transmission. Refer to Figure 6 for the start, word address, read bit, acknowledge and data transfer sequence.

Figure 5: Page Write

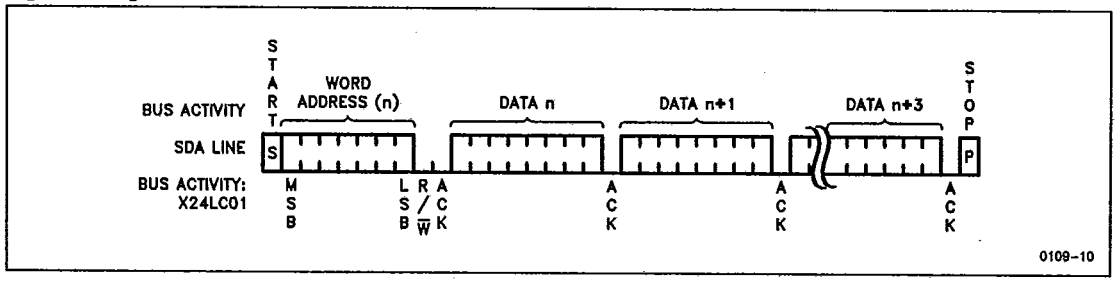
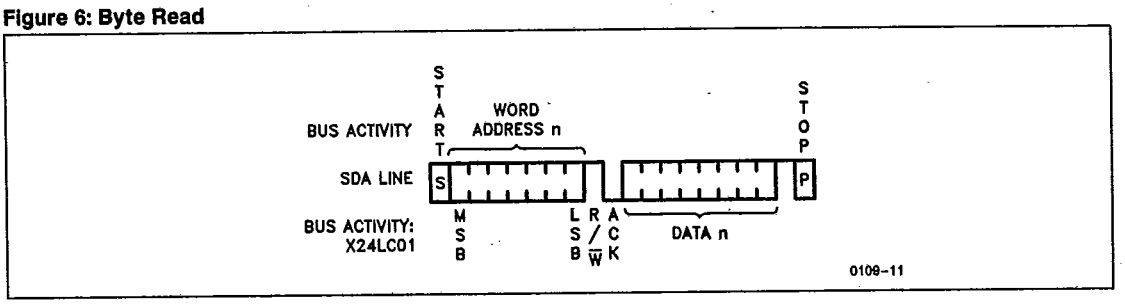


Figure 6: Byte Read

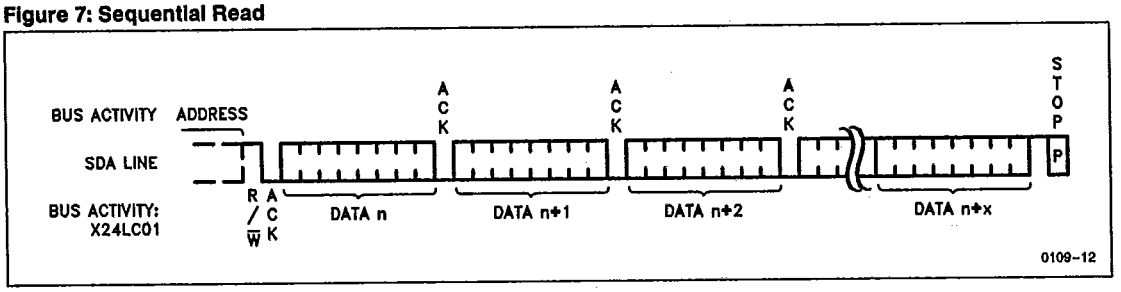


Sequential Read

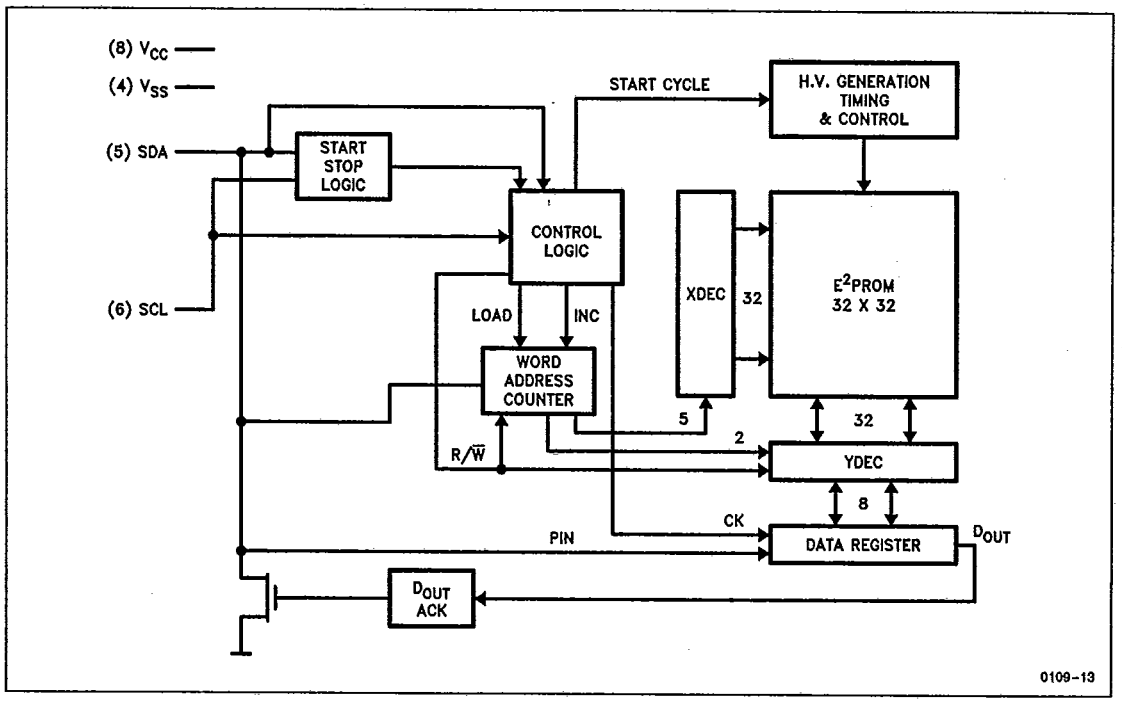
Sequential read is initiated in the same manner as the byte read. The first data byte is transmitted as with the byte read mode, however, the controller now responds with an acknowledge, indicating it requires additional data. The X24LC01 continues to output data for each acknowledge received. The read operation is terminated by the controller not responding with an acknowledge and generating a stop condition.

The data output is sequential, with the data from address n followed by the data from n+1. The address counter for read operations increments all address bits, allowing the entire memory contents to be serially read during one operation. When the highest address is reached, the counter "rolls over" to address 0 and the X24LC01 continues to output data for each acknowledge received. Refer to Figure 7 for the address, acknowledge and data transfer sequence.

Figure 7: Sequential Read

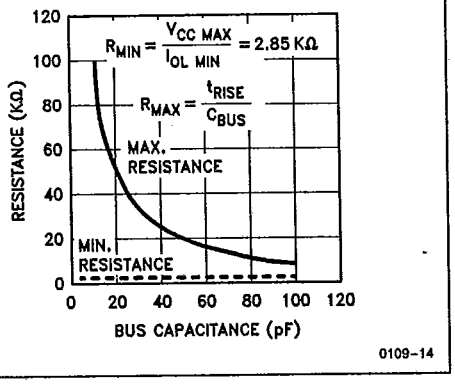


FUNCTIONAL DIAGRAM



X24LC01, X24LC01I

Guidelines for Calculating Typical Values of Bus Pull-Up Resistors



ORDERING INFORMATION

SERIAL E²PROMs

Device Order Number	Organization	Package										Temp. Range	Process Technology	Processing Level
		S	P	D	C	F1	F2	K	J	E	G			
X24LC01S	128 x 8	•										†	CMOS	Standard
X24LC01SI	128 x 8	•										I	CMOS	Standard
X24LC01P	128 x 8		•									†	CMOS	Standard
X24LC01PI	128 x 8		•									I	CMOS	Standard

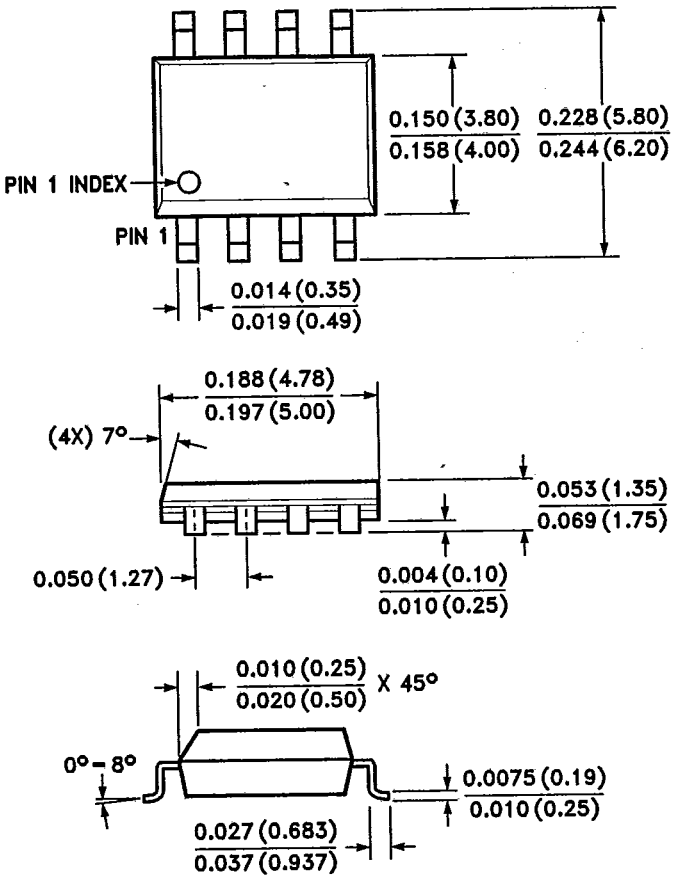
Key:

† = Blank = Commercial = 0°C to +70°C
I = Industrial = −40°C to +85°C
M = Military = −55°C to +125°C

S = 8-Lead Plastic Small Outline Gull Wing
P = 8-Lead Plastic DIP
D = Cerdip
C = Side Braze
F1 = Ceramic Flat Pack for X2864A, X2864B, X2864H and X28C64
F2 = Ceramic Flat Pack for X28C256 and X28C256B
K = Ceramic Pin Grid Array
J = J-Hook Plastic Leaded Chip Carrier
E = Ceramic Leadless Chip Carrier (Solder Seal)
G = Ceramic Leadless Chip Carrier (Glass Frit Seal)

PACKAGING INFORMATION

8-LEAD PLASTIC SMALL OUTLINE GULL WING PACKAGE TYPE S

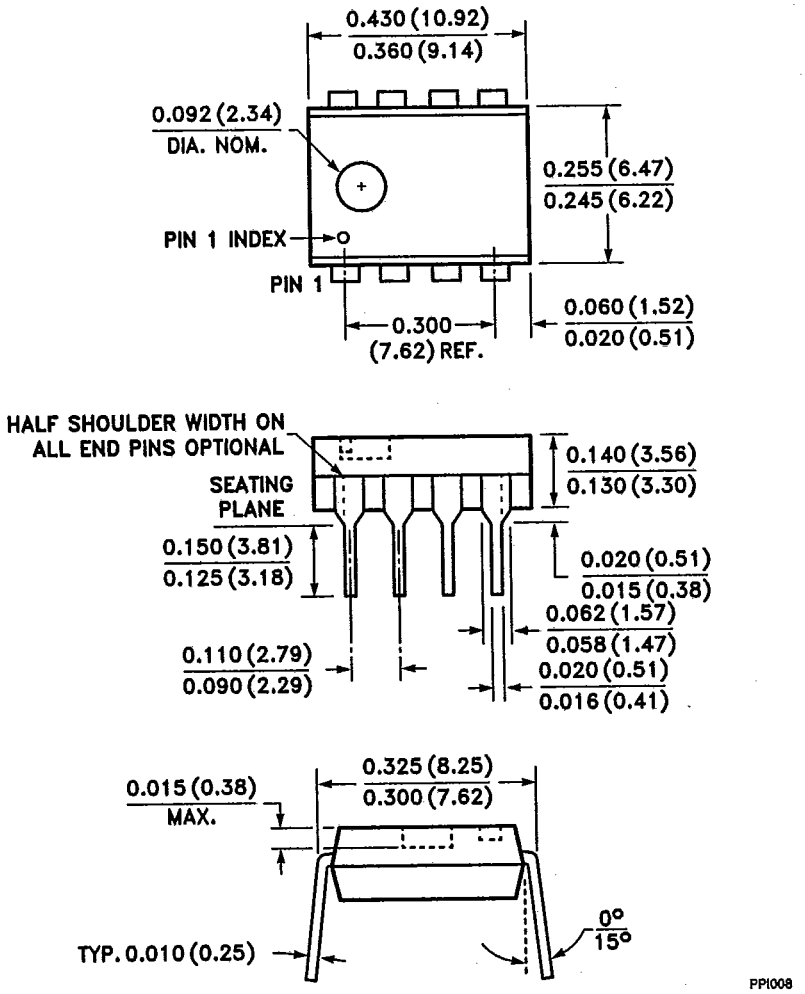


PSE008

NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

PACKAGING INFORMATION

8-LEAD PLASTIC DUAL IN-LINE PACKAGE TYPE P



NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)